

Impact of the NW-TFET Diameter on the Efficiency and the Intrinsic Voltage Gain From a Conduction Regime Perspective

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Abstract—In this work, the impact of the diameter on vertical nanowire tunnel field effect transistors is analyzed focusing on the conduction mechanism and analog parameters, considering different conduction regimes. The diameter influence is investigated using experimental and simulation data. The impact of the diameter on the analog parameters is analyzed, considering both weak and strong conduction. For a smaller diameter, the impact of band-to-band tunneling (BTBT) on the device characteristics increases, showing opposite trends for weak and strong conduction. For strong conduction, a degradation of the intrinsic voltage gain occurs for very small diameters, because the device has less available area for the occurrence of tunneling. For weak conduction, the reduction of the diameter increases the BTBT along the channel/source junction without showing this degradation.

Index Terms—Analog performance, band-to-band tunneling (BTBT), conduction mechanism, tunnel field effect transistor (TFET).

I. INTRODUCTION

TUNNEL field effect transistors (TFETs) are devices in which the designed conduction mechanism is the band-to-band tunneling (BTBT) [1]. TFETs are candidate solutions for low-power/low-voltage applications due to their capability to overcome, at room temperature, the theoretical silicon (Si) MOSFET limit of 60 mV/dec for the subthreshold swing [2]–[4].

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Although the BTBT mechanism allows an increase in the switching speed of the transistor, it provides a very low ON-state current (I_{ON}) in conventional Si TFETs. One strategy that is widely used to improve this parameter is the use of different materials with a reduced bandgap at the source of the devices. The reduced bandgap of the source leads to a reduction of the tunneling path, which improves the BTBT mechanism, increasing the I_{ON} [5]–[8].

Even though the TFET device was developed in order to replace the conventional MOSFET for switching applications, recent studies have been done focusing on their analog behavior, demonstrating that TFETs also have a good potential for analog applications [9]–[13]. The TFETs show promising analog performance since BTBT is their dominant conduction mechanism, which presents low output conduction values (high early voltage) when compared with MOSFET devices [14], provided the channel length is sufficiently large to avoid drain induced barrier thinning [15].

Heading in the same direction as the MOSFETs, new device architectures have been studied to increase the electrostatic control by the gate. One promising technology is the vertical nanowire, which is a gate all around structure [16]. The use of this structure in TFET devices improves the control of the tunneling carriers, improving I_{ON} , the transconductance, the subthreshold swing, and other important analog parameters [17], [18].

In this work, the effect of the diameter in vertical nanowire TFETs is investigated focusing on the conduction mechanism and its influence on the analog parameters, thereby considering different conduction regimes. The analyzed analog parameters were the transistor efficiency (gm/I_{DS}), the transconductance (gm), the output conduction (g_D), and the intrinsic voltage gain (A_V).

II. EXPERIMENTAL AND SIMULATION DETAILS

The experimental data have been obtained on vertical nanowire TFETs fabricated at imec, in Belgium. The devices are n-type NW-TFETs that use a top down vertical process flow [19], with a total channel length (L_{CH}) of 220 nm, a physical gate length (L_G) of 150 nm, a gate/source overlap (L_{GS}) of 30 nm and a gate/drain underlap (L_{GD}) of 100 nm.

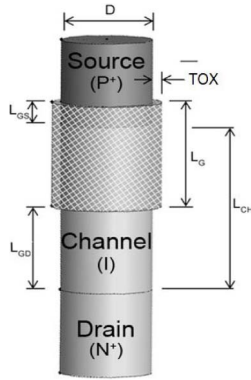


Fig. 1. Structure of the studied devices.

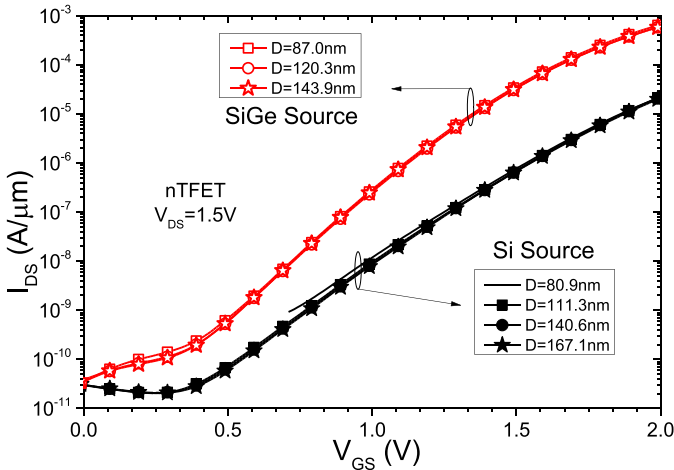


Fig. 2. Experimental normalized drain current as a function of gate bias for TFETs with different diameters and two source compositions.

The schematic of the experimental device is presented in Fig. 1. The gate dielectric consists of 3 nm of HfO_2 on top of 1 nm of SiO_2 , resulting in an equivalent oxide thickness of 2 nm. The drain region is doped with 2×10^{19} at/cm^3 As, the channel is lightly doped with 1×10^{16} at/cm^3 As, and the source is doped with 1×10^{20} at/cm^3 boron. Two different source compositions were studied, one of pure Si and the other of $\text{Si}_{0.73}\text{Ge}_{0.27}$. The $\text{Si}_{0.73}\text{Ge}_{0.27}$ source is obtained by the deposition of a layer of $\text{Si}_{0.73}\text{Ge}_{0.27}$ on top of the lightly doped silicon channel layer. More details regarding these structures can be found in [7].

The experimental devices used in this work have an effective diameter ranging from 167 down to 81 nm and have 2400 nanowires in parallel.

Simulations of the TFET performance were performed for nanowire diameters beyond the experimental values using the Atlas simulator from Silvaco without including quantum confinement models, considering the different current conduction mechanisms: Shockley–Read–Hall (SRH) recombination, trap assisted tunneling (TAT), and nonlocal BTBT. The simulation was used to reach diameters down to 15 nm.

III. ANALYSIS AND RESULTS

Fig. 2 shows the drain current (I_{DS}), normalized by the diameter, as a function of the gate voltage (V_{GS}) for two

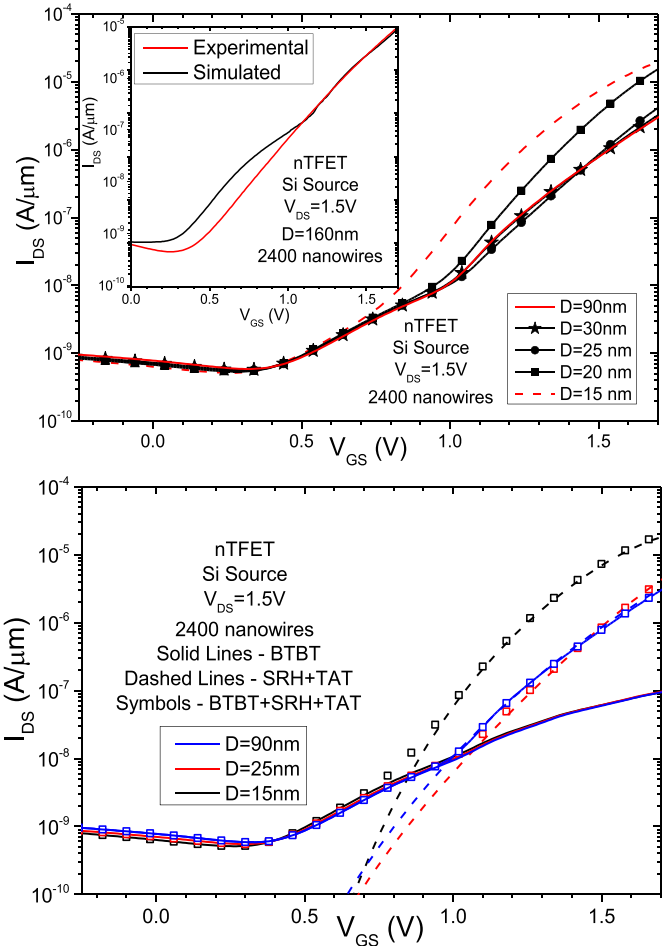


Fig. 3. Simulated normalized drain current as a function of gate bias for TFETs with (a) different diameters and the calibration in the inset and (b) its current composition.

different devices, one with a source of pure Si and another with a composition of $\text{Si}_{0.73}\text{Ge}_{0.27}$. Initially, one can observe that the on-state I_{DS} for the SiGe source device is higher than for the Si source counterpart due to the reduction of the tunnel path caused by the lower bandgap energy of the SiGe source [7].

One important characteristic that can be noted is that the normalized I_{DS} remains almost independent on the diameter, for all the available diameters, considering devices with both source compositions. For wide diameters, there is only a diameter influence on the nonnormalized I_{DS} [20].

In order to extrapolate the results for smaller diameters, numerical simulations have been carried out for diameters down to 15 nm. Fig. 3(a) shows the I_{DS} , normalized by the diameter, as a function of V_{GS} for simulated Si source nTFETs with smaller diameters. The inset of Fig. 3 illustrates the calibration used for the simulation. From Fig. 3, it is possible to observe that there is a noticeable increase in the normalized I_{ON} with the reduction of the diameter. This increase in the ON-state current is related with the dominant conduction mechanism. These results suggest that for narrower NW-TFETs, the gate to channel coupling is better, resulting in a higher BTBT current.

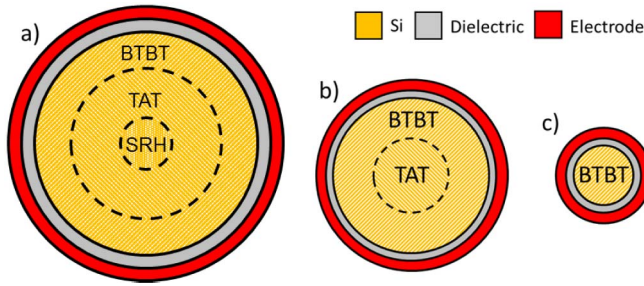


Fig. 4. Schematic of the cross section of a vertical nanowire nTFET with (a) large, (b) medium, and (c) small diameters, highlighting their dominant conduction mechanism as demonstrated by simulated data in Fig. 8.

TFETs can present three types of current mechanisms: 1) generation and recombination (SRH); 2) TAT; and 3) BTBT. The discretized conduction mechanism components are presented in Fig. 3(b), for different diameters. Fig. 4 shows a representation of a cross section of the source/channel junction of the used nanowire nTFET. In larger diameter devices [Fig. 4(a)], the current conduction is dominated by BTBT only near the Si/Oxide interface. As the potential decreases toward the center of the nanowire, the conduction band of the channel region becomes more distant from the valence band of the source. This generates a transition among the predominant conduction mechanisms along the diameter, with BTBT the predominant mechanism near the surface, becoming TAT at intermediate positions and closer to the center mainly SRH occurs.

For a medium size diameter [Fig. 4(b)], there is sufficient interaction of the gate potential in the center of the device, leading to an increase of the BTBT and TAT influence on the center. This results in a predominance of BTBT near the surface and a predominance of TAT in the center. For a small diameter [Fig. 4(c)], the impact of the gate potential at the center of the device is strong enough to guarantee that BTBT is the dominant mechanism along all the diameter of the nanowire [20].

The fact that the BTBT has become the dominant mechanism along the whole cross section is responsible for the increase in the normalized I_{DS} considering smaller diameters in Fig. 3(a). From Fig. 3(a), it is also possible to observe that the onset voltage (V_{ON}), the minimum gate voltage necessary for BTBT to become the dominant mechanism, decreases for a narrower nanowire, in agreement with the observations in [21].

In order to investigate this phenomenon, V_{ON} has been extracted (inset of Fig. 5) using the activation energy (E_A) criterion [7]. This criterion defines that for an E_A higher than 0.5 eV, the dominant conduction mechanism is SRH, for an E_A lower than 0.1 eV, the dominant mechanism is BTBT, and for E_A values between 0.5 and 0.1 eV, the dominant mechanism is TAT.

Fig. 5 presents the E_A as a function of V_{GS} for different diameters, obtained by the Arrhenius method, which is extracted using (1). From Fig. 5, it is possible to obtain the V_{ON} by analyzing the V_{GS} value when E_A is 0.1 eV (inset of Fig. 5). One can notice that for the larger diameters, the V_{ON} is almost constant, but when the diameter is reduced to values lower than 30 nm, V_{ON} starts to decrease, reducing

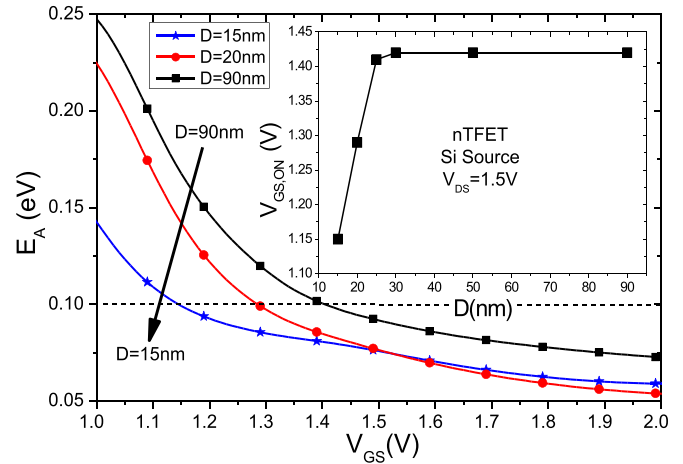


Fig. 5. Activation energy as a function of gate bias for a simulated nTFET with different diameters. Inset: onset voltage as a function of the diameter.

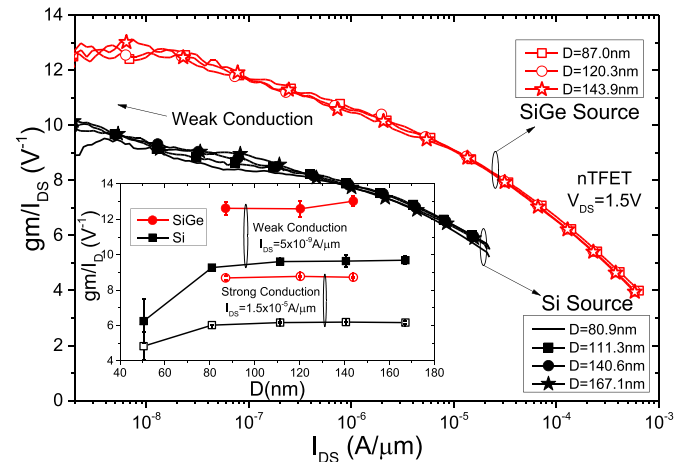


Fig. 6. Experimental efficiency as a function of the normalized drain current for TFETs with different diameters and two source compositions.

almost 300 mV when comparing the largest and the smallest diameter

$$\ln(I_{DS}) = -\left(\frac{E_A}{K \cdot T}\right) + \ln(I_0) \quad (1)$$

where K is the Boltzmann constant, T the temperature in kelvin, and I_0 is the OFF-state drain current.

These small-diameter effects can also be observed when analyzing the analog parameters of the devices. One very important parameter for the analog performance is the transistor efficiency (gm/I_{DS}). The analysis of the efficiency on the experimental devices for both source materials (Fig. 6) pointed out that as the available measured diameters are considerably large, the diameter has almost no influence on the measured efficiency characteristics, for both weak and strong conduction conditions.

Although the diameter has almost no influence on the efficiency, the efficiency for the SiGe source device is higher than for the Si source counterpart, for any conduction regime, due to the lower bandgap energy of the SiGe source, increasing all the conduction mechanisms.

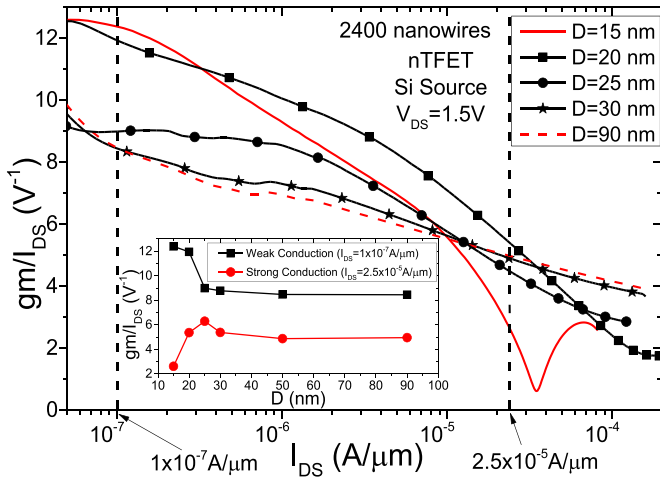


Fig. 7. Simulated efficiency as a function of drain current for Si source TFETs with different diameters.

When using numerical simulations to extrapolate the impact of the reduction of the diameter on the analog characteristics of Si-source vertical nanowire nTFETs, some interesting results can be observed. Comparing the efficiency (Fig. 7), two opposite trends can be observed: one for the weak conduction ($I_{DS} = 1 \times 10^{-7} \text{ A}/\mu\text{m}$) and another for the strong conduction ($I_{DS} = 2.5 \times 10^{-5} \text{ A}/\mu\text{m}$).

In weak conduction, i.e., the condition for which the efficiency reflects the subthreshold swing behavior, the efficiency is higher for small diameter devices. This behavior can be explained by the higher influence of the BTBT on the devices with small diameter, because the current generated by the BTBT leads to a better switching characteristic, which reduces the subthreshold swing, resulting in an improvement of the efficiency.

However, in strong conduction, which has higher values of I_{DS} , the narrower devices have insufficient area to provide an increase of the BTBT mechanism, resulting in a decrease of the efficiency when compared to larger devices that do not have BTBT as the dominant mechanism toward the center of the nanowire.

In order to better understand the diameter effect on the conduction mechanism for different conduction regions, Fig. 8 presents the generation rate as a function of the radial position of the nanowire toward the center.

From Fig. 8, it is possible to observe that for the weak conduction [Fig. 8(a)], the smaller diameter device has BTBT all along the channel/source junction, while the device with a larger diameter has BTBT only near the Si/dielectric interfaces. However, for strong conduction [Fig. 8(b)], the larger diameter device has a more pronounced BTBT in the center of the device, improving the resulting BTBT for this conduction condition.

The results presented in Fig. 8 can also explain the behavior of other analog parameters, as the transconductance (g_m) and the output conductance (g_D) (Fig. 9), both normalized by the diameter. Differently as done in [9], [10], and [12]–[14], in this paper, the same I_{DS} level is used to compare these parameters.

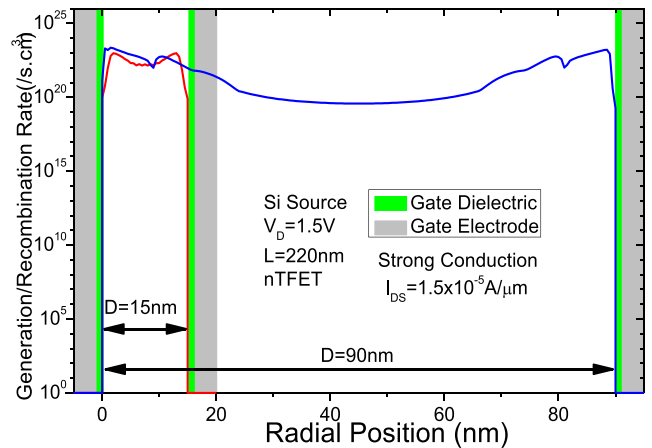
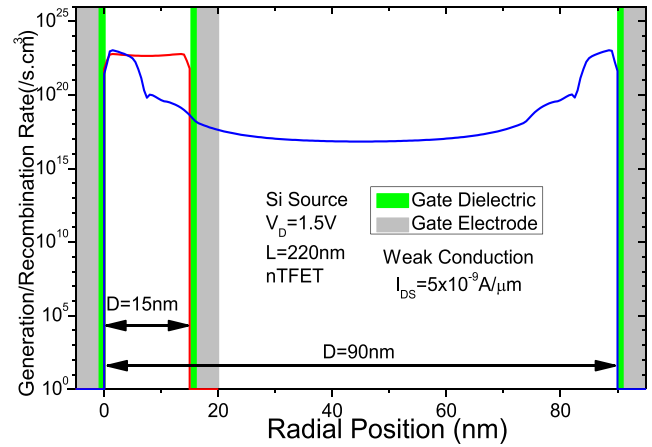


Fig. 8. Simulated generation rate as a function of radial position for Si source NW-TFETs in (a) weak and (b) strong conduction.

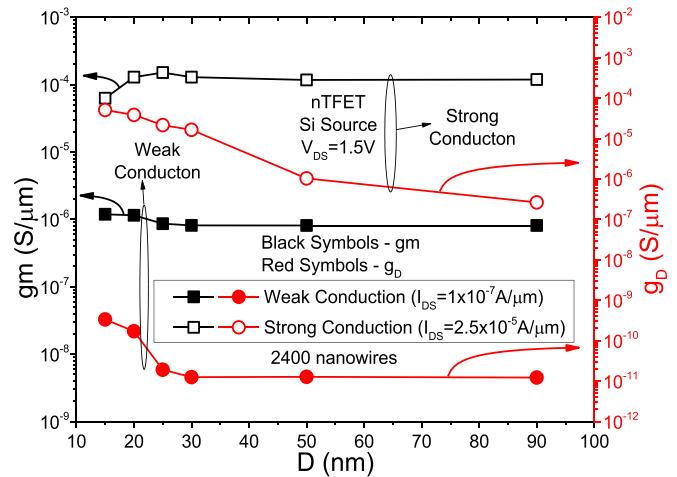


Fig. 9. Simulated normalized transconductance and output conductance as a function of the diameter for both weak and strong conduction.

From Fig. 9, analyzing initially the transconductance, it can be noticed that for the weak conduction regime, as the diameter is strongly reduced, the g_m is increased due to the increase of the gate to channel electrostatic coupling and consequently of the BTBT predominance in the current. For strong conduction, the diameter reduction also improves the g_m , but only until the device is narrow enough to ensure that

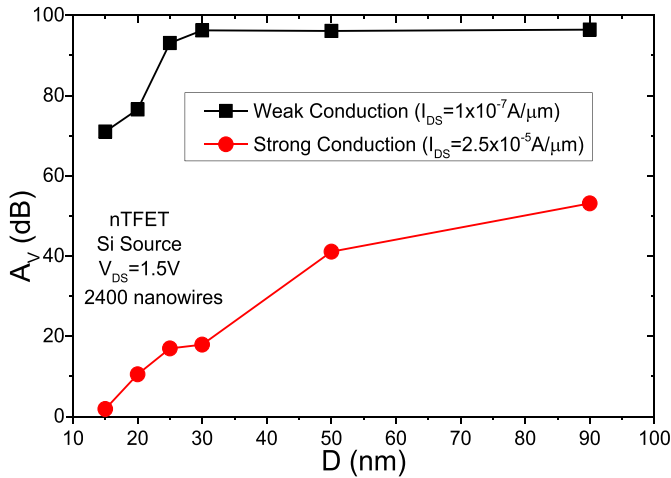


Fig. 10. Simulated intrinsic voltage gain as function of the diameter.

the BTBT dominates along the entire junction. For diameters lower than this point, gm tends to be degraded due to the limitation of the BTBT area.

The BTBT mechanism is more susceptible to the drain bias than TAT due to the BTBT dependence on the total electric field (ξ). This dependence can be studied by the model of the generation rate of the BTBT mechanism (RBTBT) proposed in [22] as shown in

$$R_{\text{BTBT}} = A \cdot \frac{n \cdot p - n_i^2}{(n + n_i)(p + n_i)} \cdot \xi^P \cdot e^{\left(\frac{B \cdot E_g \cdot (T)^{3/2}}{E_g \cdot (300)^{3/2} \cdot \xi}\right)} \quad (2)$$

where n is the electron concentration, p is the hole concentration, n_i is the intrinsic carrier concentration, T is the temperature, E_g is the bandgap, P is the electric field concentration parameter, A is the pre-exponential constant of the model, and B is the exponential constant of the model.

Since the output conductance is strongly influenced by the drain bias, the same analysis of gm is done for g_D . The output conductance has the same behavior for both conduction conditions: the g_D tends to increase (degrade) as the diameter becomes smaller due to the higher influence of the BTBT. Due to the higher influence of BTBT under strong conduction, it starts to degrade for larger diameters, increasing almost 2 orders of magnitude compared with the smallest simulated device.

When considering the influence of the diameter for both conduction conditions on the intrinsic voltage gain (A_V), which is given in (3), an interesting behavior can be noticed (Fig. 10). Under strong conduction, as the g_D is increased more pronounced for a smaller nanowire diameter than the increase of the gm, A_V has very low values and is strongly degraded with reduced diameter

$$A_V = 20 \cdot \log \left(\left| \frac{gm}{g_D} \right| \right). \quad (3)$$

Analyzing the device under weak conduction for large diameters, lowering the diameter has almost no influence on A_V . However, for the smaller diameters, the degradation of the g_D is more pronounced than the increase of the gm, resulting in

a degradation of A_V . At the same time, this degradation for the nanowire TFET in weak conduction is much lower than the one in strong conduction.

IV. CONCLUSION

In this work, the performance of vertical nanowire TFETs is investigated in function of the diameter with a focus on the conduction mechanism and the analog parameters, considering different conduction conditions.

For large diameters, the devices are hardly influenced by the reduction of the diameter. As the diameter becomes smaller, BTBT starts to become the dominant mechanism along the channel/source junction. Furthermore, the onset voltage starts to decrease as well. These two effects together generate an increase in the normalized drain current.

For narrower nanowire TFETs at strong conduction, the current generated by BTBT degrades due to the lower available area for tunneling occurrence. However, for weak conduction, the reduction of the diameter increases the BTBT along the channel/source junction without this degradation.

Concerning the analog parameters, for both conduction conditions, the transconductance is improved for narrow nanowires. However, the output conductance is more degraded, resulting in a degradation of the output conductance with the reduction of the diameter. Furthermore, the degradation at strong conduction is more pronounced than at weak conduction.

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