Multifunctional Control Strategy for Asymmetrical Cascaded H-Bridge Inverter in Microgrid Applications

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***Abstract*—A multifunctional control strategy for a single-phase asymmetrical cascaded H-bridge multilevel inverter (ACHMI), suitable for microgrid systems with nonlinear loads, is presented. The primary advantage of ACHMI is to produce a staircase output voltage with low harmonic content utilizing unequal dc voltages on the individual H-bridge cells. In a grid-connected mode of operation, the control strategy of the ACHMI is based on the conservative power theory, providing selective disturbing current compensation besides injecting its available energy. In autonomous mode of operation, two different control methods along with a damping resistor in the filter circuit are developed for regulation of the ACHMI instantaneous output voltage in a variety of load conditions. The first method is a single-loop voltage control scheme without the need of any current measurement. The second one is a multiloop voltage control scheme with a load current feedforward compensation strategy and preservation of the grid-connected current control scheme. The steady-state response and stability of both voltage control schemes are analyzed, and based on the application requirement, the control schemes are implemented individually. The effectiveness of each control strategy is experimentally verified using a hardware-in-the-loop setup with the control algorithm implemented in the TMSF28335 DSP microcontroller.**

***Index Terms*—Conservative power theory (CPT), distributed generation (DG), microgrid, multilevel inverter, power quality improvement.**

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I. INTRODUCTION

MULTILEVEL inverters are considered as efficient alternatives to high-power applications, presenting a high-quality output voltage, while increasing the efficiency, robustness, and lowering the electromagnetic interference. The well-known topologies of multilevel inverters are: neutral point clamped, flying capacitor, and cascaded H-bridge [1], [2]. This paper focuses on the asymmetrical cascaded H-bridge multilevel inverter (ACHMI) topology fed by unequal dc sources to generate a high-quality output voltage using only a few H-bridge cells. Using unequal dc sources can eliminate redundant output levels, increasing the number of output levels generated by the inverter with the same number of H-bridge cells. Therefore, a high-quality output voltage can be achieved using only a few H-bridge cells, presenting a very low harmonic content [3]. These interfacing converters then can operate either grid following to inject desired current into the grid or grid forming to establish and regulate the load voltage. The main function of such an interfacing system in grid-connected mode is active power provision. However, the interface converters can also be used as multifunctional compensators with the capability of enhancing power quality, rather than being limited to active power generation, especially in conditions where the grid might be weak, such as in rural power systems, or in remote areas [4], [5]. However, the rated capacity of the interfacing converter plays a significant role in this situation. Normally, the injection of full power available from the local power source into the grid is desired. If this power is lower than the converter power rating, the remaining power capability could be used to compensate for power quality disturbances, like harmonic pollution, unbalances, and reactive power. Therefore, some selective compensation strategies could be used, where the compensation level would be directly related to the available interfacing converter capability. For the purpose of harmonic, reactive and unbalanced current compensation, numerous control strategies have been proposed, highlighting the important contributions based on the instantaneous power (PQ) theory [6], synchronous reference frame (DQ) control method [7], and conservative power theory (CPT) [8]. In [7], a synchronous reference frame current control strategy for grid-connected inverters is presented to provide a sinusoidal current into the utility grid, despite the distorted grid

voltage and nonlinear local load conditions. In [8], a CPT-based multitask control strategy for [distributed generation (DG)] inverters is developed. In [9], a single-phase grid-interfaced PV system has been used for improving the voltage quality at the grid-tied nodes for small voltage dips and harmonic mitigation. In [10], grid-interfaced wind generation systems with active harmonic filtering capabilities have been proposed. Compared to the other control strategies, such as PQ theory and the DQ control method, CPT may be considered a novel alternative method to design and control multifunctional DG inverters. CPT is used as an alternative to generating different current references in the stationary frame, for selective disturbances mitigation and if needed, active power provision [11]–[13].

The essential requirement under islanded operating conditions is to control the system voltage parameters such as amplitude and frequency with low total harmonic distortion (THD), fast dynamic response, and zero steady-state error at the output voltages, even under highly distorted and unpredictable load currents. Various control techniques for inverters in standalone mode have been presented in the literature. Digital repetitive control [14] has been proposed to reduce harmonic distortions of the output voltage produced by nonlinear loads, but this approach generally suffers from slow dynamics and has poor performance with nonperiodic disturbances. Deadbeat control [15] has good dynamic performance, but this method exhibits sensitivity to parameter mismatches, model uncertainties, and noises. The proportional resonant control has shown superiority in eliminating the steady-state error associated with the tracking problem of ac signals, [16], but it suffers from several drawbacks, such as sensitivity to small variations in the frequency and possibility of instability margins due to the phase shift introduced by sensed signals [17]. Also, the tuning of multiple resonant frequencies is an inconvenient task. In [18], the output characteristics of a single-phase inverter with the voltage and filter inductor current feedback variables in multiloop scheme are analyzed, and the equivalent circuit model of a parallel single-phase inverter system is introduced. In [19], the multiloop voltage control consists of an outer feedback loop of the capacitor voltage, and an inner feedback loop of the capacitor current is investigated. It is shown that the inner capacitor current feedback loop provides damping of filter resonance with satisfactory steady state and transient performance. However, in this strategy, the inverter output current is not available.

In this paper, the control objective for the grid-connected ACHMI system is to provide simultaneous functionalities based on the CPT for injecting its available energy, compensating selectively the disturbing loads, and enabling a smooth transition between grid-connected and autonomous modes of operation by supplying all current components of the load with zero current injection by the grid. In the autonomous mode of operation, the control objective becomes to regulate the ACHMI output voltage. Two different control methods along with a damping resistor in the filter circuit are developed to regulate the instantaneous output voltage of the ACHMI in a variety load conditions. The first method is a single-loop voltage control scheme without the need of current measurement requiring tuning only one controller with less computational burden, less complexity, and simpler tuning, compared to a conventional

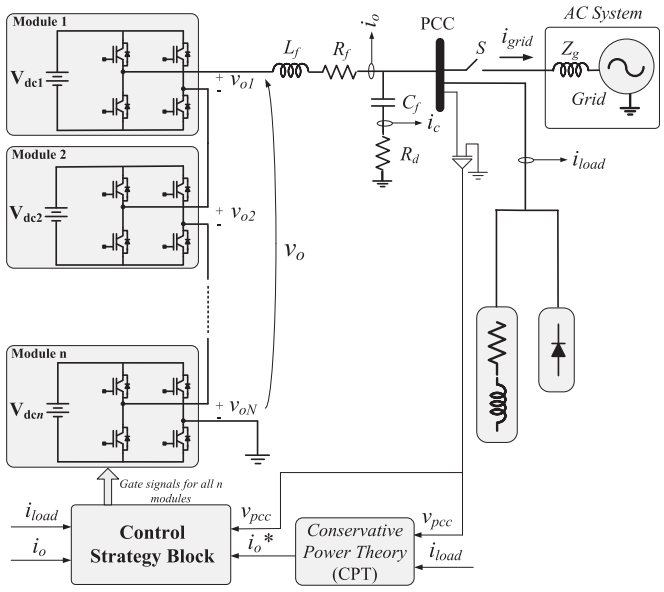

Fig. 1. Considered microgrid with ACHMI.

proportional-integral multiloop controller. The second one is a multiloop voltage control scheme with load current feedforward compensation strategy and preservation of the grid-connected current control scheme. However, the developed multiloop voltage control scheme needs implementation of load current for the feedforward path to mitigate the impact of load on the voltage regulation processes. Based on the required steady-state response and stability margin, one of them can be implemented. Both developed control methods are robust to system uncertainties and guarantee voltage regulation under abrupt load disturbances. This paper is the journal version of our presented work in the 2015 IAS annual meeting [20].

The organization of the paper is as follows: in Section II, a brief review of the considered ACHMI microgrid system and its modulation is presented. Section III presents the CPT formulation for single-phase circuits. Sections IV and V present the derivation of the multifunctional ACHMI control strategy in grid-connected and autonomous modes of the operation. In Section VI, the performance and robustness of the control strategy is experimentally verified through a real-time hardware-in-the-loop (HIL) setup. The CPT decomposition and the digital controllers are programmed in a C compiler and implemented in TMSF28335 digital signal controller. The conclusion of this paper is presented in Section VII.

II. ACHMI Structure and Modulation

The cascaded H-bridge multilevel inverter (CHMI) is structured by a series of cascaded H-bridges, each fed by independent dc sources [2]. Each H-bridge as a power cell is capable of three different voltage levels at the output. The series connection of the H-bridges generates output voltage waveforms that are synthesized by the combination of each output of the H-bridges at certain switching states. The merit of this topology is that the modulation, control, and protection requirements of each bridge cell are modular. Fig. 1 shows a single-phase topology of an ACHMI with separate dc sources connected to the distri-

bution network at the point of common coupling (PCC) via a switch.

An output voltage waveform is obtained by adding the H-bridge cells output voltages as follows:

$$v_o(t) = v_{o,1}(t) + v_{o,2}(t) + \ldots + v_{o,N}(t) = \sum_{k=1}^{N} v_{o,k}(t) \tag{1}$$

where N is the number of H − bridge cells.

If all dc-voltage sources in Fig. 1 were equal to $V_{\rm dc}$, the inverter would be then known as symmetric CHMI. The number of output levels (N_L) in a symmetric CHMI multilevel inverter is related to the number of H-bridges (N) by the following equation:

$$N_L = 1 + 2N. \tag{2}$$

The maximum output voltage $V_{o,\rm MAX}$ is then obtained as

$$V_{o,\rm MAX} = NV_{\rm dc}. \tag{3}$$

To increase the number of output levels generated by the inverter with the same number of H-bridge cells, ACHMI can be used. In [21] and [22], the magnitudes of the dc voltage sources have been usually chosen according to a geometric progression with a factor of two or three, which are called binary and trinary multilevel inverters, respectively. The number of output voltage levels for binary and trinary ACHMI, respectively, is as follows:

$$N_L = 2^{N+1} - 1 \text{ if } V_{{\rm dc},k} = 2^{k-1} V_{\rm dc};\ k = 1, 2, \ldots, N \tag{4}$$

$$N_L = 3^N \text{ if } V_{{\rm dc},k} = 3^{k-1} V_{\rm dc};\ k = 1, 2, \ldots, N. \tag{5}$$

The maximum output voltage of an ACHMI including N H-bridge cells is as follows:

$$V_{o,\rm MAX} = \sum_{k=1}^{N} V_{{\rm dc},k}\ . \tag{6}$$

Equation (6) can be rewritten as (7) and (8), respectively, for binary and trinary dc sources ACHMI

$$V_{o,MAX} = \left(2^N - 1\right) V_{\rm dc} \text{ if } V_{{\rm dc},k} = 2^{k-1} V_{\rm dc};\quad k = 1, 2, \ldots, N \tag{7}$$

$$V_{o,MAX} = \left(\frac{3^N - 1}{2}\right) V_{\rm dc} \text{ if } V_{{\rm dc},k} = 3^{k-1} V_{\rm dc};\quad k = 1, 2, \ldots, N. \tag{8}$$

Therefore, using ACHMI, some switching-state redundancies are avoided, reducing the switching losses, and more output voltage levels and a higher maximum output voltage with the same number of H-bridge cells are generated.

Modulation strategies for CHMI are naturally extended from the traditional two-level switching schemes [23]. Several modulation strategies have been proposed for CHMI to switch cascaded H-bridge cells. According to their switching frequency, they can be mainly divided either as fundamental switching frequency or high switching frequency. In the first approach, the switching losses are lower, but the harmonics in the output voltage waveform appear at lower frequencies. For high power and low dynamic systems, low frequency strategies, such as selective harmonic elimination [24], space vector control [25], and nearest level control [26] are applied. In the second approach, the harmonics are multiples of the switching frequency and their sidebands. High-frequency strategies include space vector modulation [27] and carrier-based pulse-width modulation (PWM) [28]. The carrier-based modulation schemes can be generally classified into two categories: level-shifted (LS-PWM) and phase-shifted (PS-PWM) methods. Both LS-PWM and PS-PWM switching schemes can be applied to the ACHMI. The output voltage harmonic content of PS-PWM technique is higher than the LS-PWM. Therefore, in this paper, the LS-PWM scheme is considered.

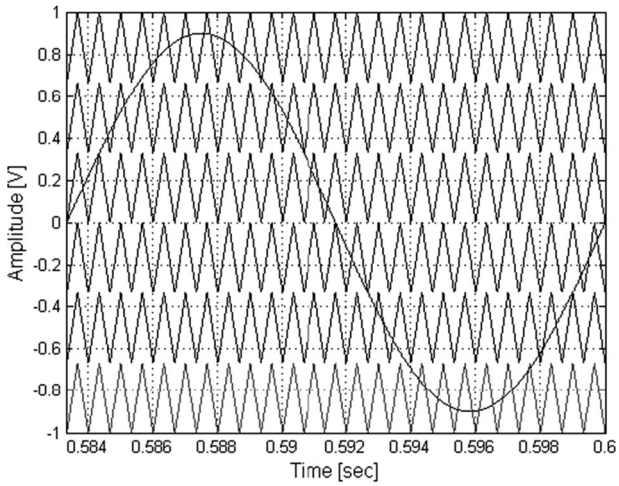

Fig. 2. Reference and carrier signals for a seven-level ACHMI.

The LS-PWM is an extension of the traditional bipolar PWM switching scheme in which a set of triangular carriers is shifted in a vertical position to cater to different voltage levels of the series-connected H-bridge cells. The modulation technique is built up of $N_L - 1$ carrier waves, with N_L number of voltage levels. Each carrier is set between two voltage levels [29]. In the considered LS-PWM, all carrier waves have the same frequency and are arranged on top of each other, with no phase shift, so that together they vary from maximum output voltage to minimum output voltage. In this paper, the ACHMI consists of two modules, with binary dc voltages scaled in the ratio 1:2 synthesizing a seven-level output voltage waveform. The vertical offset of six triangular carriers compared with a sinusoidal reference for the presented seven-level ACMLI is illustrated in Fig. 2. It can be seen that all carriers are adjacent to each other with the same phase.

The parameters of the considered ACHMI system are illustrated in Table I. The load consists of a linear resistive–inductive load plus a nonlinear single-phase full-wave bridge rectifier feeding the capacitive and resistive load. The effect of the DG unit is represented by the dc voltage source. In the grid-connected mode of operation, $v_{\rm pcc}$ is dictated by the grid representing the PCC/load voltage. In the autonomous mode of operation, the static transfer switch is open and the ACHMI

TABLE I
ACHMI PARAMETERS

Parameters	Values
Nominal phase RMS voltage	127 V
Grid frequency, f	60 Hz
Maximum power output of ACHMI	2 kVA
Output filter inductor, L_f	4 mH
Output filter resistor, R_f	0.15 Ω
Output filter capacitor, C_f	20 μF
Damping filter capacitor resistor, R_d	5 Ω
DC link voltages, V_{dc1}	80 V
DC link voltages, V_{dc2}	160 V
Switching frequency, f_s	12 kHz
Sampling Period, T_s	(1/12000) s

solely supplies the load. A damping resistor is employed in the filter circuit to improve the system stability and damp the *LC* resonance under different loading conditions especially for the single-loop voltage control scheme. Since the actual capacitor current is essentially sinusoidal, there will be minimal harmonic circulating around the closed-loop system and, hence, the influence of passive damping is negligible.

III. CONCISE OVERVIEW OF THE CPT—SINGLE PHASE

The CPT [30] allows for the decomposition of the instantaneous currents into different orthogonal current terms, valid for single- and multiphase systems, independent of the voltage conditions. Such current terms are used for generating selective current references, as the CPT decomposition results in several current related terms associated with specific load characteristics. CPT proposes a decomposition of power and current variables in the stationary frame, according to terms directly related to electrical characteristics, such as average power transfer, reactive energy, unbalanced loads, and nonlinearities. Assuming a single-phase circuit under periodic operation, where (v) and (i) are, respectively, the instantaneous voltage and current signals, and $(\hat{v})$ is the unbiased integral of the voltage measured at a given network port, the CPT splits current terms of the load as shown in following.

Active current is defined by

$$i_a = \frac{\langle v, i\rangle}{\|v\|^2}\, v \;=\; G.v \tag{9}$$

where G represents the load equivalent conductance and $\|v\|$ means the voltage's Euclidian norm or RMS value.

Reactive current is given by

$$i_r = \frac{\langle \hat{v}, i\rangle}{\|\hat{v}\|^2}\;\; \hat{v} = \; B.\hat{v} \tag{10}$$

where B represents the load equivalent reactivity.

Void current is the remaining current term, which depends on the voltage and the current distortion

$$i_v = \; i - \; i_a - i_r. \tag{11}$$

By definition, all the terms are orthogonal (decoupled) to each other. Then

$$\|i\|^2 = \|i_a\|^2 \; + \|i_r\|^2 + \|i_v\|^2. \tag{12}$$

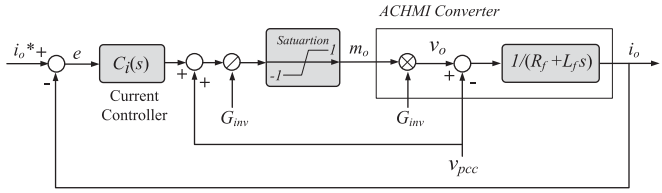

Fig. 3. Block diagram of the current-controlled scheme.

Thus, the apparent power is calculated as

$$A^2 = \|v\|^2 \,.\, \|i\|^2 = P^2 \; + Q^2 + D^2. \tag{13}$$

The active power (P) is related to the average power transfer. The reactive power (Q) is related to the reactive energy, and the void power (D) is the power due to nonlinear behavior of the load and voltage distortion.

IV. ACHMI DYNAMIC MODEL FOR THE GRID-CONNECTED MODE

Fig. 3 presents the block diagram of the current control scheme to regulate ACHMI output current at its reference commands [7]. The proposed current controller is designed based on the frequency response analysis method in a stationary frame with fast dynamic response in tracking reference commands provided by CPT to supply, selectively or not, the load current components.

Consider the ACHMI of Fig. 1 and the block diagram of Fig. 3; the dynamics of the ac-side current $i_o(t)$ are described by (14) and (15). Equation (14) represents a system in which $i_o(t)$ is the state variable, $v_o(t)$ is the control input, and $v_{\mathrm{pcc}}(t)$ is the disturbance input. Based on (15), the control input $v_o(t)$ is proportional to, and can be controlled by, the modulating signal $m_o(t)$ illustrated in Fig. 2. The transfer function and frequency response of the system are determined as in (16). The open-loop current transfer function $G_{\mathrm{oi}}(s)$ is expressed as (17) with $C_i(s)$ the controller of the current control loop, consisting of a lag compensator as (18). Furthermore, the voltage feedforward compensation is employed to mitigate the dynamic couplings between the ACHMI and the ac system, enhancing the disturbance rejection capability of the converter system

$$L_f \frac{di_o\,(t)}{dt} + R_f i_o\,(t) = v_o\,(t) - v_{\mathrm{pcc}}\,(t) \tag{14}$$

$$v_o\,(t) = G_{\mathrm{inv}} \;\; m_o\,(t) = (V_{\mathrm{dc1}} + V_{\mathrm{dc2}}) \;\; m_o\,(t) \tag{15}$$

$$G_{\mathrm{Plant}-i}\,(s) = \frac{i_o\,(s)}{v_o\,(s)} \;= \frac{1}{L_f s + R_f} \tag{16}$$

$$G_{\mathrm{oi}}\,(s) = \frac{C_i\,(s)}{R_f + sL_f} \tag{17}$$

$$C_i\,(s) = \frac{k_c\;(1 + s/\omega_z)}{(1 + s/\omega_p)}\,. \tag{18}$$

For DSP implementation of the control system, the system of (16) is converted from the continuous plane "s" to the discrete plane "z." The z-transformation of the transfer function in s-domain, combined with a zero-order holder, is given by

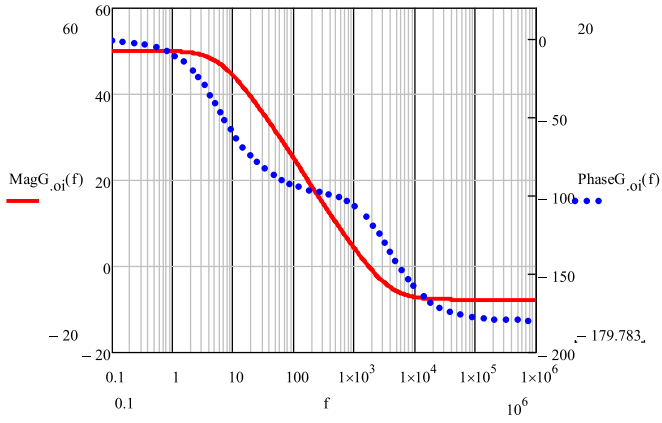

Fig. 4. Bode plot of the open-loop current transfer function.

(19). Transformation is made using the relation $z = e^{s.T_a}$. So, $G_{\mathrm{Plant}-i}(z)$ can be defined as follows:

$$G_{\mathrm{Plant}-i}(z) = Z\left\{\frac{\left(1-e^{-s.T_a}\right)G_{\mathrm{Plant}-i}(s)}{s}\right\} \quad (19)$$

$$G_{\mathrm{Plant}-i}(z) = \left(1-z^{-1}\right)Z\left\{\frac{G_{\mathrm{Plant}-i}(s)}{s}\right\}. \quad (20)$$

To allow the use of the frequency response method design, the conversion of $G_{\mathrm{Plant}-i}(z)$ transfer function from "z" plane to "w" plane is performed using the bilinear transform as shown in

$$z = \frac{1+\frac{T_a}{2}w}{1-\frac{T_a}{2}w} \quad (21)$$

from where we have

$$G_{\mathrm{Plant}-i}(w) = \frac{-0.01042w+250}{w+37.5}. \quad (22)$$

The bandwidth is chosen to be one-seventh of the switching frequency to limit the current loop response to the switching noises. However, it is high enough to achieve a fast dynamic response. For $f_{\mathrm{ci}} = 1.714$ kHz, $\varphi_{\mathrm{PMi}} = 65^\circ$ and $f_z = f_{\mathrm{ci}}/10 = 171.42$ Hz, the rest of parameters in (18) are calculated as $f_p = 140.59$ Hz and $k_c = 47.84$. The frequency response of the open-loop transfer function is illustrated in Fig. 4. At cross-over frequency $f_{\mathrm{ci}} = 1.714$ kHz, the open-loop gain of 0 dB and the phase margin of 65° are obtained.

The output current behavior of ACHMI can be described by (23). It can be seen that the output current only depends on the reference current. In other words, under the feedforward compensation, the converter system is equivalent to an independent current source as viewed by the ac system

$$i_o(s) = \frac{C_i(s)}{L_f s + R_f + C_i(s)}\, i_o^*(s). \quad (23)$$

For digital implementation of the control system in the z-domain, the controller of (18) is discretized by the bilinear transform with a sampling time of T_s that is also the switching period. Therefore, the controller transfer function $C_i(z)$ can

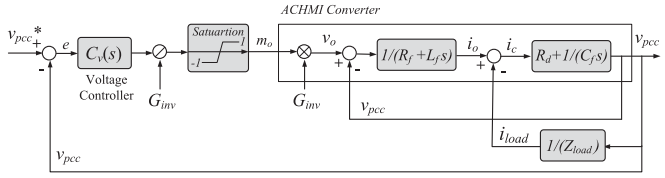

Fig. 5. Block diagram of the single-loop voltage control scheme.

be expressed as

$$C_i(z) = \frac{n_1 z^1 + n_0}{d_1 z^1 + d_0}. \quad (24)$$

The numerator parameters of (24) are calculated as follows:

$$n_1 = \frac{k_c\left(2\omega_p + T_s\omega_z\omega_p\right)}{2\omega_z + T_s\omega_z\omega_p}, \quad n_0 = \frac{k_c\left(-2\omega_p + T_s\omega_z\omega_p\right)}{2\omega_z + T_s\omega_z\omega_p} \quad (25)$$

and the denominator parameters are calculated as

$$d_1 = 1, \quad d_0 = \frac{\left(-2\omega_z + T_s\omega_z\omega_p\right)}{2\omega_z + T_s\omega_z\omega_p}. \quad (26)$$

Having a sampling period, $T_s = (1/12000)$ s, the parameters in the z-domain controller of (24) are calculated as $n_1 = 39.54$, $n_0 = -36.15$, $d_1 = 1$, and $d_0 = -0.928$.

V. ACHMI Inverter Dynamic Model for the Autonomous Mode

For this mode of operation, the control of the ACHMI to regulate the instantaneous load voltage magnitude and frequency is presented. The first method is a single-loop voltage control scheme without the need of any current measurement, and the second one is a multiloop voltage control scheme, taking advantage of the grid-connected current control scheme. The steady-state response and stability of both voltage control schemes are analyzed and based on the required steady-state response and stability margin one of them can be implemented.

A. Single-Loop Voltage Control Scheme

In this section, the proposed ACHMI single-loop voltage control scheme for regulation of instantaneous load voltage without the need of any current measurement is presented. Load voltage regulation is performed only with one control variable with less computational burden, less complexity, and easier tuning.

Fig. 5 illustrates the block diagram of the single-loop control scheme to regulate ACHMI output voltage at its reference commands.

Based on the frequency response method, the dynamics of the ac-side inductor current $i_o(t)$ are described by (27) and the dynamics of the ac-side capacitor current $i_c(t)$ is described by (28). The voltage control design is carried out under no-load conditions. Although it simplifies the analysis, this simplification ensures the stability for all inverter operating conditions. Substituting for inductor current $i_o(t)$ from (27), substituting for capacitor current $i_c(t)$ from (28), and then taking the Laplace transform, (29) is obtained. The transfer function and frequency

response of the system is determined as in (30) in which $v_{\rm pcc}(t)$ is the control output and $v_o(t)$ is the control input. Based on (15), the control input $v_o(t)$ is controlled by the modulating signal $m_o(t)$ in Fig. 2. The open-loop voltage transfer function $G_{\rm ov}(s)$ is expressed as (31) with $C_v(s)$ the controller of the voltage control loop, chosen as expressed in (32), supplying enough phase boost for the desired phase margin achievement. The tracking error from the comparison between the measured output voltage against the desired reference voltage is then passed to $C_v(s)$ in order to generate a modulation command for the LS-PWM modulator

$$L_f \frac{di_o(t)}{dt} + R_f i_o(t) = v_o(t) - v_{\rm pcc}(t) \tag{27}$$

$$C_f \frac{d\left(v_{\rm pcc}(t) - R_d i_c(t)\right)}{dt} = i_c(t) \tag{28}$$

$$i_o(s) = i_c(s) = \frac{v_o(s) - v_{\rm pcc}(s)}{L_f s + R_f} = \frac{C_f s\, v_{\rm pcc}(s)}{(C_f R_d s + 1)} \tag{29}$$

$$G_{{\rm Plant}-v}(s) = \frac{v_{\rm pcc}(s)}{v_o(s)} = \frac{(C_f R_d s + 1)}{L_f C_f s^2 + C_f(R_f + R_d)s + 1} \tag{30}$$

$$G_{\rm ov}(s) = G_{{\rm Plant}-v}(s)\, C_v(s) \tag{31}$$

$$C_v(s) = \frac{k_c}{s}\frac{(1 + s/\omega_z)^2}{(1 + s/\omega_p)^2}. \tag{32}$$

For DSP implementation of the single-loop voltage control scheme, $G_{{\rm plant}-v}(s)$ in (30) is converted from continuous plane "s" to the discrete plane "z" in (33). To allow the use of the frequency response method design, the conversion of $G_{{\rm plant}-v}(z)$ transfer function from "z" plane to "w" plane is performed, using the bilinear transform of (21) with the result shown in (34)

$$G_{{\rm plant}-v}(z) = \left(1 - z^{-1}\right) Z\left\{\frac{G_{{\rm plant}-v}(s)}{s}\right\} \tag{33}$$

$$G_{{\rm plant}-v}(w) = \frac{-0.05281w^2 + 739.4w + 1.267 * 10^7}{w^2 + 1315w + 1.267 * 10^7}. \tag{34}$$

Note that the bandwidth of the voltage controller should be chosen appropriately to achieve a fast dynamic response and to eliminate the low-order voltage harmonics due to the nonlinear loads. Applying the K-factor approach [31], for $f_{\rm cv} = 1.714$ kHz and phase margin of 65° the controller parameters of (32) are obtained as $f_z = 425.5$ Hz, $f_p = 6905.6$ Hz and $k_c = 3391.7$. The frequency response of the open-loop transfer function is illustrated in Fig. 6. At cross-over frequency, $f_{\rm cv} = 1.714$ kHz, the open-loop gain of 0 dB and the phase margin of 65° are obtained.

The output voltage can be described by

$$v_{\rm pcc}(s) = G_{\rm cv}(s)\, v^*_{\rm pcc}(s) - z_o(s)\, i_{\rm load}(s) \tag{35}$$

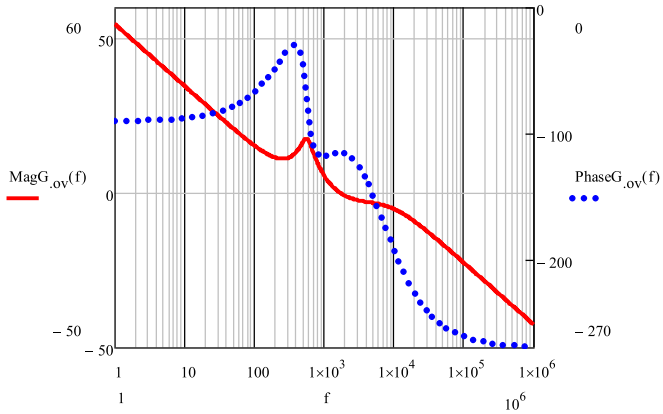

Fig. 6. Bode plot of the open-loop voltage transfer function.

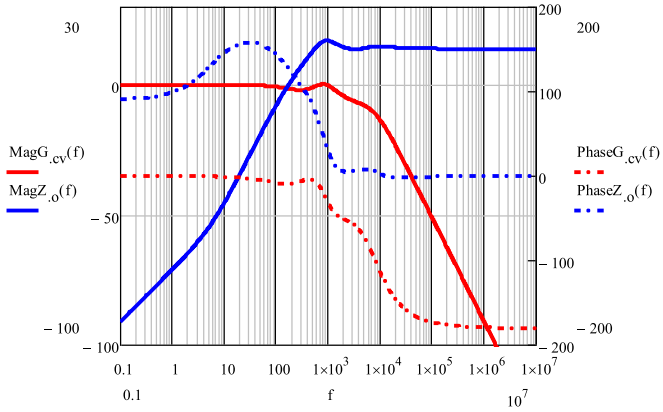

Fig. 7. Bode plot of the closed-loop voltage transfer function $G_{\rm cv}(s)$ and the system output impedance $z_o(s)$ of the single-loop voltage control scheme.

where $G_{\rm cv}(s)$ is the closed-loop voltage transfer function and $z_o(s)$ is the system output impedance

$$G_{\rm cv}(s) = \frac{C_v(s)(C_f R_d s + 1)}{L_f C_f s^2 + C_f(R_f + R_d)s + C_v(s)(C_f R_d s + 1) + 1} \tag{36}$$

$$z_o(s) = \frac{(R_f + L_f s)(C_f R_d s + 1)}{L_f C_f s^2 + C_f(R_f + R_d)s + C_v(s)(C_f R_d s + 1) + 1}. \tag{37}$$

The output voltage should exactly track its reference, while it is desirable to minimize the effect of system output impedance at the fundamental frequency, as well as at other harmonic frequencies to increase the system ability to reject load current disturbances. The steady-state response can be analyzed using the bode diagram of Fig. 7 in which the closed-loop voltage transfer function $G_{\rm cv}(s)$ and the system output impedance $z_o(s)$ is illustrated. At the fundamental frequency $f = 60$ Hz, from the frequency response of the closed-loop voltage loop controller, the gain is -0.282 dB or 0.967 and the phase lag is 5.78° in

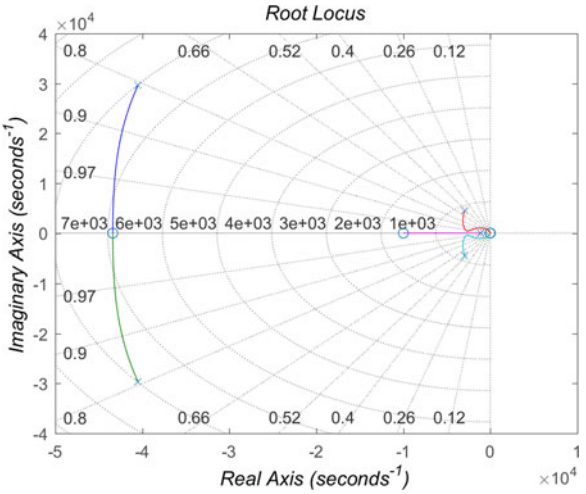

Fig. 8. Root locus of the system output impedance $z_o(s)$ of the single-loop voltage control scheme

response to $v^*_{\rm pcc}(s)$. From the system output impedance, the gain is -15.92 dB or 0.159 in response to the fundamental component of the load current. The effect of system output impedance at other harmonic frequencies of the load current is as follows: namely at $f = 180$ Hz, the gain is 0.675 dB or 1.08, and at $f = 300$ Hz, the gain is 7.06 dB or 2.25, showing the system's ability to reject load current disturbances is decreased.

From (35), the stability of the single-loop voltage control scheme is guaranteed if both the closed-loop transfer function $G_{\rm cv}(s)$ and $z_o(s)$ are stable. The stability of $G_{\rm cv}(s)$ has been guaranteed by proper selection of the controller parameters as previously discussed in Fig. 6. To analyze the stability of $z_o(s)$, the root locus of (37) is plotted as shown in Fig. 8. By examining the roots, we can see the roots are located on left side of the plane implying the characteristic equation of (37) is stable.

The digital implementation of the control system in the z-domain, $C_v(z)$, by discretizing the controller of (32) using the bilinear transform with a sampling time of T_s that is also the switching period, is presented

$$C_v(z) = \frac{n_3 z^3 + n_2 z^2 + n_1 z^1 + n_0}{d_3 z^3 + d_2 z^2 + d_1 z^1 + d_0} \tag{38}$$

where the numerator parameters of (38) are calculated as follows:

$$n_3 = \frac{1/{\omega_z}^2 T_s + 2/\omega_z {T_s}^2 + {T_s}^3}{b} \tag{39}$$

$n_2 = \frac{-(2/{\omega_z}^2 T_s + 2/\omega_z {T_s}^2)}{b}$, $n_1 = \frac{1/{\omega_z}^2 T_s}{b}$ and $n_0 = 0$.

and the denominator parameters are calculated as

$$d_3 = 1,\ d_2 = \frac{-\left({T_s}^2/k_c + 2hT_s + 3/(k_c {\omega_p}^2)\right)}{b}$$
$$d_1 = \frac{hT_s + 3/(k_c {\omega_p}^2)}{b},\ d_0 = \frac{-1/(k_c {\omega_p}^2)}{b}. \tag{40}$$

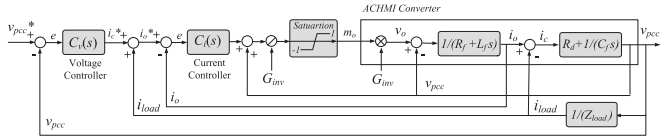

Fig. 9. Block diagram of the multiloop voltage control scheme based on load current feedforward.

The parameters b and h in (39) and (40) are calculated as follows:

$$b = {T_s}^2/k_c + hT_s + 1/\left(k_c {\omega_p}^2\right)$$
$$h = \frac{2\omega_p\omega_z - {\omega_z}^2 + k_c\left(\omega_p - \omega_z\right)}{{\omega_p}^2 k_c \omega_z}. \tag{41}$$

Having sampling period, $T_s = (1/12000)$ s, the parameters in the z-domain controller of (38) are calculated as $n_3 = 4.383$, $n_2 = -7.169$, $n_1 = 2.931$ and $n_0 = 0$, $d_3 = 1$, $d_2 = -1.524$, $d_1 = 0.563$ and $d_0 = -0.039$.

B. Multiloop Voltage Control Scheme

The proposed ACHMI multiloop voltage control scheme with inductor current feedback and load current feedforward is presented in this section and shown in Fig. 9. Load current feedforward compensation strategy mitigates the impact of load current on the voltage regulation process. Thus, the compensated system enables it to perform under a wide range of load conditions. Applying the filter inductor current as inner feedback variable, the inverter current is now measured directly; thus, the grid-connected control scheme is preserved as the inverter operated in both modes of operation. The control scheme consists of an inner current loop and outer voltage loop, implemented to achieve low steady-state error and fast transient response with sufficient stability margin. The outer voltage loop is used to ensure steady-state reference tracking performance and the inner loop provides fast dynamic compensation for system disturbances, such as rapid reference or load changes. Once the inner loop current controller is set, the next step is to tune the controller of the voltage feedback loop. The same for the single-loop voltage control scheme, the voltage control design is carried out under no-load conditions. Later, the steady-state response is analyzed under the load conditions at the fundamental frequency, as well as at other harmonic frequencies.

From Fig. 9, $v_{\rm pcc}(s)$ is controlled by $i^*_c(s)$ where $i^*_c(s)$ is the output of the voltage controller. Substituting for $i^*_o(s)$ (inductor reference current) from (43) in (42), (44) is obtained. Note that (43) is obtained from (23) in which $i_o(s)$, the output current behavior of the ACHMI, is described. Taking the Laplace transform of the dynamics of the ac-side capacitor current $i_c(t)$ in (28), and then, substituting for $i_c(s)$ in (45), (46) is acquired. Substituting for $i_o(s)$ (inverter ouput current) from (46) in (44), (47) is obtained. Equation (48) indicates the system transfer function between $v_{\rm pcc}(s)$ and $i^*_c(s)$ based on the frequency response analysis method in which $v_{\rm pcc}(s)$ is the control output and $i^*_c(s)$ is the control input. Based on (48), $v_{\rm pcc}(s)$ can be regulated independently by $i^*_c(s)$. The open-loop voltage

transfer function $G_{\rm ov}(s)$ is expressed as (49) with $C_v(s)$, the controller of the voltage control loop. Satisfactory performance can be achieved with less implementation complexity using a PI compensator, as indicated in (50), with fast dynamic response in tracking the reference command, where the parameters of k_p and T are, respectively, the proportional and time constant of the compensator

$$i_o^*(s) = i_c^*(s) \tag{42}$$

$$i_o^*(s) = \frac{L_f s + R_f + C_i(s)}{C_i(s)}\, i_o(s) \tag{43}$$

$$i_o(s) = \frac{C_i(s)}{L_f s + R_f + C_i(s)}\, i_c^*(s) \tag{44}$$

$$i_o(s) = i_c(s) \tag{45}$$

$$i_o(s) = \frac{C_f\ s\ v_{\rm pcc}(s)}{(C_f R_d s + 1)} \tag{46}$$

$$\frac{C_f\ s\ v_{\rm pcc}(s)}{(C_f R_d s + 1)} = \frac{C_i(s)}{L_f s + R_f + C_i(s)}\, i_c^*(s) \tag{47}$$

$$G_{{\rm Plant}-v}(s) = \frac{v_{\rm pcc}(s)}{i_c^*(s)} = \frac{C_i(s)\,(C_f R_d s + 1)}{C_f\ s\ (L_f s + R_f + C_i(s))} \tag{48}$$

$$G_{\rm ov}(s) = G_{{\rm Plant}-v}(s)\, C_v(s) \tag{49}$$

$$C_v(s) = k_p \left(\frac{sT+1}{sT}\right). \tag{50}$$

For DSP implementation of the cascaded voltage control scheme, the functions of continuous plane "s" is converted to the discrete plane "z." The Plant transfer function in z-domain is obtained by means of the z-transformation in (51). To allow the use of the frequency response method design, the conversion of $G_{{\rm plant}-v}(z)$ transfer function from "z" plane to "w" plane is performed, using the bilinear transform of (21) with the result shown in (52)

$$G_{{\rm plant}-v}(z) = \frac{C_i(z) * \left(1 - z^{-1}\right) Z\left\{\frac{\frac{(C_f R_d s+1)}{C_f\ s\,(L_f s + R_f)}}{s}\right\}}{\left(1 + C_i(z) * G_{{\rm Plant}-i}(z)\right)} \tag{51}$$

$$G_{{\rm plant}-v}(w) = \frac{\begin{array}{c}-3.458w^5 + 4.151 * 10^4 w^4 + 9.229 * 10^8 w^3 \\ +1.707 * 10^{12} w^2 + 8.521 * 10^{14} w + 2.96 * 10^{16}\end{array}}{\begin{array}{c}w^5 + 1.833 * 10^4 w^4 + 3.399 * 10^7 w^3 \\ +1.709 * 10^{10} w^2 + 5.939 * 10^{11} w + 2.668 * 10^5\end{array}}. \tag{52}$$

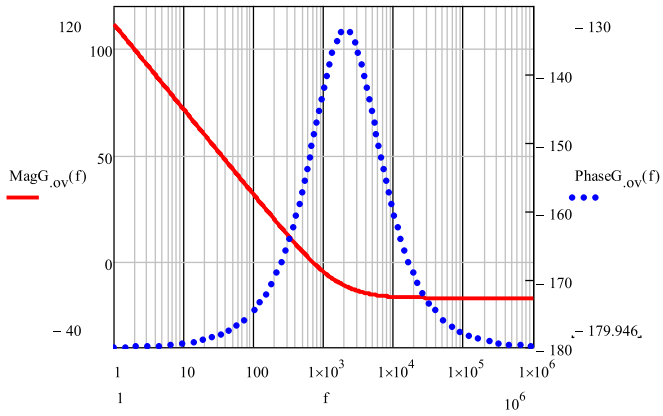

Fig. 10. Bode plot of the open-loop voltage transfer function.

The choice of system bandwidth is a compromise between the transient response and the disturbance rejection requirements. In practice, a value in the range of ten times, the fundamental frequency and one-tenth of the switching frequency may be chosen to get both fast dynamics and switching noise immunity. A good approximation is to consider $f_{\rm cv}$ between one-second and one-third of current loop crossover frequency. For $f_{\rm cv} =$ 700 Hz and phase margin $\varphi_{\rm PMv}$ of 30°, we can then calculate that $T = 0.139$ ms and $k_p = 0.042$. The frequency response of the open-loop voltage control system is illustrated in Fig. 10. It can be seen that at the cross-over frequency $f_{\rm cv} = 700$ Hz, the open-loop gain of 0 dB and the phase margin of 30° are obtained.

The output voltage can be shown to be given by

$$v_{\rm pcc}(s) = G_{\rm cv}(s)\, v_{\rm pcc}^*(s) - z_o(s)\, i_{\rm load}(s) \tag{53}$$

where $G_{\rm cv}(s)$ is the closed-loop voltage transfer function and $z_o(s)$ is the system output impedance, see (54) and (55) as shown at the bottom of the page.

The output voltage should follow its reference, while it is desired to minimize the effect of system output impedance at the fundamental and at other harmonic frequencies to increase the system ability to reject load current disturbances. The steady-state response is analyzed using the bode diagram of Fig. 11 in which the closed-loop voltage transfer function $G_{\rm cv}(s)$ and the system output impedance $z_o(s)$ are illustrated. At the fundamental frequency $f = 60$ Hz, from the frequency response of the voltage closed-loop voltage controller, the gain is 0.081 dB or 1.009 and the phase lag is 0.03° in response to $v_{\rm pcc}^*(s)$. From the system output impedance, the gain is -27.78 dB or 0.04 in response to the fundamental component of the load current. The effect of system output impedance at other harmonic frequencies of the load current is as follows: namely at $f = 180$ Hz,

$$G_{\rm cv}(s) = \frac{C_v(s)\, C_i(s)\,(C_f R_d s + 1)}{L_f C_f s^2 + C_f(R_f)\, s + C_f C_i(s)\ s + C_v(s)\, C_i(s)\ (C_f R_d s + 1)} \tag{54}$$

$$z_o(s) = \frac{(R_f + L_f s)\,(C_f R_d s + 1)}{L_f C_f s^2 + C_f(R_f)\, s + C_f C_i(s)\ s + C_v(s)\, C_i(s)\ (C_f R_d s + 1)} \tag{55}$$

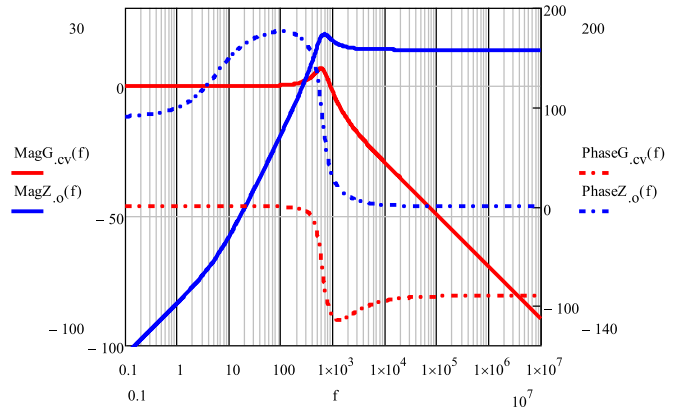

Fig. 11. Bode plot of the closed-loop voltage transfer function $G_{\rm cv}(s)$ and the system output impedance $z_o(s)$ of the multiloop voltage control scheme with load current feedforward.

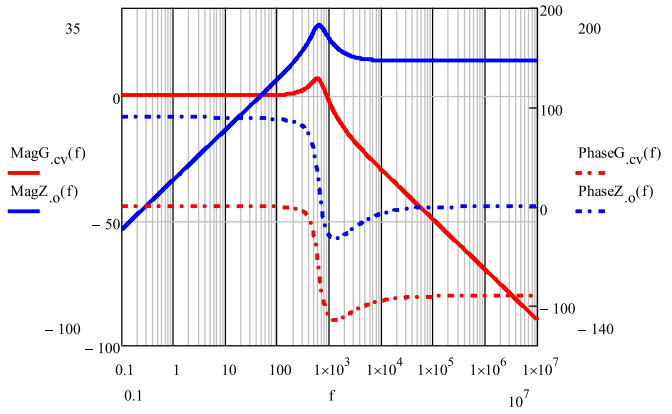

Fig. 12. Bode plot of the closed-loop voltage transfer function $G_{\rm cv}(s)$ and the system output impedance $z_o(s)$ of the multiloop voltage control scheme without load current feedforward.

the gain is -7.41 dB or 0.425, and at $f = 300$ Hz, the gain is 3 dB or 1.41, showing the system ability to reject load current disturbances is improved compared with the single-loop voltage control scheme. Note that in the single-loop voltage control scheme, there is a phase lag of 5.78° in response to $v^*_{\rm pcc}(s)$, which may cause the ACHMI to import some transient power when connecting to the grid. This phase lag is reduced to 0.03° in the multiloop voltage control scheme resulting in a better transient performance.

For the purpose of comparison, in the following section, the steady-state response of the multiloop voltage control scheme without implementing the load current feedforward path is also analyzed. The output voltage can be described as (53), however, $G_{\rm cv}(s)$, the voltage closed-loop voltage transfer function and $z_o(s)$, the system output impedance, are obtained as (56) and (57), shown at the bottom of the page.

From (54)–(57), it is shown that disconnecting the load current feedforward path in the control process does not change $G_{\rm cv}(s)$, while it changes $z_o(s)$ in (57) by adding the term $[C_i(s)(C_f R_d s + 1)]$ to its numerator. The steady-state response can be analyzed using the bode diagram of Fig. 12 in which the closed-loop voltage transfer function $G_{\rm cv}(s)$ and the system output impedance $z_o(s)$ without implementation of the load current feedforward path is illustrated. As $G_{\rm cv}(s)$ does not change, the frequency response of the closed-loop voltage loop controller in response to $v^*_{\rm pcc}(s)$ remains unchanged showing the same performance is obtained for the closed-loop voltage transfer function. However, from the frequency response of the system output impedance to the fundamental component of the load current, $f = 60$ Hz, the gain of 1.98 dB or 1.25 is obtained, showing the fundamental load current component is amplified. The effect of system output impedance at other load current harmonic frequencies is also amplified, namely at $f = 180$ Hz, the gain is 12.06 dB or 4.01, and at $f = 300$ Hz, the gain is 17.74 dB or 7.71, showing the system is amplifying load current harmonics and deteriorating the output voltage. Therefore, a load current feedforward compensation strategy is required to mitigate the impact of load current on the voltage regulation processes enabling the compensated system to perform under a wide range of load conditions.

From (53), the stability of the multiloop voltage control scheme is guaranteed if both the closed-loop transfer function $G_{\rm cv}(s)$ and $z_o(s)$ are stable. To analyze the effect of the feedforward path on the stability of the multiloop voltage control scheme, only the stability of $z_o(s)$ is analyzed. The stability of $G_{\rm cv}(s)$ has been guaranteed by proper selection of the controller parameters as previously discussed in Fig. 10 and does not change with or without the load current feedforward path as it is shown in (54) and (56). To analyze the stability of $z_o(s)$, the root locus of (55) and (57) are plotted in Figs. 13 and 14, respectively. By examining the roots in Figs. 13 and 14, we can see that the implementation of the load current feedforward pushes the dominant roots toward to the right, and hence, stability is reduced. However, the roots in both Figs. 13 and 14 are located on left side of the plane implying the characteristic equations of (55) and (57) are stable. Therefore, feeding a load current in the feedforward path has two effects: one is to enable the compensated system to mitigate the impact of load current on the voltage regulation, and the other one is the positive feedback control effect which essentially degrades the stability of the system. For that, the voltage controller should be designed properly to keep the dynamic performance of the control strategy stable.

$$G_{\rm cv}(s) = \frac{C_v(s)\,C_i(s)\,(C_f R_d s + 1)}{L_f C_f s^2 + C_f(R_f)\,s + C_f C_i(s)\;s + C_v(s)\,C_i(s)\;(C_f R_d s + 1)} \tag{56}$$

$$z_o(s) = \frac{(R_f + L_f s + C_i(s))\,(C_f R_d s + 1)}{L_f C_f s^2 + C_f(R_f)\,s + C_f C_i(s)\;s + C_v(s)\,C_i(s)\;(C_f R_d s + 1)} \tag{57}$$

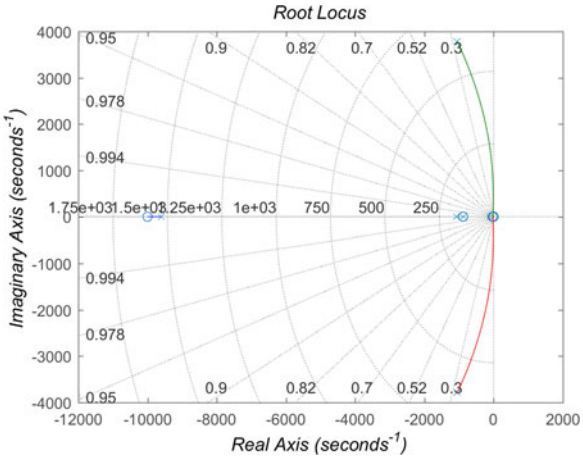

Fig. 13. Root locus of the system output impedance $z_o(s)$ of the multiloop voltage control scheme with load current feedforward.

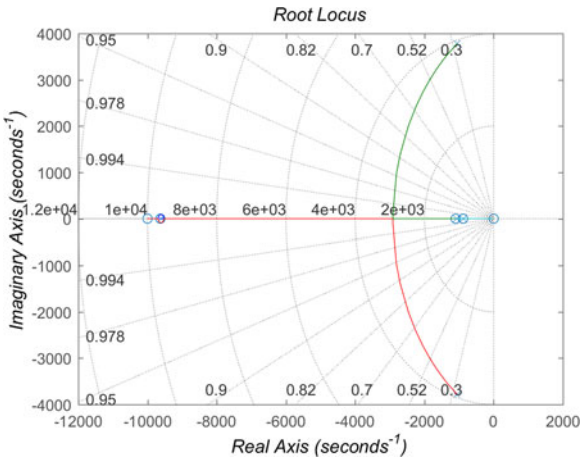

Fig. 14. Root locus of the system output impedance $z_o(s)$ of the multiloop voltage control scheme without load current feedforward.

The digital implementation of the PI voltage controller (50) in the z-domain, $C_v(z)$, is achieved using the bilinear transform as in (58) with a sampling time of T_s that is also the switching period, where the numerator and denominator parameters of (58) are calculated as (59)

$$C_v(z) = \frac{n_1 z^1 + n_0}{d_1 z^1 + d_0} \tag{58}$$

$$n_1 = \left(\frac{k_p}{2T}\right) T_s + k_p, \quad n_0 = \left(\frac{k_p}{2T}\right) T_s - k_p,$$
$$d_1 = 1, \quad d_0 = -1. \tag{59}$$

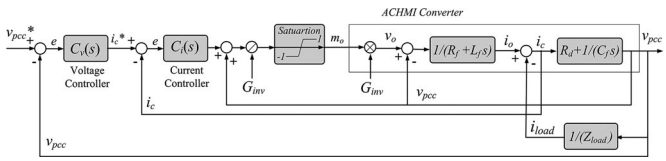

Fig. 15. Block diagram of the multiloop voltage control scheme based on filter capacitor current feedback.

Having sampling period, $T_s = (1/12000)$ s, the parameters in the z-domain controller of (58) are calculated as $n_1 = 0.054$, $n_0 = -0.029$, $d_1 = 1$, and $d_0 = -1$.

In the following section, a comparison between the developed multiloop voltage control scheme with inductor current feedback and load current feedforward and the conventional multiloop voltage control scheme with inner capacitor current feedback loop is presented. The cascaded control with capacitor current feedback control loop for ACHMI is shown in Fig. 15.

This control scheme only needs a low cost sensor for capacitor current measurement, limiting capacitor current as the inner feedback variable. The output voltage is shown as follows:

$$v_{\rm pcc}(s) = G_{\rm cv}(s)\, v^*_{\rm pcc}(s) - z_o(s)\, i_{\rm load}(s) \tag{60}$$

where $G_{\rm cv}(s)$ is the closed-loop voltage transfer function and $z_o(s)$ is the system output impedance, see (61) and (62) as shown at the bottom of the page.

From (54), (55), (61), and (62), it is noted that the same $G_{\rm cv}(s)$ and $z_o(s)$ is achieved for both voltage control strategies, meaning that the load current feedforward compensation scheme of Fig. 9 has an equivalent structure as the filter capacitor current feedback of Fig. 15 so that similar voltage control performance is expected [32]. Note that since the inverter output current is not available, the inner capacitor current feedback loop strategy cannot cooperate in the grid-connected mode of operation.

VI. Experimental Results With Case Studies

To confirm the validity of the proposed control strategy, a single-phase ACHMI setup is experimentally verified using a real time HIL system. The power plant was built inside MATLAB\Simulink. Then, the system was compiled inside the real-time simulator "Opal-RT." The control algorithm was implemented in a TMSF28335 floating point digital signal controller from Texas Instruments.

A. Selective Injection of the Load Current Components in the Grid-Connected Mode of Operation

Figs. 16 and 17 present the waveforms of voltages and currents measured at the PCC for the grid-connected ACHMI. Note

$$G_{\rm cv}(s) = \frac{C_v(s)\, C_i(s)\, (C_f R_d s + 1)}{L_f C_f s^2 + C_f (R_f)\, s + C_f C_i(s)\ s + C_v(s)\, C_i(s)\ (C_f R_d s + 1)} \tag{61}$$

$$z_o(s) = \frac{(R_f + L_f s)\, (C_f R_d s + 1)}{L_f C_f s^2 + C_f (R_f)\, s + C_f C_i(s)\ s + C_v(s)\, C_i(s)\ (C_f R_d s + 1)} \tag{62}$$

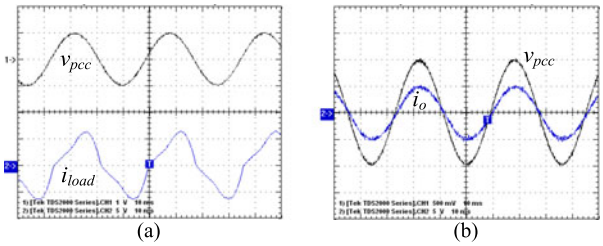

Fig. 16. (a) PCC voltage and load current and (b) PCC voltage and ACHMI current with active current injection.

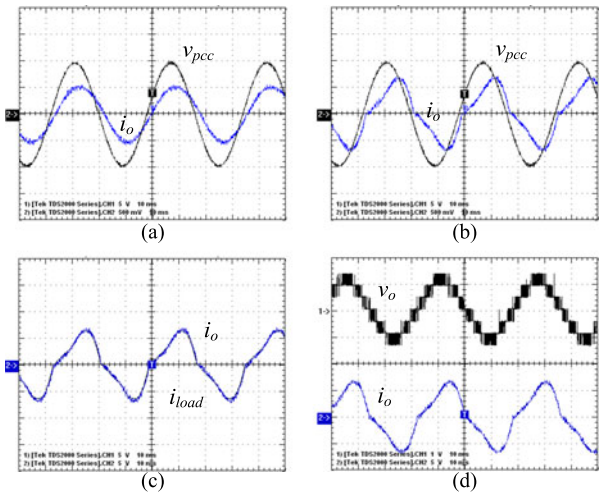

Fig. 17. (a) PCC voltage and ACHMI current with active and reactive current injection, (b) PCC voltage and ACHMI current with entire load current injection, (c) Response of the current controller to load current as reference, and (d) ACHMI terminal voltage and current with load current injection.

that the voltage waveforms are scaled down by the gain (1/180) inside the HIL setup and sent out as analog output along with current waveforms to be measured by the oscilloscope. Fig. 16(a) presents the PCC voltage and load current waveforms under a linear resistive–inductive load plus a nonlinear single-phase full-wave bridge rectifier feeding capacitive and resistive load, before implementing any compensation strategy. Note that the load current is significantly distorted, presenting a THD of 30%. The next sections present the waveforms for some of the more illustrative injection strategies. Note that the current circulating in the ACHMI differs in each strategy.

Fig. 16(b) presents the PCC voltage and the ACHMI current waveforms while ACHMI supply is set to supply the active current component of the load, ($i_{\rm ref} = i_a$). The injected current is sinusoidal and in phase with the PCC voltage, such as in the case of an equivalent balanced resistive load. This indicates the absence of reactive power and nonlinearities. It also confirms the selectivity (and decoupling) of the injection strategies due to the orthogonality between the current components of the CPT decomposition. Note that the grid is responsible for supplying the undesirable characteristics of the load current (reactive and harmonics), that is ($i_{\rm grid} = i_{\rm load} - i_a = i_r + i_v$).

In Fig. 17(a)–(d), the ACHMI also operates as an active filter compensating the current components associated with the disturbances generated by the load (nonactive currents). Fig. 17(a) shows that the ACHMI task is changed for supplying both active and reactive current components of the load, that is ($i_{\rm ref} = i_a + i_r$). This means that the ACHMI is set to attenuate the reactive power, thus its current is no longer in phase with the voltages. In other words, injecting the load reactive power component aims to compensate for the lag between the grid voltage and current waveforms to obtain a unit power factor. In this strategy, the grid supplies the load nonlinearity related disturbance, that is ($i_{\rm grid} = i_v$).

In Fig. 17(b), the ACHMI is set to supply all current components of the load current, including the void current component that is ($i_{\rm ref} = i_{\rm load}$). Using this strategy, the ACHMI consumes its maximum available rating to meet the load demand while zero current is injected by the grid, ($i_{\rm grid} = 0$), ensuring a power balance between the ACHMI and load. If this condition is not fulfilled, a load shedding policy is needed before switching to the autonomous mode to avoid a power imbalance or under-generation situation, and as a result, a smooth transition is obtained [33].

Fig. 17(c) shows the response of the ACHMI current controller while it supplies the entire load current. We can see that the current controller follows its reference precisely. In Fig. 17(d), the ACHMI terminal voltage (v_o) and the inverter current before inverter transfer from the grid-connected to islanded mode is depicted. The ACHMI terminal synthesizes a seven-level output voltage with module voltages scaled in the ratio 1:2. As can be seen from Figs. 16 and 17, the ACHMI tasks become very flexible due to the possibility of being performed selectively. The task of ACHMI in the islanded mode of operation is to regulate the load voltage/frequency.

B. Regulation of the Load Voltage in Autonomous Mode of Operation Based on Single-Loop Voltage Control Scheme

Fig. 18 presents the waveforms of the load voltage and current of islanded ACHMI using the single-loop voltage control scheme. First, the steady-state performance of the ACHMI under linear and nonlinear load is evaluated. In bode plot of Fig. 7, the steady-state response of the controller was analyzed and it is shown that at $f = 60$ Hz, $G_{\rm cv}(s)$ has the gain of 0.967 and the phase of -5.78° in response to $v^*_{\rm pcc}(s)$, and $z_o(s)$ gain in this frequency is 0.159 in response to the fundamental component of the load current. The gain of system output impedance at $f = 180$ Hz is 1.08, and at $f = 300$ Hz is 2.25, showing the system ability to reject load current disturbances is decreased. The voltage waveform and its corresponding reference are shown in Fig. 18(a). The performance is great despite the nonlinear load current, where good voltage regulation with a low steady-state error in tracking its reference voltage based on a Type 3 controller is achieved. Using ACHMI to synthesize a seven-level voltage waveform also helped to produce a better quality output voltage with reduced harmonic content. The output voltage and load current are shown in Fig. 18(b) with minimal harmonic distortion indicating that voltage controller can eliminate the low-order voltage harmonics, stemming from the nonlinear loads with the merit of tuning only one controller.

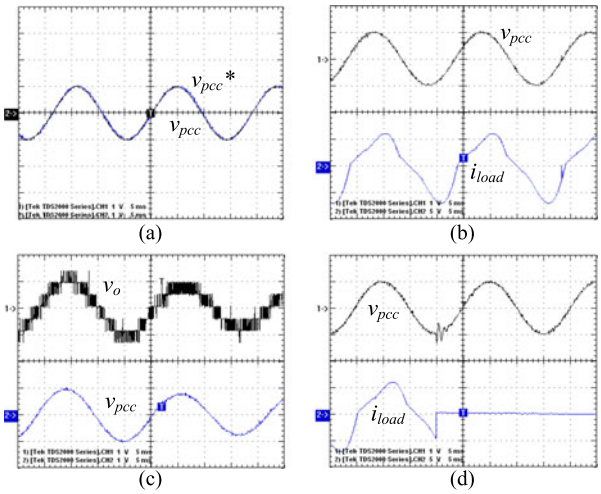

Fig. 18. (a) ACHMI output voltage tracking its reference based on a Type 3 controller, (b) PCC voltage and load current in continuous operation, (c) PCC and terminal voltage of the ACHMI when the reference voltage reduces to 140 V, the number of voltage levels reduces to five-level, and (d) Dynamic response of the voltage-controlled ACHMI to sudden changes in the load.

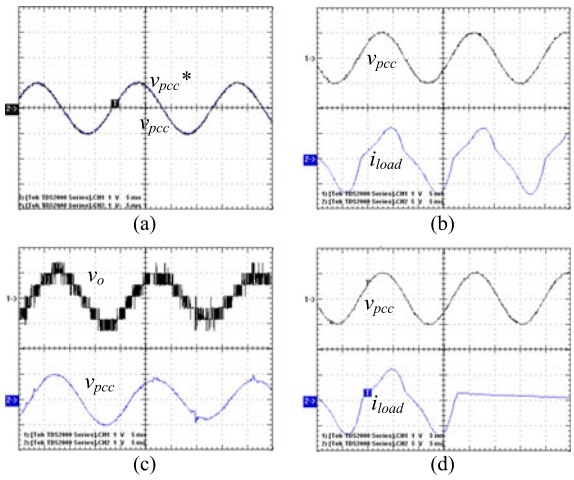

Fig. 19. (a) ACHMI output voltage tracking its reference based on the multiloop scheme, (b) PCC voltage and load current in continuous operation, (c) PCC and terminal voltage of the ACHMI when the reference voltage reduces to 140 V, the number of output voltage levels reduces to five-levels, and (d) Dynamic response of the voltage-controlled ACHMI to sudden changes in the load.

Fig. 18(c) shows the voltage waveform at the PCC and the terminal voltage of the ACHMI (v_o). The ACHMI terminal voltage has the maximum seven levels. In Fig. 18(c), the reference voltage reduces to 140 V. This step in the reference was made only to verify the efficacy and fast dynamic response of the voltage controller. In real microgrids, such a step is not applicable. The levels of ACHMI terminal voltage reduces to five levels, because the carrier waves are modulated with aspect of the voltage magnitude for each respective voltage level meaning each carrier wave is connected to a specific output voltage level. So, when the reference voltage reduces to 140 V, the highest and lowest carriers are not modulated any more.

Fig. 18(d) illustrates the transient performance of the ACHMI voltage controller in response to a load step from nominal load to the no-load is investigated. The voltage regulator dynamic is very fast. The output voltage undergoes very little variation during the transient time. The damping resistor in series with the filter capacitor damps the *LC* resonance even under no-loads and therefore enables an increase in the system bandwidth and avoids instability problems. Fig. 18 depicts that the proposed control strategy is not only simple, but also robust to system uncertainties and sudden load disturbances.

C. Regulation of the Load Voltage in Autonomous Mode of Operation Based on Multiloop Voltage Control Scheme

Fig. 19 demonstrates the voltage and current waveforms of the islanded ACHMI using the multiloop voltage control scheme. The steady-state response of the multiloop voltage control scheme was analyzed in bode plot of Fig. 11, and it is shown that at $f = 60$ Hz, $G_{\rm cv}(s)$ has the gain of 1.009 and the phase of -0.03° in response to $v^*_{\rm pcc}(s)$, and $z_o(s)$ gain in this frequency is 0.04 in response to the fundamental component of the load current. The gain of system output impedance at $f = 180$ Hz is 0.425, and at $f = 300$ Hz is 1.41, showing the system ability to reject load current disturbances is improved compared with the single-loop voltage control scheme.

Fig. 19(a) presents the regulated output voltage waveform tracking its corresponding reference with successful elimination of the steady-state error based on the multiloop voltage control scheme. Note that in the single-loop voltage control scheme there is a phase lag of 5.78° in response to $v^*_{\rm pcc}(s)$, which may cause the ACHMI to import some transient power when connecting to the grid. This phase lag is reduced to 0.03° in the multiloop voltage control scheme resulting in a better transient performance.

Fig. 19(b) presents the steady-state performance of the regulated ACHMI voltage and load current. The performance is excellent irrespective of the load current, with minimal harmonic distortion. The control scheme consists of an inner current loop and outer voltage loop, requiring just a simple PI controller.

Fig. 19(c) shows the voltage waveform at the PCC and the terminal voltage of the ACHMI when the reference voltage reduces to 140 V. Also, the number of terminal voltage levels reduces to five levels as the carrier waves are modulated with aspect of the voltage magnitude.

Fig. 19(d) illustrates the transient performance of the ACHMI voltage controller in response to an unexpected and abrupt load switching. The load is switched OFF and, thereafter, the operating system stays under the no-load circumstances. The output voltage shows no variations during the transient time. The current loop provides fast dynamic compensation for system disturbances, including rapid reference or load changes, improving stability of the controller.

VII. Conclusion

This paper proposes a multifunctional control strategy applicable to ACHMIs with simultaneous functionalities suitable for microgrid systems with nonlinear loads; hence, a wide applicable scope is yielded. The control schemes were analyzed

based on the frequency response method, and digital characterizations of the controllers in the z-domain for DSP implementation were presented. The controller performance was satisfactory for tracking the reference commands provided by CPT, in order to supply, selectively or not, the load current components. The control strategies do not use any kind of reference-frame transformation and they can be applied without any additional consideration. Regulation of load voltage in autonomous mode, based on two different voltage control schemes, was proposed. Based on the required steady-state response and stability margin, one of the proposed control schemes can then be implemented.

Considering the closed-loop voltage transfer function and the system output impedance in each control strategy, it is shown that the multiloop voltage control scheme with load current feedforward has better ability to mitigate the impact of load current on voltage regulation, while due to positive feedback control, the stability of the system degrades. Therefore, the voltage controller should be designed properly to keep the dynamic performance of the control strategy stable. Regarding the single-loop voltage control scheme, lower mitigation of the load current on the voltage regulation was achieved with enhanced stability which makes this control strategy more attractive for linear load application. Both developed voltage control methods are robust to system uncertainties and guarantee voltage regulation with fast dynamic performance under abrupt load disturbances showing the superiority of the proposed voltage control strategies. The effectiveness of each control strategy is experimentally verified being capable of tracking their corresponding reference value rapidly with reliable transient response.

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