Simplified Small-Signal Model for Output Voltage Control of Asymmetric Cascaded H-Bridge Multilevel Inverter

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***Abstract*—This paper proposes a simplified small-signal model for output voltage control of a single-phase asymmetrical cascaded H-bridge multilevel inverter (ACHMI). The ACHMI is an *n*-series connected H-bridge converter, each one with a unique value at the dc link and usually scaled at {1:2:6:...} or {1:3:9:...}. By assuming that the small-signal variation component is equal in all *n* converter terminal ports, a simplified small-signal model is obtained. This assumption is carefully described and justified. To verify the veracity of the proposed model, two distinct control strategies are applied. One is a single-loop control scheme based on a modified proportional-integral (PI) controller. The other one is a double-loop control scheme based on a PI controller with feedforward action of the load current. Both controllers are tuned based on the dynamic behavior of the proposed model. Since the designed controllers based on the simplified model make the ACHMI output voltage to follow the reference without steady-state error, the proposed simplified model truly represents the inverter. Experimental results show the efficacy of the simplified model of the ACHMI through the two mentioned control strategies as well as the ACHMI installed in a microgrid.**

***Index Terms*—Modeling, multilevel inverter, small-signal, staircase modulation, voltage control.**

I. Introduction

THE usage of multilevel converters is proliferated in the past years, motivated mainly by the possibility of handling a great amount of power directly in the medium voltage without the need of using bulky transformers. Additionally, high-quality waveforms with low commutation frequency can be achieved. As a result, the filtering requirements are reduced and the production of electromagnetic radiation is minimized. Multilevel converters also have a niche of applications in low-voltage systems. The feature of modularity increases the reliability of the device, making these converters attractive choice for new applications [1].

Multilevel inverters can be realized by a variety of topologies such as diode-clamped [2], capacitor-clamped [3], modular cascaded [4], symmetric cascaded [5], [6], and asymmetric cascaded [7]–[9]. Regarding the last two topologies, their structures are similar. They are composed of H-bridge converters with isolated dc sources. Then, the multilevel inverter is made of all series-connected H-bridge converters. One dc source is used for each converter. The difference between the asymmetric and symmetric topologies falls in the value of the dc sources. In the symmetric topology, all converters use dc sources with the same value, while in the asymmetric topology, the dc sources have different values, usually scaled in {1:2:6:...} or {1:3:9:...}.

The multilevel inverter based on the asymmetrical cascaded H-bridge multilevel inverter (ACHMI) topology is an attractive choice for driving high-power loads in a standalone configuration. One of the main advantages of the ACHMI topology is the capability of the H-bridge converter with the highest dc source to operate at a reduced number of commutations compared to a classical H-bridge converter with a pulse width modulation (PWM). This means that the dc source is commuted few times within a 60-Hz cycle, and the bulk of the processing power in the whole structure is processed on this H-bridge converter with the highest dc source, resulting in reduced switching losses. However, this is only possible if the staircase modulation [10], [11] is applied. Different from the PWM, the staircase modulation does not present a well-behaved pattern for the harmonic content. The staircase modulation produces a nontrivial harmonic content and it is different for each H-bridge converter used in the ACHMI [12]. The equations describing the output voltage of an H-bridge converter when the staircase modulation is applied is also nontrivial, but they should be used in modeling the ACHMI dynamic behavior.

Even though the staircase modulation brings complexity to the topology, the ACHMI is employed in a variety of standalone

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applications [13]– [22]. In [13], [20], and [21], an ACHMI is used to drive a high-power machine, while in [15]–[17] and [19], some modifications in the H-bridge converter are proposed in order to achieve specific goals such as more levels at the output voltage with reduced number of modules or power loss reduction. An ACHMI using only one dc source to feed all H-bridge converters is proposed in [22]. These research works have their efficacy and validity. However, they are based on open-loop control strategies.

Employing open-loop control strategies is acceptable since the connected load is able to operate in such a condition. Nevertheless, when the load is sensitive, the ACHMI output voltage must be regulated through a dedicated controller aiming at reliable amplitude and frequency, waveforms with low total harmonic distortion, a fast dynamic response, and a zero steady-state error at the output voltage, even under a highly distorted and unpredictable load current.

In order to accurately design a controller suited for such requirements, a small-signal model representing the system is required. The small-signal model must contain all functions involved in the closed-loop strategy, such as the ACHMI, sensor, and the modulation transfer functions. Due to the nature of the staircase modulation, the small-signal model would be complex and linearization is not directly achieved [12]. In this context, this paper presents a simplified small-signal model for controlling the ACHMI output voltage in single-phase and standalone systems. The staircase modulation is used to command the switches of the ACHMI. By assuming that the small-signal variation component is equal in all *n* converter terminal ports, the process to obtain the small-signal model is simplified. This assumption is carefully described and justified.

To verify the veracity of the proposed model, two distinct control strategies are applied. One is a single-loop control scheme based on a modified proportional-integral (PI) controller. The other one is a double-loop control scheme based on a PI controller with feedforward action of the output current. Both controllers are tuned based on the dynamic behavior of the proposed model. Experimental results show that the controlled voltage follows the reference without a steady-state error, which leads to a conclusion that the proposed model truly represents the ACHMI dynamic behavior.

II. System Description

Fig. 1 presents the ACHMI connected to the point of common coupling (PCC) through an *LC* filter. The ACHMI is composed of *n* series-connected H-bridge converters, named module 1, 2, and *n*. A resistor *R* represents a generic load, connected to the PCC. Its value is later adopted as very high. The PCC voltage is measured and sent to the control block diagram, which in turn, runs the voltage controller and commands the switches for all modules. Each module has a terminal voltage composed of the product of the switching function $u(t)$ by the corresponding value of the dc-link voltage. In this paper, the $V_{\rm dc}$ voltages are assumed to be scaled in the ratio $\{1{:}2{:}6{:}\ldots\}$. Module 1 is considered to be the module with the highest $V_{\rm dc}$ voltage. A resistor is inserted in series with the capacitor to damp resonances of the *LC* filter.

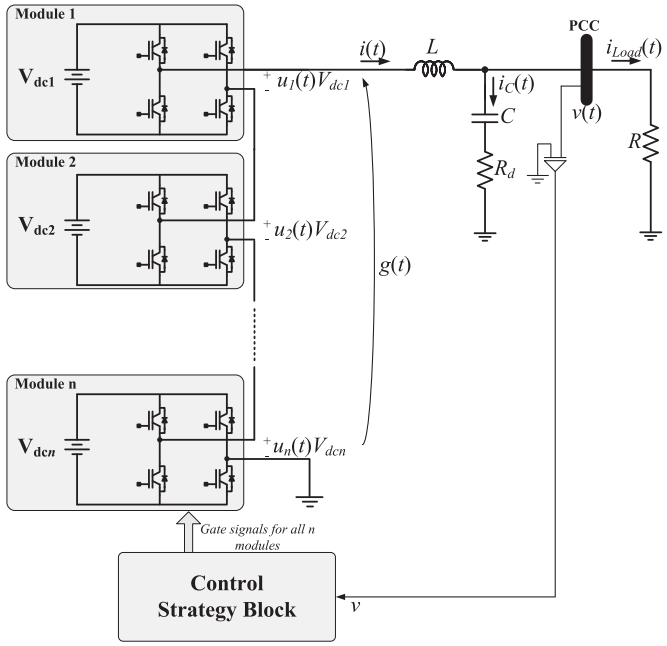

Fig. 1. ACHMI connected to a PCC through an *LC* filter.

A. Obtaining a Simplified Small-Signal Model

In order to design a controller for the ACHMI output voltage, a simplified small-signal model is required. The small-signal model is a transfer function that relates the output voltage with the switching function. By applying the voltage and current Kirchhoff's Laws in the circuit shown in Fig. 1, following equations are obtained:

$$L\frac{di\,(t)}{dt}+v\,(t)\;=\;u_1\,(t)\,V_{\rm dc1}u_2\,(t)\,V_{\rm dc2}+\cdots+u_n\,(t)\,V_{\rm dcn} \tag{1}$$

$$i_c\,(t)\;=\;i\,(t)-i_{\rm Load}\,(t)\,. \tag{2}$$

The right side of (1) can be written as

$$u_1\,(t)\,V_{\rm dc1}+u_2\,(t)\,V_{\rm dc2}+\cdots +u_n\,(t)\,V_{\rm dcn}=\sum_{k=1}^{n}u_k\,(t)\,V_{{\rm dc}k}. \tag{3}$$

Equation (3) can be written as

$$g\,(t)=\sum_{k=1}^{n}u_k\,(t)\,V_{{\rm dc}k}. \tag{4}$$

The current through the capacitor is given by

$$i_c\,(t)=C\frac{dv\,(t)}{dt}-C\frac{dR_d i_c\,(t)}{dt}. \tag{5}$$

Replacing (2) into (5), it results in

$$i\,(t)-i_{\rm Load}\,(t)=C\frac{dv\,(t)}{dt}-C\frac{dR_d\,(i\,(t)-i_{\rm Load}\,(t))}{dt}. \tag{6}$$

The current through the load is given by

$$i_{\mathrm{Load}}\left(t\right)=\frac{v\left(t\right)}{R}. \tag{7}$$

The current $i(t)$ in (6) is obtained by isolating $i(t)$ in (1), as

$$i\left(t\right)=\int\frac{g\left(t\right)}{L}dt-\int\frac{v\left(t\right)}{L}dt. \tag{8}$$

By replacing (7) and (8) into (6), it results in the following expression:

$$\int\frac{g\left(t\right)}{L}dt-\int\frac{v\left(t\right)}{L}dt-\frac{v\left(t\right)}{R}=C\frac{dv\left(t\right)}{dt} -C\frac{dR_d\left[\int\frac{g(t)}{L}dt-\int\frac{v(t)}{L}dt-\frac{v(t)}{R}\right]}{dt}. \tag{9}$$

Deriving both sides of (9) in time and arranging it, it results in

$$\frac{g\left(t\right)}{L}+\frac{CR_d}{L}\frac{dg\left(t\right)}{dt}=C\frac{d^2v\left(t\right)}{dt^2}+\frac{CR_d}{R}\frac{d^2v\left(t\right)}{dt^2} +\frac{1}{R}\frac{dv\left(t\right)}{dt}+\frac{CR_d}{L}\frac{dv\left(t\right)}{dt}+\frac{1}{L}v\left(t\right). \tag{10}$$

The left side of (10) is nonlinear due to the switching function. By applying the perturbation and linearization technique [23], output voltage and the switching function are replaced by a constant value added to a small-signal variation component, given by (11) and (12), respectively

$$v\left(t\right)=\bar{V}+\tilde{v}\left(t\right) \tag{11}$$

$$u\left(t\right)=\bar{U}+\tilde{u}\left(t\right). \tag{12}$$

Replacing (11) and (12) into (10), and using the notation given in (4), it results in

$$\frac{1}{L}\sum_{k=1}^{n}[\bar{U}_k+u_k(t)]V_{\mathrm{dc}k}+\frac{CR_d}{L}\frac{d}{dt}\left[\sum_{k=1}^{n}[\bar{U}_k+u_k(t)]V_{\mathrm{dc}k}\right] =C\frac{d^2[\bar{V}+\tilde{v}(t)]}{dt^2}+\frac{CR_d}{R}\frac{d^2[\bar{V}+\tilde{v}(t)]}{dt} +\frac{1}{R}\frac{d[\bar{V}+\tilde{v}(t)]}{dt}+\frac{CR_d}{L}\frac{d[\bar{V}+\tilde{v}(t)]}{dt}+\frac{1}{L}[\bar{V}+\tilde{v}(t)]. \tag{13}$$

Equation (13) can be split into the constant part and the small-signal part. The constant part is given by (14), once the derivative of constant terms is null.

$$\bar{V}=\sum_{k=1}^{n}\overline{U_k}V_{\mathrm{dc}k}. \tag{14}$$

Equation (14) is confirmed through the Kirchhoff's voltage Law in Fig. 1. Since the average voltage across the inductor is null, the average PCC voltage is the sum of the average voltages of all modules.

The small-signal part is given by

$$\frac{1}{L}\sum_{k=1}^{n}[\bar{U}_k+u_k(t)]V_{\mathrm{dc}k}+\frac{CR_d}{L}\frac{d}{dt}\left[\sum_{k=1}^{n}[\bar{U}_k+u_k(t)]V_{\mathrm{dc}k}\right] =C\frac{d^2\tilde{v}(t)}{dt^2}+\frac{CR_d}{R}\frac{d^2\tilde{v}(t)}{dt^2}+\frac{1}{R}\frac{d\tilde{v}(t)}{dt} +\frac{CR_d}{L}\frac{d\tilde{v}(t)}{dt}+\frac{1}{L}\tilde{v}(t). \tag{15}$$

The small-signal variation must be within a tiny range for allowing the operation point to be seen as linear. For this purpose, it is assumed that the small-signal variations from all modules have a linear proportion related to each other, simplifying the obtaining of a small-signal model. This statement is reinforced in the next section.

Therefore, the small-signal variation of the modules can be written as

$$u_1\left(t\right)=\frac{u_2\left(t\right)}{\epsilon_2}=\cdots=\frac{u_n\left(t\right)}{\epsilon_n}=\tilde{u}\left(t\right) \tag{16}$$

where $\epsilon_1\ldots\epsilon_n$ are the relation between the small-signal variation of the modules. $\epsilon_1\ldots\epsilon_n$ are constant and dependent on the operation point.

Thus, (15) can be rewritten as

$$\frac{1}{L}\tilde{u}\left(t\right)\sum_{k=1}^{n}\epsilon_kV_{\mathrm{dc}k}+\frac{CR_d}{L}\frac{d}{dt}\left[\tilde{u}\left(t\right)\sum_{k=1}^{n}\epsilon_kV_{\mathrm{dc}k}\right] =C\frac{d^2\tilde{v}\left(t\right)}{dt^2}+\frac{CR_d}{R}\frac{d^2\tilde{v}\left(t\right)}{dt^2}+\frac{1}{R}\frac{d\tilde{v}\left(t\right)}{dt} +\frac{CR_d}{L}\frac{d\tilde{v}\left(t\right)}{dt}+\frac{1}{L}\tilde{v}\left(t\right). \tag{17}$$

Taking the Laplace transform from (17) and arranging it, it results in

$$\frac{\tilde{V}\left(s\right)}{\tilde{U}\left(s\right)}=G_V\left(s\right)=\frac{\left(1+CR_ds\right)\sum_{k=1}^{n}\epsilon_kV_{\mathrm{dc}k}}{s^2\left(LC+\frac{LCR_d}{R}\right)+s\left(CR_d+\frac{L}{R}\right)+1}. \tag{18}$$

Equation (18) represents the proposed simplified small-signal model for the output voltage control of ACHMI.

B. Modulation Strategy

The switching function is defined according to the modulation strategy applied to the ACHMI. The ACHMI needs a suitable modulation in order not to lose its main advantage, which is the low commutation capability at the module with the highest V_{dc} voltage. The application of PWM in the ACHMI is not feasible due to its inherent high switching frequency. If the PWM is applied, all modules operate at a high switching frequency, considerably increasing the power losses.

The most common modulation applied to an ACHMI is the Staircase [10], [11], also known sometimes as nearest level modulation [24]. Fig. 2 presents the principle of operation of the staircase modulation. The reference signal for the desired ACHMI output voltage (a sinusoidal in this case) is used also as a signal to generate the pattern waveform for module 1 terminal voltage. This signal and a positive and a negative dc value are

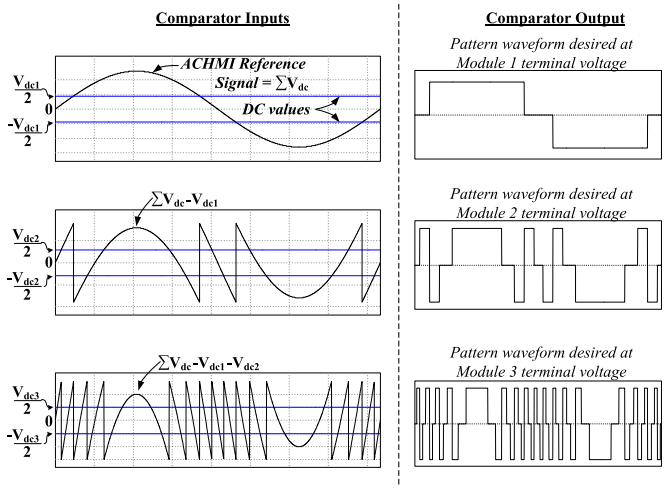

Fig. 2. Principle of operation of the staircase modulation.

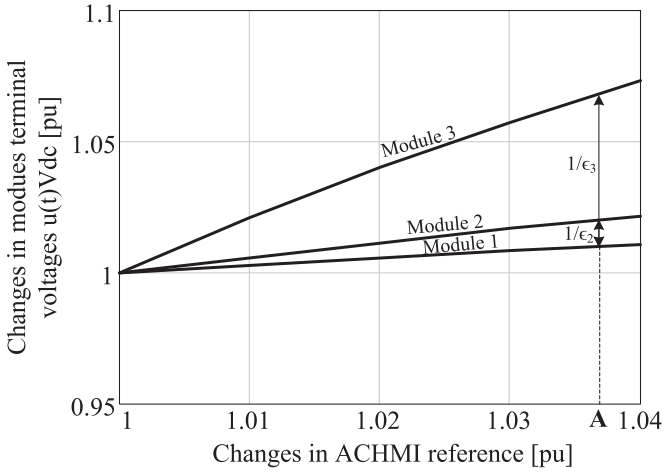

Fig. 3. How changes in the ACHMI reference modify the module terminal voltages.

used as inputs to a comparator. If the reference is higher than the dc value, in the positive semicycle, the comparator output is positive. Otherwise, it is null. A similar procedure is applied to the negative semicycle. The output signal of the comparator is the desired waveform at the terminal voltage of module 1.

The signal to generate the pattern waveform for module 2 is obtained by subtracting the sinusoidal reference from the comparator output signal of module 1. Then, the resulting signal is compared to another positive and negative dc value. The process is repeated until the last module has its pattern waveform. Since all the signals generating the pattern waveform for the modules come from one signal reference, a small variation on the signal reference will cause a small variation at each module reference. As a result, the statement presented in (16) is justified.

Fig. 3 shows how changes in the ACHMI reference modify the module terminal voltages. This chart was plotted considering the values presented in Table I by taking the average values of a half-cycle of the fundamental period. The chart also shows how to obtain ϵ_2 and ϵ_3 at the point of operation **A**. Since the

TABLE I
PARAMETERS OF THE SYSTEM

Symbol	Quantity	Value
L	Inductor	4.25 mH
C	Capacitor	5 uF
R	Fictitious Load	10 kΩ
Rd	Damping Resistor	25 Ω
n	Number of modules	3
$V*$	RMS value of the voltage reference	127 V
f	Fundamental frequency	60 Hz
$Pout$	Nominal power	2 kVA
V_{DC1}	V_{DC} voltage of module 1	144 V
V_{DC2}	V_{DC} voltage of module 2	48 V
V_{DC3}	V_{DC} voltage of module 3	24 V
ϵ_2	Relation between the module 1 and 2 terminal voltage	0.012846
ϵ_3	Relation between the module 1 and 3 terminal voltage	0.010036
Hv	Sensor gain	1/216
fs	Sampling frequency	12 kHz

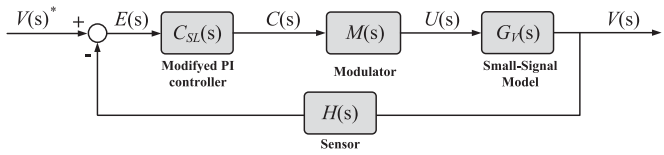

Fig. 4. Single-loop voltage control scheme.

desired ACHMI output voltage is almost always set at a defined value (127 Vrms for instance), its reference never changes and the values of ϵ_2 and ϵ_3 are easily obtained.

III. Designing Controllers From the Simplified Small-Signal Model

The proposed simplified small-signal model is verified through two different control approaches. One based on modified PI-based controller and another one based on a PI controller with feedforward action. These types of controllers were chosen because they are found in a large number of applications [25]. The first approach consists of a single-loop control strategy where the output variable is the ACHMI output voltage. The second consists of a double-loop strategy where the output variable is also the ACHMI output voltage and the inner loop is a current-controlled closed-loop mesh. Therefore, by showing that the voltage controller in these two approaches can be correctly designed by taking into account the proposed simplified small-signal model and that such controller makes the output voltage follow the reference without a steady-state error, the veracity of such a model is verified. The parameters of the system presented in Fig. 1 are given in Table I.

A. Single-Loop Voltage Control Scheme Based on a Modified PI Controller

Fig. 4 presents the single-loop voltage control scheme. The loop is composed of a modified PI controller, the staircase modulator, and the obtained simplified small signal. The modified PI controller is composed of two poles and one zero. This

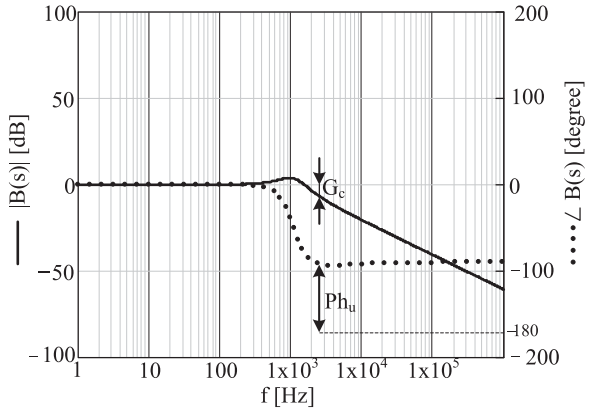

Fig. 5. Bode diagrams of the open-loop transfer function without the controller.

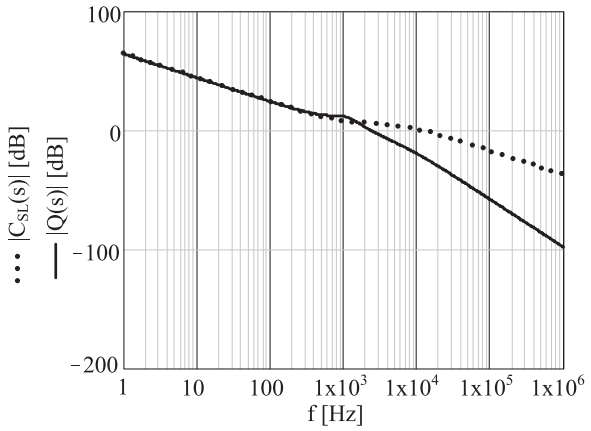

Fig. 6. Magnitude bode diagrams for the designed controller and the controlled open-loop transfer function.

TABLE II
REQUIREMENTS CHOSEN FOR DYNAMIC RESPONSE

Symbol	Quantity	Value
δ_{SL}	Desired phase margin	50°
f_c	Desired cutoff frequency	2.4 kHz

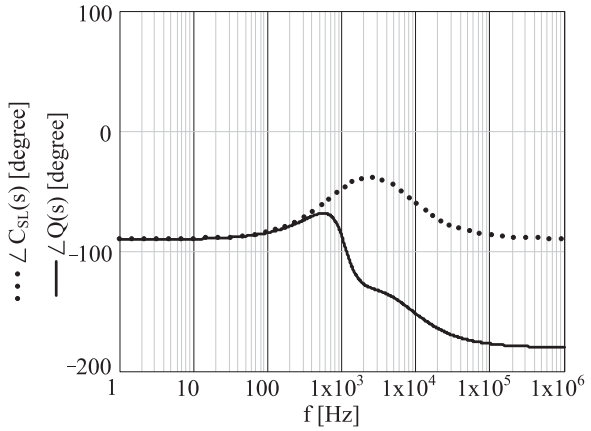

Fig. 7. Phase bode diagrams for the designed controller and the controlled open-loop transfer function.

composition is sufficient to make the controlled variable follow the sinusoidal reference in the system shown in Fig. 1 [26].

The open-loop transfer function without the controller is given by (19). This transfer function is defined for the sake of comparison with the open-loop transfer function with the controller included

$$B\left(s\right) = M\left(s\right) H\left(s\right) G_V\left(s\right). \tag{19}$$

The $G_v(s)$ is already given in (18). The modulator transfer function can be assumed equal to one [10]. Fig. 5 presents the Bode diagrams of the open-loop transfer function without the controller.

The open-loop transfer function with the controller is given by

$$Q\left(s\right) = C_{SL}\left(s\right) M\left(s\right) H\left(s\right) G_V\left(s\right) = C_{SL}\left(s\right) B\left(s\right). \tag{20}$$

The transfer function of the modified PI controller is given by

$$C_{SL}\left(s\right) = \frac{k_{SL}}{s} \frac{\left(1 + s/2\pi f_z\right)}{\left(1 + s/2\pi f_p\right)}. \tag{21}$$

To design the controller given in (21), Table II presents the requirements chosen for the dynamic response of the ACHMI output voltage.

According to the plots presented in Fig. 5, the gain and phase to be compensated are given by, respectively

$$G_c = \left|B\left(f_c\right)\right| = 6.05461 \text{ dB} = 2.007847 \tag{22}$$

$$\alpha_c = \delta_{\mathrm{SL}} - Ph_u - 90^\circ = 51.7495132^\circ \tag{23}$$

where Ph_u is the phase at the desired cutoff frequency in the open-loop transfer function without the controller, given by

$$Ph_u = \angle B\left(f_c\right) = -91.7495132^\circ. \tag{24}$$

The design procedure for the controller of (18) can be based on the methodology "*K*-factor approach" [27].

The *k*-factor is given by

$$k = \tan\left(\frac{\alpha_c}{2} + 45^\circ\right) = 2.8837181. \tag{25}$$

Therefore, the zero, pole, and the gain of the modified PI controller are given by respectively

$$f_z = \frac{f_c}{k} = 832.258879\,\mathrm{rad/s} \tag{26}$$

$$f_p = f_c k = 6.920923\ \mathrm{krad/s} \tag{27}$$

$$k_{\mathrm{SL}} = G_c 2\pi f_z = 1.0499509 \times 10^4. \tag{28}$$

Fig. 6 presents the magnitude bode diagrams for the designed controller and the controlled open-loop transfer function. The requirements were achieved. The cutoff frequency is 2.4 kHz.

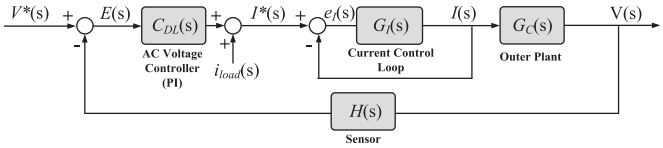

Fig. 8. Cascaded voltage control scheme.

Fig. 7 presents the phase bode diagrams for the designed controller and the controlled open-loop transfer function. The requirements were achieved. The phase margin is 50°.

B. Cascaded Voltage Control Scheme Based on a PI Controller

An alternative to control the output voltage of the ACHMI is to use a PI controller with feedforward action of the load current. One advantage of this method is that the damping structure is not needed. However, the load current (which is equal to the current after the *RC* branch) must be measured. In a scenario with several loads, all load currents must be measured. Fig. 8 presents the cascaded voltage control scheme. The ACHMI output voltage is controlled using a PI controller. The feedforward of the load current is added to the output signal of the ac voltage controller. An inner current control loop controlling the ACHMI output current is placed at the ac voltage controller.

Details of the procedure to design the controller in the inner loop are beyond the scope of this paper but can be found in [28] and [29]. It is assumed that the current follows its reference without a steady-state error and its closed-loop transfer function is given by

$$P\left(s\right)=\frac{G_I\left(s\right)}{1+G_I\left(s\right)}=\frac{1}{\tau_i s+1} \tag{29}$$

where τ_i is the constant time. Additionally, it is assumed that the cutoff frequency of the inner loop is sufficiently higher than that for the outer loop in order to make the controller decoupled.

To design the controller, the proposed small-signal model is reduced to a transfer function that relates the ACHMI output voltage and its output current. Replacing (2) and (7) into (5) and taking the Laplace Transform, the desired transfer function is

$$C_C\left(s\right)=\frac{\tilde{V}\left(s\right)}{\tilde{I}\left(s\right)}=\frac{1+sCR_d}{sC\left(1+\frac{R_d}{R}\right)+\frac{1}{R}}. \tag{30}$$

The open-loop transfer function without the controller and considering only the reference input is given by

$$L\left(s\right)=P\left(s\right)H\left(s\right)G_C\left(s\right). \tag{31}$$

The transfer function of the PI controller is given by

$$C_{\mathrm{DL}}\left(s\right)=k_{\mathrm{PI}}\frac{\left(s+z_{\mathrm{PI}}\right)}{s} \tag{32}$$

Table III presents the requirements chosen for the dynamic response of the ACHMI output voltage.

TABLE III
REQUIREMENTS CHOSEN FOR DYNAMIC RESPONSE

Symbol	Quantity	Value
δ_{DL}	Desired Phase Margin	60°
f_c	Desired cutoff frequency	600 Hz

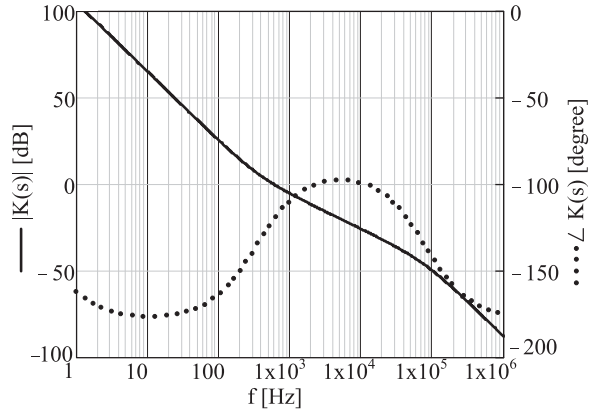

Fig. 9. Bode diagram of the open-loop transfer function with the designed PI controller.

The parameters of the PI controller are found as

$$z_{\mathrm{PI}}=\frac{\tan\left(\beta_c+90^\circ\right)}{2\pi f_c}=4.5887850\times10^{-4} \tag{33}$$

$$k_{\mathrm{PI}}=\sqrt{\frac{{G_c}^2}{\frac{{z_{\mathrm{PI}}}^{-2}+\left(2\pi f_c\right)^2}{\left(2\pi f_c\right)^2}}}=3.26474786 \tag{34}$$

where β_c is given by

$$\beta_c=\delta_{\mathrm{DL}}-Ph_{\mathrm{uDL}}-180^\circ=-30.030388^\circ. \tag{35}$$

Ph_{uDL} is the phase at the desired cutoff frequency in the open-loop transfer function without the controller. In this case, its value is –89.969º.

The open-loop transfer function with the controller is given by

$$K\left(s\right)=C_{\mathrm{DL}}\left(s\right)P\left(s\right)H\left(s\right)G_C\left(s\right)=C_{\mathrm{DL}}\left(s\right)L\left(s\right). \tag{36}$$

Fig. 9 presents the Bode diagram of the open-loop transfer function with the designed PI controller. As observed, the requirements were achieved.

IV. EXPERIMENTAL RESULTS

The system presented in Fig. 1 with the parameters showed in Table I was experimentally verified in a 2 kVA prototype. The control strategy approaches from Section III were implemented in the TMSF28335 floating point digital signal processor (DSP) and tested separately. A nonlinear load composed of a single-phase diode rectifier with an RC filter at the dc side is connected to the PCC, while the resistor *R* showed in Fig. 1 is removed.

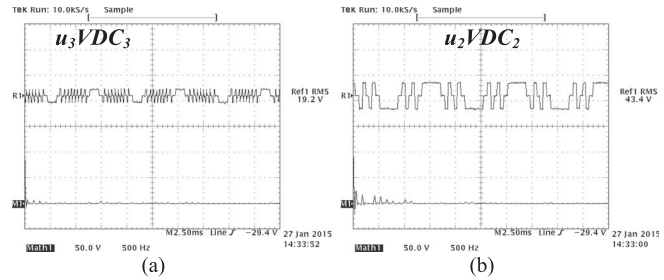

Fig. 10. Modules and ACHMI terminal voltages, and their harmonic contents. (a) Module 3, (b) module 2 (ChR1: 100V/div).

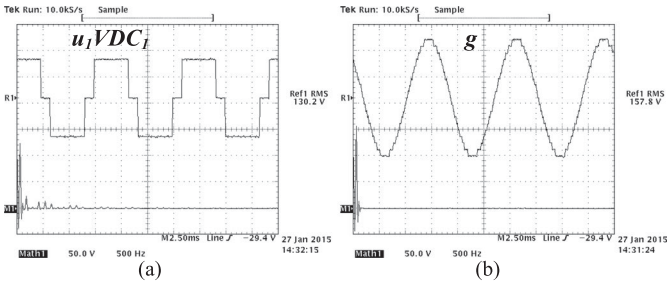

Fig. 11. Modules and ACHMI terminal voltages, and their harmonic contents. (a) Module 1 and (b) ACHMI. (ChR1: 100V/div).

A. Results for the Module Terminal Voltage With Staircase Modulation

Figs. 10 and 11 present the module terminal voltages as well as the ACHMI terminal voltage and their harmonic content. The results showed in Figs. 10(a), (b) and 11(a) are the module terminal voltages of the ACHMI. A reduced number of commutations within a 60-Hz cycle is evident, especially for the module 1 terminal voltage [see Fig. 11(a)]. Concerning the harmonic content, it is predominantly located around the fundamental component. Fig. 11(b) shows the ACHMI terminal voltage. The waveform is close to a sinusoidal, indicating the possibility of using a low-volume output filter. These results were collected with the ACHMI not connected at the PCC for a better visualization of the produced voltage when the staircase modulation is employed.

B. Results for the Single-Loop Voltage Control Scheme Based on a Modified PI Controller

Fig. 12 presents the ACHMI output voltage and its reference signal. The figure is divided into two parts. At the bottom, the result is shown in three 60 Hz cycles. At the top, a detail of the result is presented when the reference signal suffers a step on its amplitude. The output voltage follows the reference with negligible steady-state error as well as fast transient response, showing the efficacy of the controller designed based on the proposed simplified small-signal model. The reference signal was generated within the DSP and collected experimentally through a digital-to-analog converter (DAC). Due to the processing time required for the DAC conversion, the reference signal may suffer a delay compared to the controlled voltage.

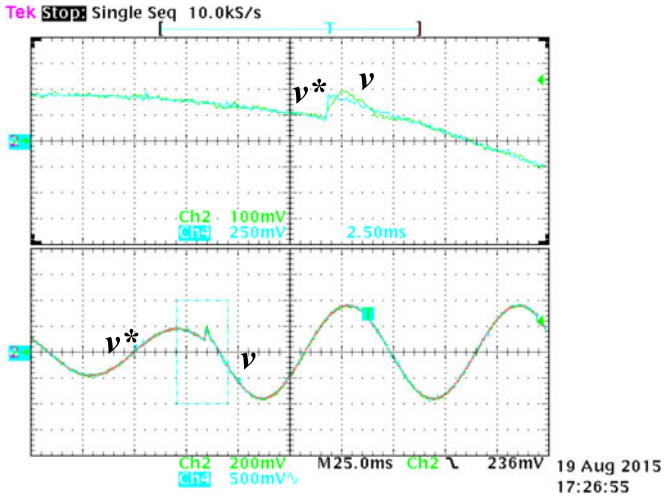

Fig. 12. ACHMI output voltage and its reference signal (Ch2: 2 mV/V).

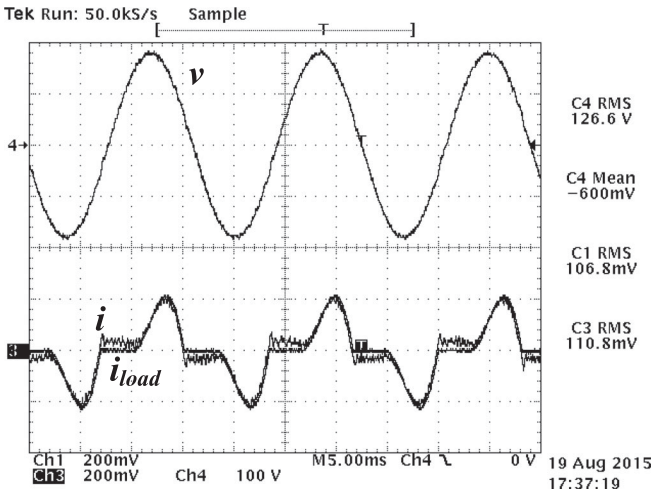

Fig. 13. ACHMI output voltage, the ACHMI output current the load current (Ch1,Ch3: 0.1 V/A).

Fig. 13 presents the ACHMI output voltage, the ACHMI output current, and the load current. The voltage is kept sinusoidal even under the presence of a nonlinear load. The slight difference in the currents is mainly due to the capacitor fundamental current component and damping resistor. Since they have similar and overlapped waveforms, the damping resistor has not significant effect on the power losses of the system.

C. Results for Cascaded Voltage Control Scheme Based on a PI Controller

Fig. 14 presents the ACHMI output voltage and its reference signal. Similarly, to the previous case, the ACHMI output voltage follows the reference signal with a negligible steady-state error.

Fig. 15 presents the ACHMI output voltage v, the ACHMI terminal voltage g, the module 1 terminal voltage ($u_1 V_{\mathrm{DC1}}$), and the load current. The module 1 terminal is derived from the staircase modulation. The ACMHI terminal voltage is close to a

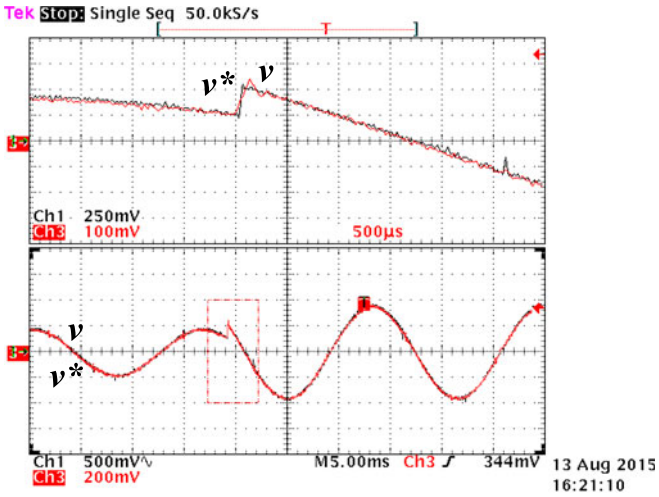

Fig. 14. ACHMI output voltage and its reference signal (Ch3: 2 mV/V).

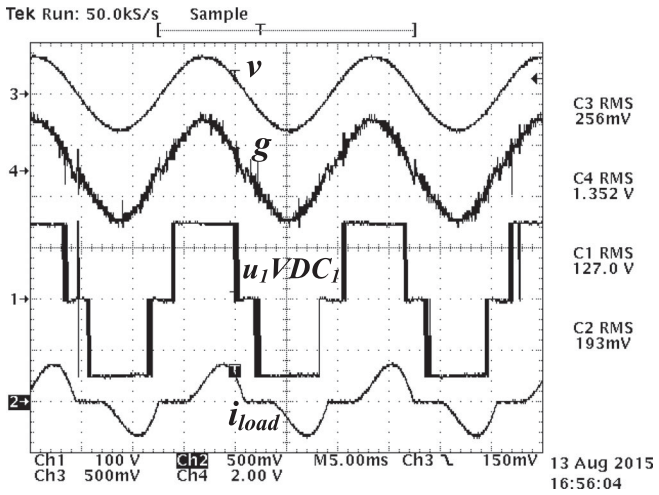

Fig. 15. ACHMI output voltage and its reference signal (Ch2: 0.1 V/A, Ch3: 2 mV/V, Ch4:10 mV/V).

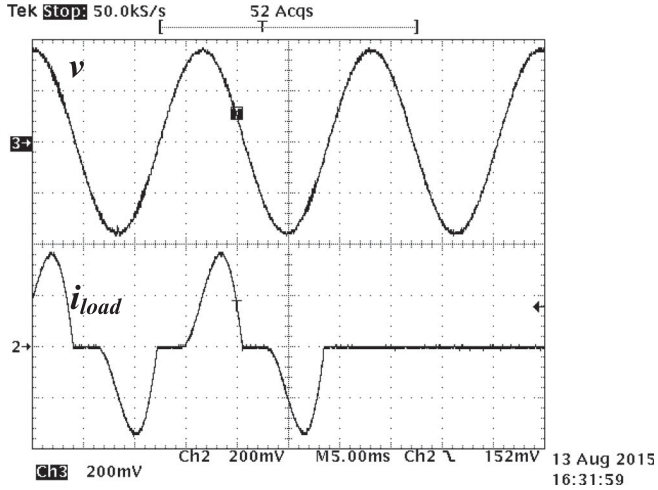

Fig. 16. ACHMI output voltage and the load current (Ch3: 0.1 V/A).

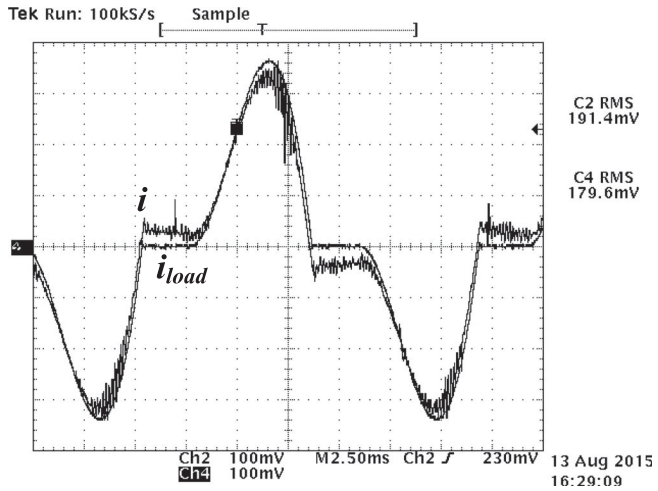

Fig. 17. ACHMI and load currents (Ch2,Ch4: 0.1 V/A).

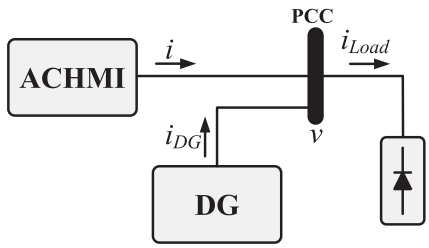

Fig. 18. ACHMI connected to an isolated microgrid.

sinusoidal waveform, and it is composed of the sum of module 1, 2, and 3 (the last two not shown) terminal voltages.

Fig. 16 presents the ACHMI output voltage and the load current. The voltage is kept sinusoidal even under the presence of the nonlinear load. After some time, the load is disconnected and the ACHMI is operating with no load. Nevertheless, the output voltage keeps controlled.

Fig. 17 presents the ACHMI output current and the load current. The waveforms are close to each other. The difference between them is due to the capacitor current.

D. Evaluation in an Isolated Grid

An ACHMI designed with the proposed small-signal model can operate in isolated microgrids. Isolated grids are characterized by the absence of a stiff generator. One of the generators must supply a controlled voltage regulated in frequency and amplitude. Other generators shall not temper these quantities. Isolated grids differ from islanded grids in the fact that the first is permanently energized by their DG, while the second is primarily energized by their DG only in the occurrence of a fault in the stiff generator. Fig. 18 presents the ACHMI connected to an isolated microgrid. The grid is composed of one PCC, one nonlinear load and one DG. The ACHMI is responsible for supplying the controlled voltage while the DG is controlled in current mode. For the sake of simplicity, the primary source of the DG is considered free of energy shortage. The ACHMI

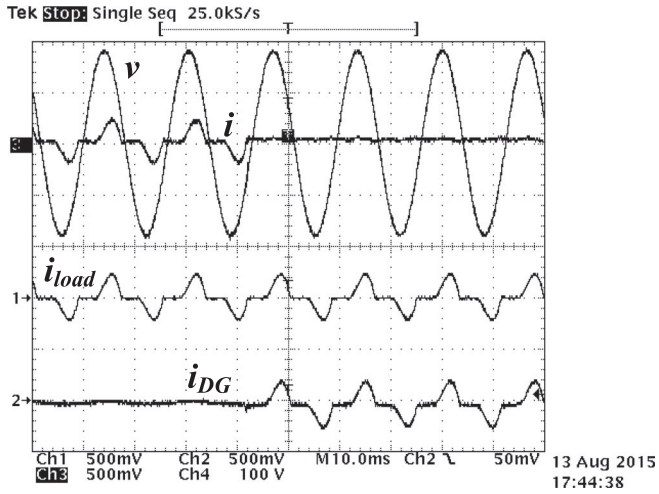

Fig. 19. Results for the moment when the DG begins to operate (Ch1,Ch2,Ch3: 0.1 V/A).

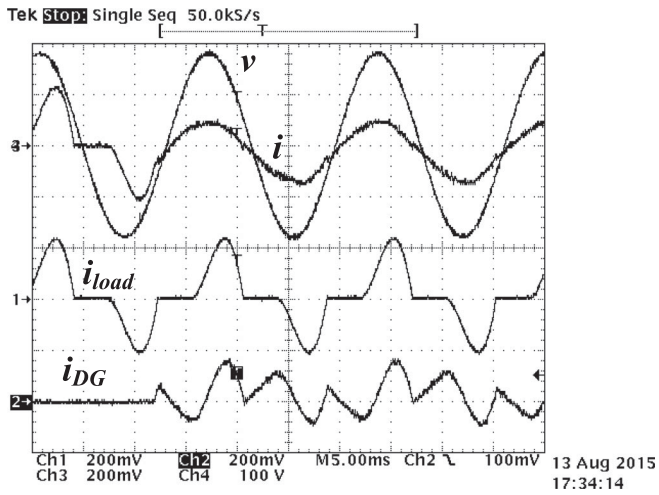

Fig. 20. Results for the moment when the DG operates as an active filter (Ch1,Ch2,Ch3: 0.1 V/A).

is voltage-controlled based on the procedure presented in Section III-A. The current reference for the DG is obtained through the conservative power theory [30].

Fig. 19 presents results for the moment the DG begins to operate. Initially, the ACHMI is feeding the load current and the DG current is null. Later, the DG supplies the load, and the ACHMI current is canceled. The load current and the PCC voltage are kept unchanged.

Fig. 20 presents results for the moment when the DG operates as an active filter for the ACHMI. Initially, the current of the ACHMI is the load current and the DG is inactive. As soon as the DG begins to operate as an active filter, the ACHMI has its current reshaped to a sinusoidal waveform.

V. Conclusion

This paper proposed a simplified small-signal model for the output voltage control of an ACHMI. To obtain the model, the assumption that the small-signal variation components in all modules of the ACHMI are equals was made. Later, the proposed model was verified through two distinct control strategies. One was a single-loop control scheme based on a modified PI controller, while the other one was a double-loop control scheme based on a PI controller with feedforward action of the load current. Both controllers were tuned based on the dynamic behavior of the proposed model. Since the designed controllers based on the simplified model made the ACHMI output voltage follow the reference without steady-state error, it can be concluded that the proposed simplified model truly represents the inverter. Experimental results showed the efficacy of the simplified model of the ACHMI through the two mentioned control strategies as well as the ACHMI behavior installed in a microgrid. The simulation files used in this project will be freely available on *busarello.prof.ufsc.br*.

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