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Comparative analysis of the intrinsic voltage gain and unit gain frequency between SOI and bulk FinFETs up to high temperatures

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ABSTRACT

This paper presents an experimental analysis of the analog application figures of merit: the intrinsic voltage gain (A_V) and unit gain frequency, focusing on the performance comparison between silicon triple gate pFinFET devices, which were processed on both Si and Silicon-On-Insulator (SOI) substrates. The high temperature (from 25 °C to 150 °C) influence and different channel lengths and fin widths were also taken into account. While the temperature impact on the intrinsic voltage gain (A_V) is limited, the unit gain frequency was strongly affected due to the carrier mobility degradation at higher temperatures, for both p- and n-type FinFET structures. In addition, the pFinFETs showed slightly larger A_V values compared to the n-type counterparts, whereby the bulk FinFETs presented a higher dispersion than the SOI FinFETs.

1. Introduction

A few years ago, multiple gate devices were considered as an alternative for planar CMOS scaling [1]. Most popular is the FinFET structure, which may come in a dual or triple-gate architecture, due to its electrostatic improvements and short-channel effect control [1,2]. Nowadays, for 28 nm and below CMOS technologies there is a competition between planar FD SOI devices and FinFETs. FinFETs can be fabricated on either bulk silicon or Silicon-On-Insulator (SOI) substrates as schematically represented in Fig. 1. After a decade of extensive research with the efforts to improve and study the device performance, the main semiconductor industries have been investing in this technology, such as Intel and IBM. The first one has been working on FinFET triple-gate devices (3D-transistors) fabricated on a silicon substrate. Its first generation microprocessor (Ivy-Bridge) introduced in 2011 used the 22 nm node [3] and in 2014 Intel launched the 14 nm node as its second bulk FinFET generation [4]. On the other hand, IBM has been developing its products on SOI substrates [5]. Concerning integrated circuits (IC's) scaling, the FinFET technology is widely used not only because of its feature size but also due to the constant necessity to provide higher levels of integration with less power consumption within IC's [6].

Apart from FinFET structures, ultra-thin body and buried oxide (UTBB) and gate-all-around (GAA) devices are promising candidates for the next generation technology nodes. UTBB, such as Fully Depleted SOI has significantly improved the V_T variability and minimizing the short-channel effect (SCE). On the other hand, it has raised new challenges related to the influence of source–drain (SD) series resistance and associated variability, which play an important role in analog figure of merit of these innovative devices [7]. The GAA devices can be stacked (planar nanowires) or fabricated vertically and present the best electrostatic control, resulting in superior immunity to the SCEs as compared to other structures. The GAAFETs are intended for the 7-nm technology node and beyond. Even though GAA devices allow gate length scaling, contact resistance still limits the performance [8].

It has been reported [9,10] that a FinFET presents inferior frequency behavior compared to a planar device, essentially owing to the lower carrier mobility along the sidewalls (n-channels)

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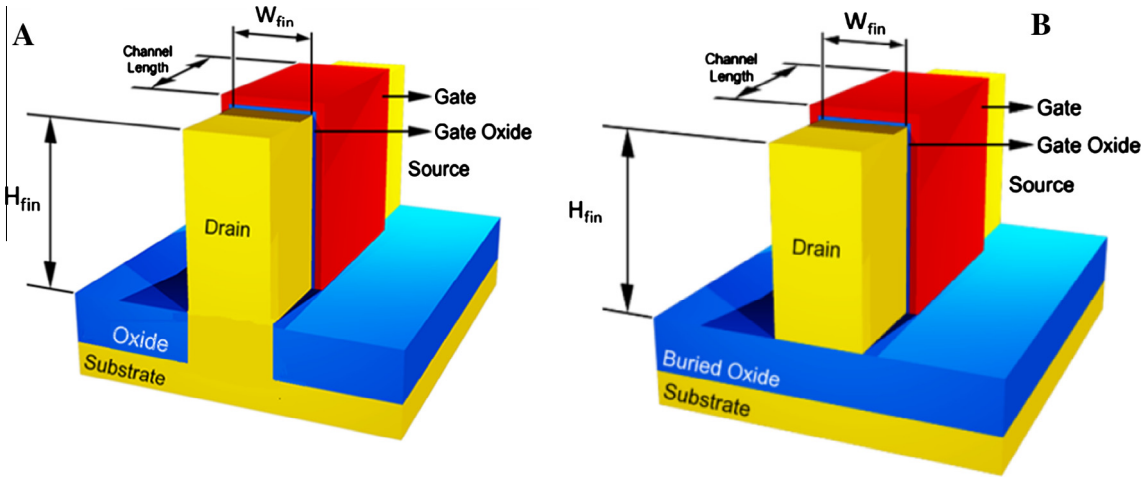

Fig. 1. Triple gate FinFET structures on silicon (A) and SOI (B) wafers.

and a higher series resistance, which limits mainly the unit gain frequency (f_T). In addition, according to the ITRS, the main figures of merit (FOM's) for RF and analog/mixed-signal technologies are the intrinsic gain (A_V), the cutoff frequency or unit gain frequency (f_T) and the parasitic capacitances [11]. Therefore, regarding analog applications, A_V and f_T are essential parameters that must be evaluated in FinFET structures.

It is worth mentioning that there is a secondary effect that might affect the analog performance, known as self-heating effect (SHE) [12], which is associated to the heating flux through the channel layer to the substrate. In a few cases, the low field mobility is degraded and another side effect is the negative output conductance [12]. Comparing both SOI and bulk FinFET structures, the bulk one presents a lower thermal resistance, so that the SHE is less effective there [13]. Moreover, it is believed that, as the operating frequency increases, the heating inside the device follows the same trend. If so, it would be expected that the unit gain frequency (f_T) and transconductance are degraded due to the low field mobility degradation by self-heating. On the other hand, as long as the output conductance (g_D) does not become negative, its value would increase, which is positive for the intrinsic voltage gain (A_V). This has indeed been confirmed for planar devices [14]. However, the operating frequency mode for SOI and bulk FinFETs must be further investigated in order to evaluate the impact of SHE on the analog performance.

In the literature, there are many works that compare the performance of bulk planar and SOI FinFETs [9,10,15]. Since FinFETs appear to have a potential for analog applications [6,15–18] many studies evaluated in detail the analog performance of FinFETs from different perspectives, mainly in SOI structures, such as: dual-dielectric constant (k) spacer underlap for n- and p-substrate types [19], underlap devices at low temperature operation [20], gate-underlap design effects [21], the influence of strain techniques [22] and the impact of the fin width on digital and analog performances of n-type devices [23]. On the other hand, few studies focus on the comparison of the bulk and SOI FinFET structures. At room temperature operation, this comparison has already been reported [1,24,25], with the focus on the impact of the device dimensions on the basic analog parameters. Aiming to complement the comparative study, this work evaluates the performance of bulk and SOI pFinFETs, taking into account the temperature influence A_V and f_T. In addition, a comparison will be made with the analog FOM for nFinFET counterparts at high temperature operation [26], for different channel lengths and fin widths.

2. Device characteristic details

The studied devices have been fabricated at imec/Belgium. Both bulk and SOI FinFETs were processed on p-type bulk and SOI substrates, respectively. In the latter case, the buried oxide thickness was 145 nm. The experiments were performed on SOI and bulk FinFETs with a fin height (H_{fin}) of 65 nm; fin widths (W_{fin}) of 20 nm, 65 nm and 130 nm; channel lengths (L) of 130 nm and 1 μm and a gate oxide of 2.5 nm SiON. In addition, all the FinFET structures have 5 fins in parallel and the wafer natural doping concentration was used (not intentionally doped).

The data were obtained by a semiconductor device parameter analyzer: Agilent B1500A. All measurements were performed with the temperature ranging from 25 °C up to 150 °C and for each condition three samples are evaluated. The threshold voltage and carrier mobility have been extracted by using the second derivative [27] and the Ghibaudo method (Y-function) [28] techniques, respectively.

In addition, 3D simulations have been performed using Sentaurus-Device simulator [29]. The models considered in the simulations include doping dependence model, high field saturation model, and vertical electric field dependence model (Enormal model) for mobility and the Shockley–Read–Hall model for carrier recombination. The gate work function value used is 4.5 eV.

The triple gate FinFET structures with dimension details for both bulk (A) and SOI (B) FinFETs, are presented in Fig. 1.

3. Results and discussion

Fig. 2 shows the temperature influence on the threshold voltage (V_T) for bulk and SOI pFinFETs, considering channel lengths (L) of 130 nm (A) and 1 μm (B) and different fin widths (W_{fin}).

One can notice that the SOI FinFETs present a small V_T reduction as the temperature increases. Since the channel is not intentionally doped ($\sim 10^{15}$ cm^{-3}), the Fermi level potential is less affected and as a result, V_T exhibits almost no variation for SOI pFinFETs when the temperature changes. On the other hand, the bulk FinFETs show a higher V_T variation, particularly as a function of W_{fin}. It is a consequence of the anti-punchthrough implantation, also known as ground plane (GP), which isolates the drain and source regions and one fin from the other, reducing the leakage current under the channel region that flows from the source to the drain [26]. This GP improves the Drain-Induced Barrier Lowering and also results in a higher threshold voltage for the bulk FinFET than the SOI one [30]. Moreover, as the temperature increases, there is a

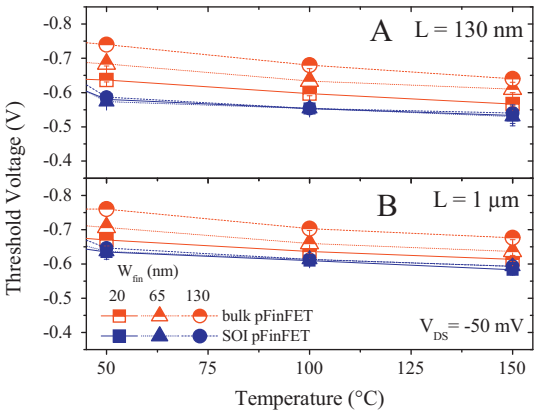

Fig. 2. Threshold voltage as a function of temperature, for 130 nm (A) and 1 µm (B) channel lengths, for bulk and SOI pFinFET devices.

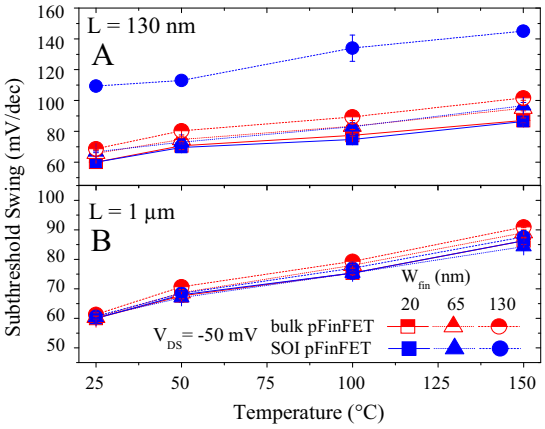

Fig. 4. Subthreshold swing as a function of the temperature for 130 nm (A) and 1 µm (B) channel lengths, for bulk and SOI pFinFET devices.

reduction of the current density [26], which contributes to both the Fermi level potential and V_T decrease. That confinement is not observed in SOI or bulk FinFETs that received no anti-punchthrough implantation [26].

Fig. 3 shows the simulated hole current density for two bulk pFinFET devices at $V_{GT} = -0.2$ V, Fig. 3A for a narrow device (W_{fin} of 20 nm) and Fig. 3B for a wide device (W_{fin} of 130 nm), where the cut plane was considered across the center of the channel. The ground plane has a Gaussian profile with a peak doping concentration of 1×10^{18} cm^{-3}. It is clearly noticeable that the narrowest device presents a strong coupling, giving rise to a current density flowing predominantly along the sidewalls. On the other hand, despite the fact that the main current also flows along the interface oxide/channel layers, for the widest device the current density is confined into the top and sidewall channel due to the GP, which indicates that the depletion region from the top gate is strongly modulated by the GP. As a result, the threshold voltage has a dependence on the fin width, as showed in Fig. 2, i.e. the V_T increases in absolute value (more negative values) as the W_{fin} becomes wider for the bulk pFinFET devices.

Fig. 4 shows the subthreshold swing (SS) as a function of temperature for different fin widths and channel lengths. As the temperature increases the SS also increases for both FinFETs, since it is proportional to the temperature [31]. In Fig. 4A one can observe that for a L of 130 nm SOI pFinFETs, the SS value is higher than for the other dimensions and devices. This behavior is due to the parasitic back interface conduction, which degrades the SS and the drain leakage current, which can be suppressed by applying a negative back gate bias [24]. Furthermore, it worsens even more with the temperature increase, which results in the gm/|I_{DS}| strong degradation (below 15 V^{-1}) as will be showed in Fig. 5B. It is worth to mention that, as SS is proportional to the temperature, the increase should be higher for SOI than bulk when self heating effect (SHE) has to be taken into account which is not observed in Fig. 4, indicating that SHE is not important in the studied devices.

Fig. 5 shows the transconductance over drain current ratio (gm/|I_{DS}|) as a function of the normalized drain current (|I_{DS}|/(W_{eff}/L)) for different fin widths, temperatures and both SOI and bulk FinFETs. It is possible to observe that the temperature degrades the gm/|I_{DS}| in the weak inversion region for both FinFET types due to the higher subthreshold swing (SS). However, the degradation is more pronounced in SOI FinFETs than in bulk counterparts for wide fins (W_{fin} of 130 nm). This behavior is due to the parasitic back interface conduction, which degrades the SS and the drain leakage current and it can be suppressed by a negative back gate bias [24]. Furthermore, it worsens even more with the temperature increase, as shown in Fig. 5B. On the other hand, in strong inversion gm/|I_{DS}| only slightly reduces compared to weak inversion, due to the carrier mobility (μ) degradation with the temperature increase for both FinFET types. It suggests that there is no significant dimensional dependence in this case. In addition, the temperature effects are the same as for L of 130 nm and W_{fin} of 20 nm devices in Fig. 5A.

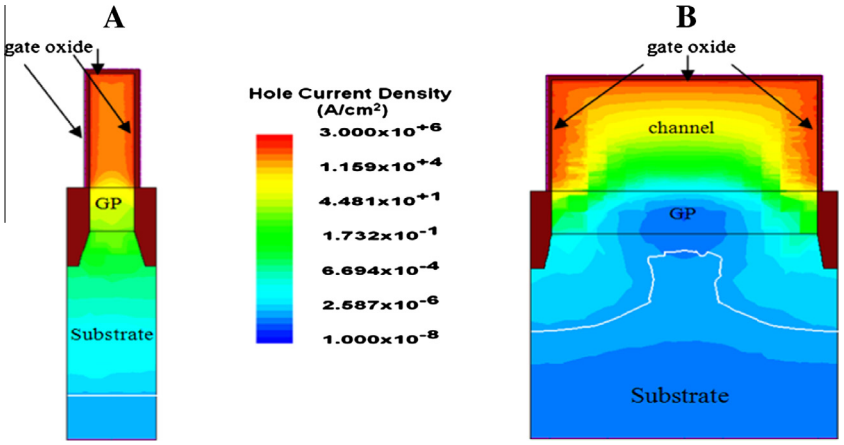

Fig. 3. Hole current density for bulk pFinFET structures 20 nm (A) and 130 nm (B) fin widths @ $V_{GT} = -0.2$ V.

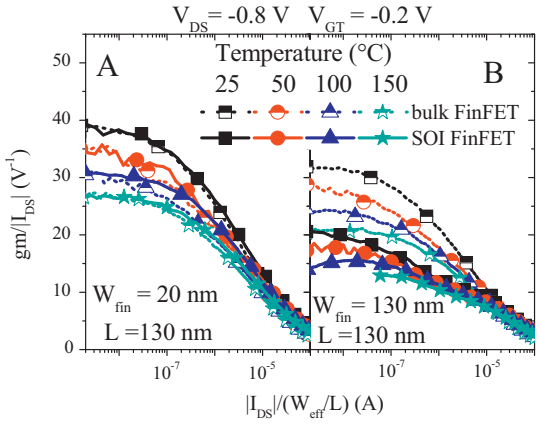

Fig. 5. Transconductance over drain current ratio as a function of normalized drain current for bulk and SOI pFinFET devices at different temperatures, for 20 nm (A) and 130 nm (B) fin widths.

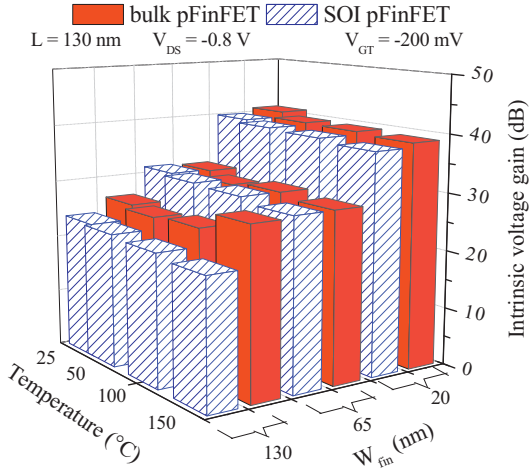

Fig. 7. Intrinsic voltage gain as a function of temperature and fin width, for bulk and SOI pFinFETs and channel length of 130 nm.

When the long channel devices (1 μm) are considered, the gm/|I_{DS}| for SOI and bulk FinFETs presents similar values since there is no predominance of parasitic effects at these dimensions.

Fig. 6 presents the early voltage (V_{EA}) as a function of temperature for short (130 nm) and long (1 μm) channels and different fin widths for both SOI and bulk FinFET technologies. Considering the long channel devices in Fig. 6B, the SOI FinFETs present higher V_{EA} values than the bulk ones, for all fin widths studied. It indicates that the buried oxide, in SOI FinFETs shows to be more effective to suppress the impact of the lateral electric field than the anti-punchthrough implantation or GP for bulk FinFETs. On the other hand, for shorter channels (130 nm) in Fig. 6A, similar V_{EA} values are found for SOI and bulk FinFETs. Furthermore, the temperature presents almost no significant V_{EA} variation for pFinFETs, at least for the studied range. Similar results have been reported for nFinFETs [21].

Fig. 7 shows the intrinsic voltage gain (A_V) as a function of temperature and fin width (W_{fin}), for bulk and SOI pFinFETs with channel length of 130 nm. It is clearly noticed that the A_V values increase as the fin width decreases due to a stronger electrostatic coupling. Focusing on the technology comparison (SOI and bulk), it is observed that similar A_V values are found, except for the wide fins where the SOI FinFETs are degraded due to the parasitic back-channel conduction. Regarding the temperature effects on the intrinsic voltage gain, no pronounced influence is reported, which indicates that the mobility degradation was the predominant factor in both the transconductance (gm) and the output conductance (g_D). Since A_V is given by the gm over g_D ratio, the temperature dependence of A_V is compensated. A comparison of the A_V values for the two FinFET and channel types is presented in Table 1. One can observe that the pFinFETs present higher A_V than the nFinFETs for both bulk and SOI structures, however, the bulk FinFET presents a larger dispersion of A_V independent of the channel type. Possibly the GP implantation is a strong source of variability.

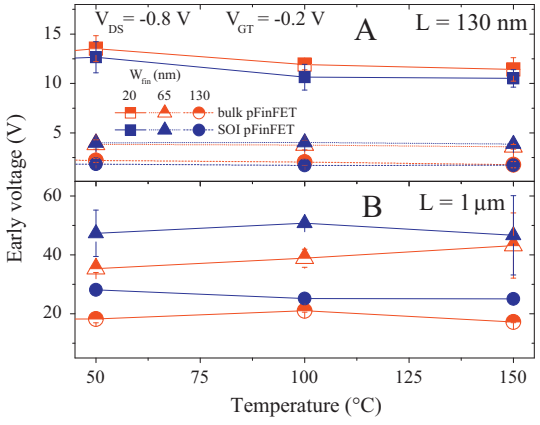

Fig. 6. Early voltage as a function of temperature for 130 nm (A) and 1 μm (B) channel lengths.

Fig. 8 presents the effective hole mobility, which was extracted by the Y-function technique, as a function of temperature for bulk and SOI FinFETs with a channel length of 130 nm. It shows that as the temperature increases the effective hole mobility (μ) decreases due to its degradation by phonon scattering [32]. In addition, the SOI FinFETs present a higher effective mobility than the bulk ones, independent of the fin width. It is a consequence of the ground plane (GP) implantation, as previously discussed, which degrades the carrier mobility in the channel region for bulk FinFETs. The fabrication processes of the anti-punchthrough implantation or GP [1] results in unrepaired displacement damage in the silicon lattice, giving rise to a lower μ compared to SOI FinFETs, where the GP is not present.

Figs. 9 and 10 present the unity gain frequency (f_T) as a function of temperature and fin width for bulk and SOI FinFETs with a channel length of 130 nm, for p-type and n-type channels, respectively.

The f_T can be calculated as shown in (1), where a load capacitance (C_L) of 1 pF is used.

$$f_T = \mathrm{gm}/(2\pi^* C_L) \quad (1)$$

In both figures it is noticeable that the SOI FinFETs present higher f_T values than the bulk ones, independent of fin width and temperature. This increase amounts to 20 MHz and 10 MHz, for p-type and n-type channels, respectively. As known from planar technology, the better control effectiveness (higher transconductance) for SOI technology than for bulk silicon is due to the body factor [31]. However, for SOI FinFETs, the higher transconductance is a consequence of the higher carrier mobility (μ), as previously shown in Fig. 8. Furthermore, when comparing the same FinFET structures with different channel type it is noticed that the f_T for n-type devices is around 40% higher than for p-type. The main reason is that the electron carrier mobility is larger than the corresponding value for holes.

Fig. 11 presents the simulated normalized capacitance ($C = C_{GD} + C_{GS}$) as a function of frequency for narrow and wide devices for both bulk and SOI pFinFETs.

Table 1
Intrinsic voltage gain at 150 °C for SOI vs. bulk FinFETs and p- vs. n-type channels for a channel length of 130 nm.

	W_{fin} of 20 nm		W_{fin} of 130 nm	
	n-type channel [26]	p-type channel	n-type channel [26]	p-type channel
	A_V (dB)			
SOI FinFET	37.15 ± 0.54	42.99 ± 0.36	20.28 ± 4.15	21.98 ± 0.03
bulk FinFET	37.62 ± 2.29	38.92 ± 0.85	25.22 ± 1.90	28.91 ± 5.52

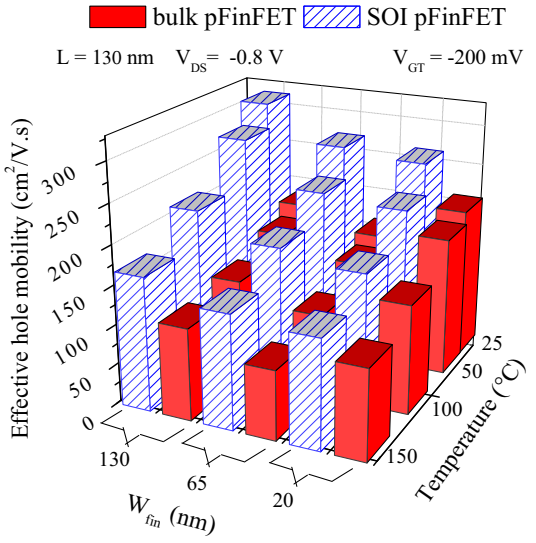

Fig. 8. Effective hole mobility as a function of temperature and fin width, for bulk and SOI pFinFETs with a channel length of 130 nm.

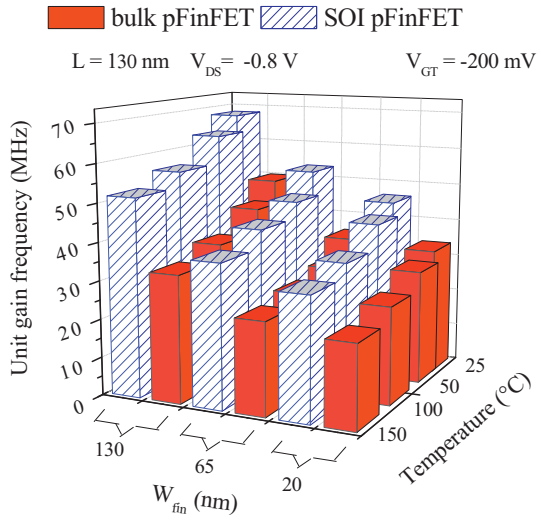

Fig. 9. Unit gain frequency as a function of temperature and fin width, for bulk and SOI pFinFETs with a channel length of 130 nm.

From these data one notices that the normalized C is slightly lower for the SOI FinFETs compared to bulk ones. This might be related to the main structural differences, i.e., the presence of a buried oxide (SOI devices) and a GP for the bulk counterparts. Therefore, the higher unit gain frequency for SOI FinFETs is not only due to a higher transconductance, but also thanks to the lower C values than the bulk FinFET devices.

As the gate channel length is scaled down towards 20 nm, the SOI FinFET seems to be more robust to DIBL and lower off-region drain current as compared to bulk FinFETs [33] due to the complete isolation from the source and drain regions by the buried oxide. Therefore, it would be expected that the intrinsic voltage gain might be affected by a transconductance reduction for the bulk FinFET, rather than the SOI counterpart, which should be further investigated.

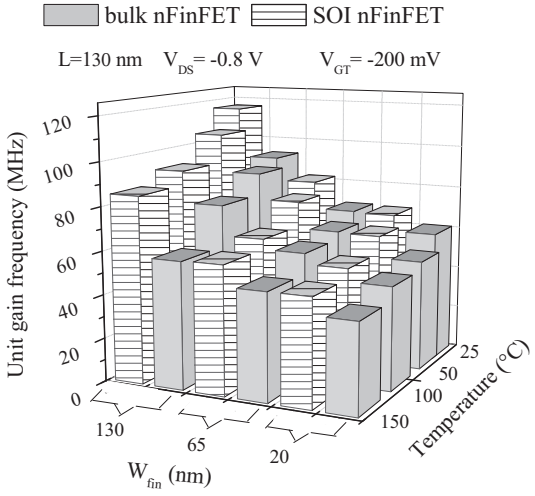

Fig. 10. Unit gain frequency as a function of temperature and fin width, for bulk and SOI nFinFETs with a channel length of 130 nm.

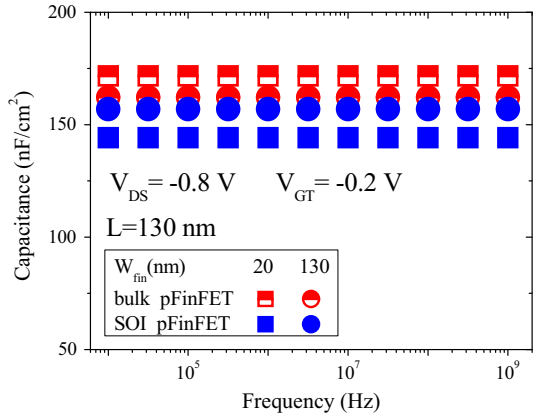

Fig. 11. Normalized capacitance as a function of frequency for bulk and SOI pFinFETs with different fin widths and a channel length of 130 nm.

4. Conclusions

Bulk FinFETs are shown to be comparable to the SOI counterparts, from a viewpoint of A_V and f_T. On the other hand, the latter present the best results, as long as the SOI FinFETs do not suffer from parasitic back conduction. Overall, the fin width is an important

parameter to be taken into account in analog applications: while the narrow devices seem to be the better option for optimizing A_V, on the other hand, the wider devices are more suitable for improved f_T performance.

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