

GR-Noise Characterization of Ge pFinFETs With STI First and STI Last Processes

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Abstract—This letter characterizes the generation-recombination noise of Ge pFinFETs, for three different integration schemes: shallow trench isolation (STI) first strained devices; STI last for relaxed and strained ones. It is shown that many Lorentzians exhibit a V_{GS} -independent and thermally activated characteristic frequency. This points out that the responsible defects are located inside the fin and they are found for all studied process conditions. One type of defect with a time constant value of 10 ms at room temperature is process-independent. Regarding the defects, their activation energies and hole capture cross sections have been extracted for fin widths varying from planar-like devices to narrow ones. It is shown that the STI last strained and relaxed devices yield a surface trap density three orders of magnitude above the typical value obtained for a blanket wafer.

Index Terms—Ge pFinFET, GR-noise characterization, STI first, STI last.

I. INTRODUCTION

THE beyond silicon materials (Ge and III-V) integration on a Si platform is challenging, one of the reasons being the large lattice mismatch with the silicon substrate [1]. Relaxation of the mismatch strain leads to the formation of a high density of misfit (MD) and/or threading dislocations (TD) [2]. When present, dislocations introduce deep states in the band gap, which give rise to generation-recombination of excess carriers [3], degrading several device parameters [4], [5] such as the threshold voltage (V_T), junction leakage current, and the inversion-layer mobility. Considering germanium for future node p-channel transistors, several strategies can be followed to reduce the TD density [6]. The different schemes studied in this work are outlined in Fig. 1. In the case of Shallow Trench

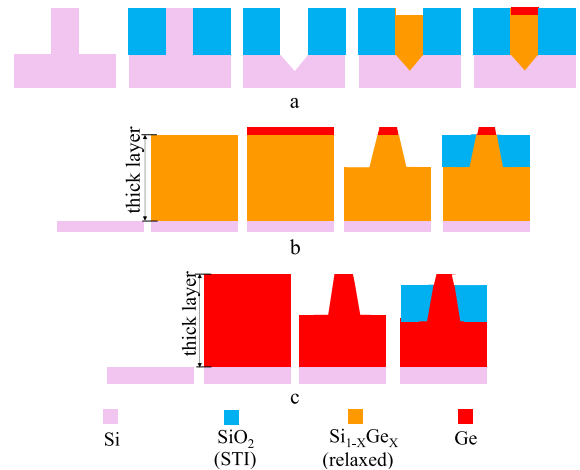


Fig. 1. Schematic of three different processes: STI first strained device; STI last strained and relaxed devices. (a) STI first process – strained Ge channel. (b) STI last process – strained Ge channel. (c) STI last process – relaxed Ge channel.

Isolation (STI) last integration, post-deposition annealing after epitaxial growth of a thick relaxed Ge-on-Si layer typically yields a TDD in the low 10^7 cm^{-2} range. For the STI first case, one can speculate on the aspect-ratio-trapping of dislocations at the STI oxide sidewalls to result in a defect-free top device layer. However, this only works for narrow devices while wide fins should not benefit from the effect. Finally, application of a SiGe relaxed buffer (SRB) layer between the Si substrate and the Ge channel may yield a low TDD in the range of a few 10^6 cm^{-2} [7].

This letter provides a first comparison of the impact of the different Ge-on-Si integration schemes shown in Fig. 1 on the device performance, using GR noise as an evaluation tool. It is demonstrated that the Lorentzian parameters, i.e., characteristic frequency (f_{ci}) and the plateau amplitude (A_i) can be used to study the lattice defects in the Ge fins, which are either grown-in (TDs) or processing-induced point defects. It is shown that the strained-Ge (sGe) fins on SiGe SRBs yield the lowest trap densities. At the same time, there is a tendency for smaller GR noise in narrow fins compared with more planar-like devices.

II. DEVICE CHARACTERISTICS

The p-type Ge FinFETs have been fabricated at imec/Belgium on 300 mm Si (100) wafers. The basic fabrication steps can be found in [8]. The FinFET device dimensions

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are a fin width (W_{fin}) that varies from 20 nm to 100 nm, geometric channel length (L_G) of 77 nm and fin height (H_{fin}) of 20 nm and 30 nm, STI first and last, respectively. The n-type in-situ doped relaxed buffers for both STI first ($Si_{1-x}Ge_x$ $x=75\%$) and last ($Si_{1-x}Ge_x$ $x=70\%$) have a doping concentration around $5 \times 10^{18} \text{ cm}^{-3}$. Except for the fabrication of the Ge channel, the device processing was identical. The gate stack is composed of a partially oxidized silicon passivation layer, HfO_2 , and a TiN metal gate, the Capacitance Equivalent Thickness (CET) is ~ 1.5 nm for both STI first strained and STI last relaxed devices and ~ 1.8 nm for STI last strained.

III. METHODOLOGY

A low-frequency noise spectrum is basically composed by three elements, i.e., white noise at high(er) frequency f ; $1/f'$ (or flicker noise) and a sum of Lorentzian components, also known as generation-recombination noise (GR). The latter can originate from traps in the gate oxide (so-called Random Telegraph Signals - RTSs) or in the depletion region of the transistor. Roughly speaking, RTS and bulk defects correspond with gate voltage (V_{GS}) dependent and independent Lorentzian parameters, respectively [9]. In the case of trap centers in the depletion region, one can derive an effective surface trap density for the GR centers N_{eff} from the plateau amplitude of the gate voltage spectral density A_i , as in (1) [10]

$$A_i = \frac{q^2 N_{eff}}{W_{eff} L_G C_{ox}^2} \tau_i \quad (1)$$

where q is the elementary charge, W_{eff} is the effective width (defined as the sum of W_{fin} and two times the fin height), L_G is the channel length and C_{ox} is the capacitance density. Finally, the GR center time constant (τ_i) is defined as $1/(2\pi f_{ci})$ [11]. The f_{ci} can be easily extracted from the observed bumps in the noise power spectra multiplied times f . The N_{eff} can be calculated from (1), considering the plateau from the gate voltage spectral density (S_{VG}), which is obtained from the ratio of the current power spectral density (S_{ID}) over the transconductance squared (S_{ID}/g_m^2).

The temperature dependence of the GR characteristics can be expressed by using (2) [12]

$$\ln(\tau T^2) = \frac{E_T - E_V}{kT} + \ln\left(\frac{h^3}{4k^2 \sigma_p \sqrt{6\pi^3 M_C m_e^{3/2} m_h^{1/2}}}\right) \quad (2)$$

where h is the Planck constant; m_e^* , m_h^* are the effective mass of electrons and holes respectively and M_C is the number of conduction band energy minima. From the $\ln(\tau T^2)$ as a function of $(1/kT)$ one extracts the trap activation energy (ΔE) and the hole capture cross section (σ_p), from the slope and y-intercept, respectively.

IV. DISCUSSION AND RESULTS

Fig. 2 shows the GR-noise time constant (τ) as a function of the gate voltage bias (V_{GS}) for different fin widths. One can observe that τ is V_{GS} -independent for the three different Ge pFinFETs processes, which strongly indicates that the defects are located in the depletion region, in other words: inside the fin. In addition, it is worth mentioning that the 30 nm wide STI-first strained pFinFET presents two different V_{GS} -independent GR centers, a fast and a slow one.

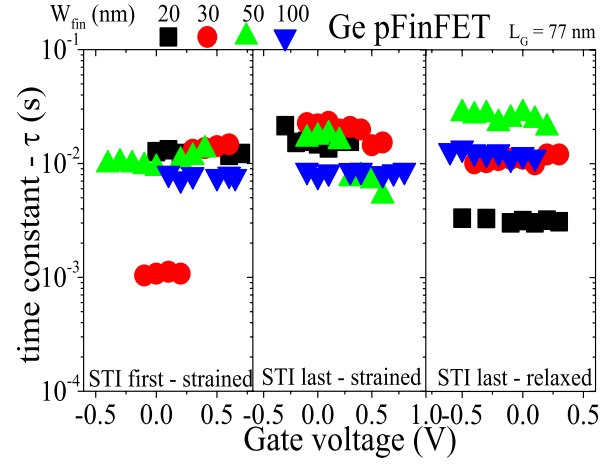


Fig. 2. Generation-recombination noise time constant as a function of gate voltage, for different Ge pFinFET processes at room temperature.

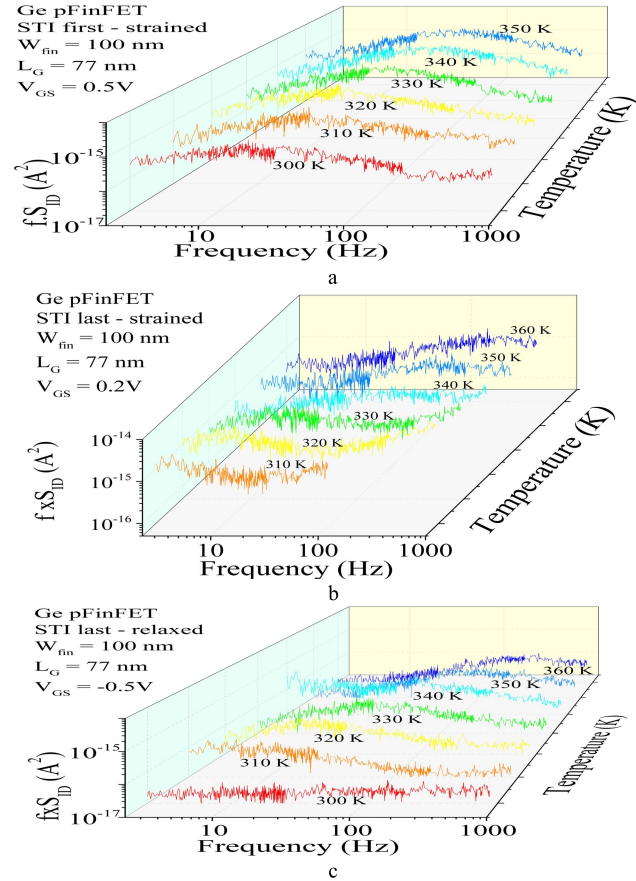


Fig. 3. Normalized spectral density as a function of frequency and temperature for different Ge pFinFET processes. (a) STI first process – strained Ge channel. (b) STI last process – strained Ge channel. (c) STI last process – relaxed Ge channel.

The latter dominates the weak inversion region (~ 10 ms), while the other the strong inversion one (~ 1 ms). Furthermore, it is possible to identify at least four τ values with the one around 10 ms not correlated with the Ge integration on silicon. As the front-end processing was the same for the different types of pMOSFETs, this could point to some common processing induced GR centers, i.e., related to S/D ion implantation and annealing, for example. Reference [13]

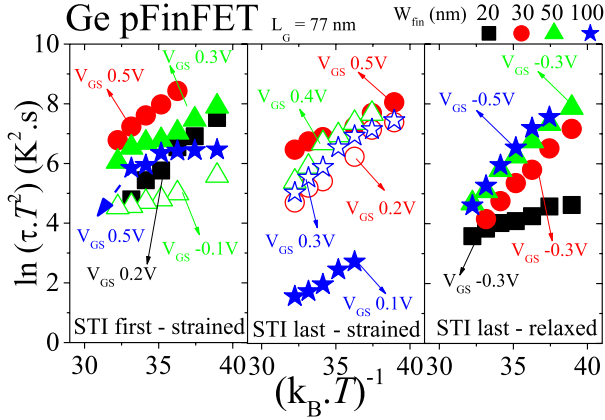


Fig. 4. Arrhenius plot for different Ge pFinFET STI processes.

TABLE I

DEVICE PARAMETERS FOR DIFFERENT Ge pFinFET STI PROCESSES

Process	W_{fin} (nm)	V_{GS} (V)	$*V_{GT}$ (V)	ΔE (eV)	σ_p (cm²)
STI first strained	20	0.2	0.43	0.47	1.4×10^{-17}
	30	0.5	0.02	0.40	1.5×10^{-19}
	50	0.3	0.28	0.25	2.4×10^{-21}
	50	-0.1	0.68	0.16	6.4×10^{-22}
	100	0.5	0.07	0.15	1.5×10^{-22}
STI last strained	30	0.2	0.32	0.41	1.7×10^{-18}
	30	0.5	0.02	0.23	7.8×10^{-22}
	50	0.4	0.08	0.44	1.6×10^{-18}
	100	0.3	0.17	0.37	2.5×10^{-19}
	100	0.1	0.37	0.3	1.3×10^{-18}
STI last relaxed	20	-0.3	0.55	0.41	1.2×10^{-21}
	30	-0.3	0.47	0.23	1.4×10^{-16}
	50	-0.3	0.44	0.44	1.7×10^{-17}
	100	-0.5	0.52	0.37	3.5×10^{-16}

* @ room temperature

reports the GR noise component V_{GS} -independent in Ge-on-Si planar pMOSFETs, which allows the extraction of its corner frequency (f_{ci}), consequently its time constant, from the presented humps in the power spectral density. The found f_{ci} varies from ~ 15 -25 Hz, resulting in a time constant range around ~ 6 -10 ms, which confirms that the typical value around 10 ms is related to the Ge layers.

Fig. 3 shows that the GR-noise is present in both STI approaches with a corner frequency, shifting towards higher values for increasing temperature, thanks to the inverse relation between the time constant and the intrinsic carrier concentration (n_i) [12], whereby the latter is thermally activated according to $\sim E_G/2$ (half the band gap energy) [14]. Therefore, the temperature increase results in a corner frequency shift towards higher frequency, i.e., a smaller time constant.

Fig. 4 presents the GR time constant in an Arrhenius diagram, which yields the activation energy (ΔE) and the hole capture cross-section (σ_p), as shown in Table I. Also the corresponding gate overdrive voltage (V_{GT}) is included, which represents the difference between the gate (V_{GS}) and threshold (V_T) voltages, and the V_{GS} value for each device during the temperature evaluation. According to the literature, the activation energy of a threading dislocation (TD) in Ge is between ~ 0.26 -0.33 eV above the valence band, as derived from Deep-Level Transient Spectroscopy (DLTS) [15]. Although

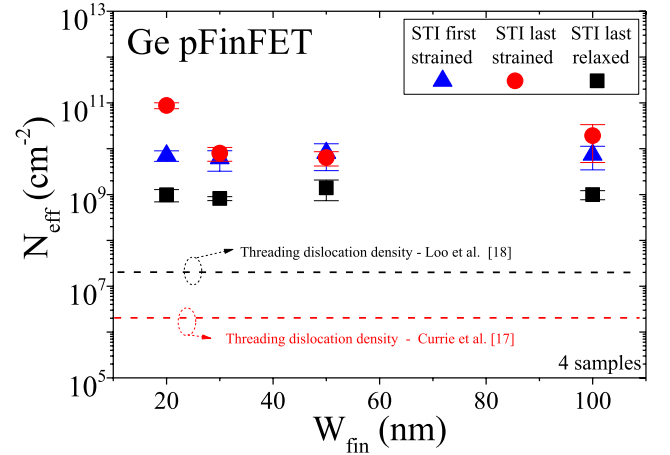


Fig. 5. Average of surface (effective) trap density as a function of fin width, for different Ge pFinFET processes at room temperature. Two reported values for blanket wafers are also indicated.

the ΔE values in Table I are derived from LFN measurements and there is some scatter for the different processes, one might correlate the defect origin with TDs. Additionally, it should be remarked that the weak inversion is the common and W_{fin} -independent operation regime for the studied devices, where the substrate typically affects the GR noise [16].

Fig. 5 shows the impact of the different processes on the surface trap density as a function of fin width. Both STI last approaches (strained and relaxed) clearly present higher surface trap density (N_{eff}) levels compared to the threading dislocation density (TDD) for blanket wafers $\sim 2 \times 10^6$ cm $^{-2}$ [17] and $\sim 1 \times 10^7$ cm $^{-2}$ [18], respectively. The STI-last relaxed devices show the lowest N_{eff} values thanks to the lower surface area compared to the other approaches.

The surface area values used for the N_{eff} extraction are $2.5 \sim 5.8 \times 10^{-9}$ cm 2 , $3.3 \sim 6.6 \times 10^{-9}$ cm 2 , $1.1 \sim 2.1 \times 10^{-9}$ cm 2 for STI first, STI last strained and relaxed devices, respectively.

For the STI first process, there is no significant difference of N_{eff} levels between narrow and wide devices, indicating that the SRB defect density value is lower than the obtained ones. Since most of the defects are trapped at the bottom of the trench due to the aspect ratio trapping (ART) and more efficiently in narrow trenches compared with the wide ones [19], the latter should present a higher trap density than for the narrow case. Furthermore, the STI-first devices present similar N_{eff} values than the STI-last counterpart, indicating that threading dislocations may not be the predominant GR centers in this case, which suggests processing-induced point defects as the responsible GR centers.

V. CONCLUSIONS

From the GR noise observed in Ge pFinFETs fabricated by three different STI processes, it is concluded from the gate-voltage independence of the Lorentzian parameters that the responsible defects reside in the fin region. The trap density is most likely not related to the better crystalline quality of the SiGe SRB. Furthermore, the ART effect, in the case of STI first, cannot be seen in the trap density. Finally, the responsible GR centers seem to originate from processing-induced point defects.

REFERENCES

- [1] S. Takagi and M. Takenaka, "Prospective and critical issues of III–V/Ge CMOS on Si platform," *Electrochem. Soc. Trans.*, vol. 35, no. 3, pp. 279–298, May 2011, doi: 10.1149/1.3569921.
- [2] R. People and J. C. Bean, "Calculation of critical layer thickness versus lattice mismatch for G_xSi_{1-x} /Si strained-layer heterostructures," *Appl. Phys. Lett.*, vol. 47, no. 3, pp. 322–324, Aug. 1985, doi: 10.1063/1.96206.
- [3] W. Schröter and H. Cerva, "Interaction of point defects with dislocations in silicon and germanium: Electrical and optical effects," *Solid State Phenomena*, vols. 85–86, pp. 67–144, Dec. 2011, doi: 10.4028/www.scientific.net/SSP.85-86.67.
- [4] E. Simoen, G. Eneman, M. B. Gonzalez, D. Kobayashi, A. L. Rodríguez, J.-A. Jiménez Tejada, and C. Claeys, "High doping density/high electric field, stress and heterojunction effects on the characteristics of CMOS compatible p-n junctions," *J. Electrochem. Soc.*, vol. 158, pp. R27–R36, Mar. 2011, doi: 10.1149/1.3555103.
- [5] E. Simoen, G. Brouwers, R. Yang, G. Eneman, M. B. Gonzalez, F. Leys, B. D. Jaeger, J. Mitard, D. Brunco, L. Souriau, N. S. Cody, S. Thomas, L. Lajaunie, M.-L. David, and M. Meuris, "Is there an impact of threading dislocations on the characteristics of devices fabricated in strained-Ge substrates?" *Phys. Status Solidi C*, vol. 6, no. 8, pp. 1912–1917, Aug. 2009, doi: 10.1002/pssc.200881446.
- [6] C. Claeys, E. Simoen, G. Eneman, K. Ni, A. Hikavy, R. Loo, S. Gupta, C. Merckling, A. Alian, and M. Caymax, "Review—Device assessment of electrically active defects in high-mobility materials," *Electrochem. J. Solid State Sci. Technol.*, vol. 5, no. 4, pp. P3149–P3165, Apr. 2016, doi: 10.1149/2.0221404jss.
- [7] E. A. Fitzgerald, Y. H. Xie, M. L. Green, D. Brasen, A. R. Kortan, J. Michel, Y.-J. Mii, and B. E. Weir, "Totally relaxed Ge_xSi_{1-x} layers with low threading dislocation densities grown on Si substrates," *Appl. Phys. Lett.*, vol. 59, p. 811, May 1991, doi: 10.1063/1.105351.
- [8] A. V. Oliveira, P. G. D. Agopian, J. A. Martino, E. Simoen, J. Mitard, L. Witters, R. Langer, N. Collaert, C. Claeys, and A. Thean, "Effective hole mobility and low-frequency noise characterization of Ge pFinFETs," in *Proc. Joint Int. EUROSOTI Workshop Int. Conf. Ultimate Integr. Silicon*, Vienna, Austria, 2016, pp. 162–165, doi: 10.1109/ULIS.2016.7440078.
- [9] I. Lartigau, J. M. Routoure, W. Guo, B. Cretu, R. Carin, A. Mercha, C. Claeys, and E. Simoen, "Low temperature noise spectroscopy of 0.1 μm partially depleted silicon on insulator metal-oxide-semiconductor field effect transistors," *J. Appl. Phys.*, vol. 101, p. 104511, May 2007, doi: 10.1063/1.2732685.
- [10] E. Simoen, M. G. C. de Andrade, M. Aoulaiche, N. Collaert, and C. Claeys, "Low-frequency-noise investigation of n-channel bulk FinFETs developed for one-transistor memory cells," *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1272–1278, May 2012, doi: 10.1109/TED.2012.2186815.
- [11] N. B. Lukyanchikova, "Sources of the lorentzian components in the low-frequency noise spectra of submicron metal-oxide-semiconductor field-effect transistors," in *Noise and Fluctuations Control in Electronic Devices*, A.A. Balandin, Ed. American Scientific Publishers, 2002, pp. 1–34.
- [12] V. Grassi, C. F. Colombo, and D. V. Camin, "Low frequency noise versus temperature spectroscopy of recently designed Ge JFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 12, pp. 2899–2905, Dec. 2001, doi: 10.1109/16.974725.
- [13] E. Simoen, J. Mitard, B. De Jaeger, G. Eneman, A. Dobbie, M. Myronov, D. R. Leadley, M. Meuris, T. Hoffmann, and C. Claeys, "Defect-related excess low-frequency noise in Ge-on-Si pMOSFETs," *IEEE Electron Device Lett.*, vol. 32, no. 1, pp. 87–89, Jan. 2011, doi: 10.1109/LED.2010.2089968.
- [14] B. Lengeler, "Semiconductor devices suitable for use in cryogenic environments," *Cryogenics*, vol. 14, no. 8, pp. 439–447, Aug. 1974, doi: 10.1016/0011-2275(74)90206-9.
- [15] M. B. Gonzalez, E. Simoen, G. Eneman, B. De Jaeger, G. Wang, R. Loo, and C. Claeys, "Defect assessment and leakage control in Ge junctions," *Microelectron. Eng.*, vol. 125, pp. 33–37, Aug. 2014, doi: 10.1016/j.mee.2014.01.012.
- [16] E. Simoen, J. Mitard, B. De Jaeger, G. Eneman, A. Dobbie, M. Myronov, T. E. Whall, D. R. Leadley, M. Meuris, T. Hoffmann, and C. Claeys, "Low-frequency noise characterization of strained germanium pMOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 3132–3139, Sep. 2011, doi: 10.1109/TED.2011.2160679.
- [17] M. T. Currie, S. B. Samavedam, T. A. Langdo, C. W. Leitz, and E. A. Fitzgerald, "Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing," *Appl. Phys. Lett.*, vol. 72, pp. 1718–1720, Apr. 1998, doi: 10.1063/1.121162.
- [18] R. Loo, G. Wang, L. Souriau, J. C. Lin, S. Takeuchi, G. Brammert, and M. Caymax, "High quality Ge virtual substrates on Si wafers with standard STI patterning," *J. Electrochem. Soc.*, vol. 157, no. 1, pp. H13–H21, Nov. 2009, doi: 10.1149/1.3244564.
- [19] J. Z. Li, J. Bai, C. Major, M. Carroll, A. Lochtefeld, and Z. Shellenbarger, "Defect reduction of GaAs/Si epitaxy by aspect ratio trapping," *J. Appl. Phys.*, vol. 103, p. 106102, May 2008, doi: 10.1063/1.2924410.