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Split CV mobility at low temperature operation of Ge pFinFETs fabricated with STI first and last processes

A V Oliveira^{1,2}, E Simoen^{2,3}, P G D Agopian^{1,4}, J A Martino¹, J Mitard², L Witters², R Langer², N Collaert², A Thean² and C Claeys^{2,5}

¹ LSI/PSI/USP, University of Sao Paulo, Sao Paulo, Brazil

² imec, Leuven, Belgium

³ Department of Solid State Sciences, Ghent University, Ghent, Belgium

⁴ UNESP, Universidade Estadual Paulista, Sao Joao da Boa Vista, Brazil

⁵ EE Department, KU Leuven, Leuven, Belgium

E-mail: avo.eng@gmail.com

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Abstract

The effective hole mobility of long strained Ge pFinFETs, fabricated with shallow trench isolation (STI) first and last approaches, is systematically evaluated from room temperature down to 77 K, from planar-like (100 nm) to narrow (20 nm) devices. The goal is to identify the dominant scattering mechanism. Here, the split capacitance-voltage (CV) technique has been applied, based on combined current-voltage (I - V) and CV measurements. It is shown that even at 77 K, the phonon scattering mechanism dominates the STI last process, while the Coulomb scattering strongly affects the STI first approach. On the other hand, the latter shows slightly higher hole mobility compared to the STI last counterpart.

Keywords: split CV mobility, low temperature operation, Ge pFinFETs, STI first process, STI last process

(Some figures may appear in colour only in the online journal)

Introduction

High-mobility materials, such as germanium (SiGe) and/or III-V are promising alternatives to replace silicon beyond the 7 nm Complementary Metal–Oxide–Semiconductor (CMOS) node. However, Si platform integration must be taken into consideration in order for it to become compatible with industrial manufacturing [1]. The Si-based platform integration is not limited to Ge and III-V CMOS options [2], but also extends to millimeter-wave (mm-wave) [3], III-V for photonic [4] and low-cost photovoltaic [5] applications, monolithic integration of CMOS and optoelectronic devices [6] and III-V lasers [7]. Additionally, the expertise from the Si devices, i.e. low leakage in multiple gate structures in a Field Effect Transistor (FET), such as FinFETs [8] can be highly taken into consideration for future devices. The four times higher bulk hole mobility of Ge compared with Si [9] makes it

relevant for p-channel devices. On the other hand, a few challenges should be either overcome or reasonably controlled to meet this goal; the surface passivation layer can reduce the density of interface states (D_{IT}), the formation of low-leakage source/drain junctions with a low parasitic series resistance and the crystalline defects in the channel [9]. The latter challenge arises from the misfit dislocation and threading dislocation (TD) [10] in the Ge layers on silicon, since Ge layers have to be heteroepitaxially grown on bulk Si wafers. The presence of these extended defects results in device performance degradation [11, 12].

A few approaches can be employed in order to reduce the TD density level. One of them is growing a virtual Ge substrate that consists of a thick relaxed Ge layer grown directly on a Si wafer [13]; this, however, presents an inferior performance compared with compressively strained Ge devices [14]. The other approach is to grow a SiGe strain-relaxed

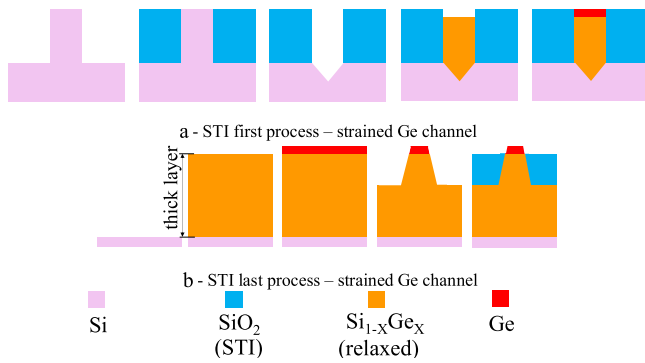


Figure 1. Schematic of two different STI processes: first strained and last strained devices.

buffer (SRB) layer, followed by the growth of a thin compressively strained Ge layer. The SRB process can involve either a thick grown layer ($\sim 1 \mu\text{m}$) on a Si wafer that achieves the lowest TD density value ($\sim 10^6 \text{ cm}^{-2}$) [15] or consist of applying a fabricated layer in a predefined shallow trench isolation (STI) region. The latter approach benefits from aspect ratio trapping (ART), which traps most of the TDs in the bottom part of the layer when the SRB layer thickness has an aspect ratio greater than 3 [16]. The STI processes have been extensively investigated in order to achieve similar device performances for both processes [17–20]. One advantage of the STI first process is that there is no necessity of growing a $1 \mu\text{m}$ thick SRB layer; this results in a more cost effective option compared with the STI last one. On the other hand, the maximum transconductance and off-drain current are important parameters to consider, whereby the STI last approach has presented a slightly improved performance compared to the STI first counterpart [18, 19].

This work aims to evaluate the combination of a promising high-mobility channel material, i.e. Ge, and a FinFET structure, which presents a superior short-channel effect control compared to planar devices [21]. These Ge pFinFETs have been fabricated with a STI first and STI last process flow, as presented in figure 1. The influence of low temperature operation on the off-current region has already been reported in [14, 22] for the studied devices. Here, emphasis is on the on-current regime and in particular on the extraction of the inversion-layer hole mobility as a function of temperature (T), in order to gain insight into the dominant scattering mechanisms. This paper is arranged as follows. It starts with the description of the main device characteristics, where the main dimensions and process data are shown. Subsequently, it describes how the effective mobility analysis has been done, where the split capacitance-voltage (CV) method is briefly discussed. Next, the effective mobility behavior as a function of the fin width and temperature is presented. Finally, a general discussion is outlined in order to give further explanation for the main findings.

Device characteristics

Si platform-integrated hetero-epitaxy devices, i.e. p-type Ge FinFETs, have been fabricated at imec on 300 mm Si (100)

substrates for both STI first and last processes. The basic fabrication steps and the main device dimensions can be found in figure 2 and table 1, respectively. Except for the fabrication of the Ge channel, the front-end device processing was similar.

The STI first devices have been fabricated through predefined STI trenches with different widths, where a $\sim 140 \text{ nm}$ thick SiGe SRB layer replaces a previous Si fin. The SiGe SRB layer is thick enough to keep the advantages of the ART technique. Afterwards, a thin strained Ge layer is grown by chemical vapor deposition (CVD), reaching a final fin height of 20 nm . Further SRB and Ge layer growths for the STI first process are detailed in [23]. The STI last approach starts from a thick SiGe SRB layer ($\sim 1 \mu\text{m}$), followed by 30 nm thin Ge layer growth, where the fin is defined through the Ge recess, and subsequently the STI is deposited in etched trenches. Details of the Ge layer grown on SRB for the STI last approach can be found in [24]. A thin Ge layer implies a compressive stress into the channel [25], which may boost the p-channel device performance. Therefore, in both processes the Ge layer thickness is smaller than 30 nm .

Methodology

Split CV is employed in this study; it is an important evaluation tool that allows us to extract the effective carrier mobility. This technique is based on the measurement of the linear drain current (I_{DS}) and gate-to-channel capacitance (C_{GC}) versus gate voltage (V_{GS}).

The I_{DS} in the linear regime, where the absolute value of drain voltage ($|V_{\text{DS}}|$) is much lower than the overdrive gate voltage ($V_{\text{GT}} = V_{\text{GS}} - V_{\text{T}}$), can be calculated as outlined in equation (1). The current–voltage (I – V) curves were measured from accumulation to inversion, stepping the gate voltage by 20 mV and a fixed V_{DS} value of -50 mV . All I – V measurements were obtained from an HP 4146 C—Semiconductor Device Parameter Analyzer.

$$I_{\text{DS}} = \mu_{\text{eff}} \frac{W_{\text{eff}}}{L} Q_{\text{INV}} V_{\text{DS}} \quad (1)$$

where μ_{eff} is the effective carrier mobility, W_{eff} is the effective channel width (two times the fin height added to the fin width), L is the channel length and Q_{INV} is the inversion charge density. The latter is calculated as in equation (2) [26]; C_{OX} is the oxide capacitance density

$$Q_{\text{INV}} = C_{\text{OX}} (V_{\text{GS}} - V_{\text{T}}) \quad (2)$$

Figure 3 presents the normalized drain current as a function of gate voltage for strained Ge STI first and last pFinFETs from room temperature down to 77 K .

The inversion charge density can also be obtained by integrating the gate-to-channel capacitance from V_{T} to a voltage value in strong inversion, as in equation (3) [26]. The CV measurement was carried out with an Agilent E4980A high frequency CV meter, where the ac signal had a frequency of 1 MHz . Concerning the dc one, the gate voltage has been stepped by 20 mV from inversion to accumulation regime.

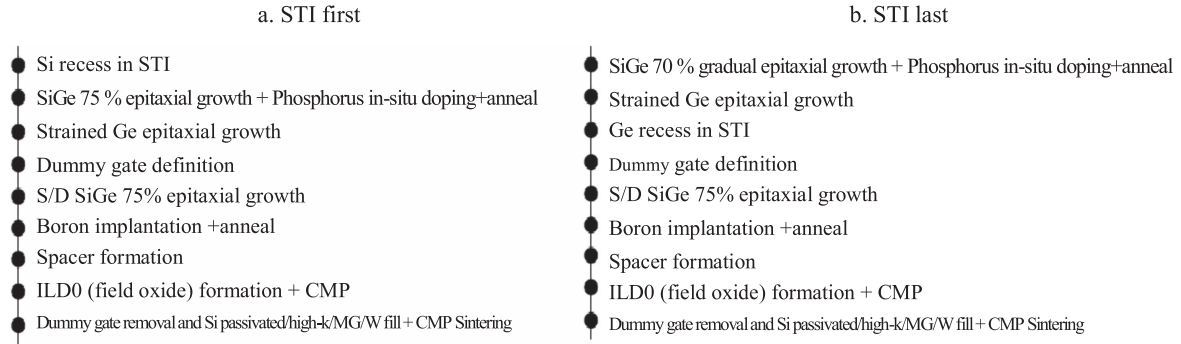


Figure 2. Basic process flow description of the Ge pFinFETs for both STI processes in this work.

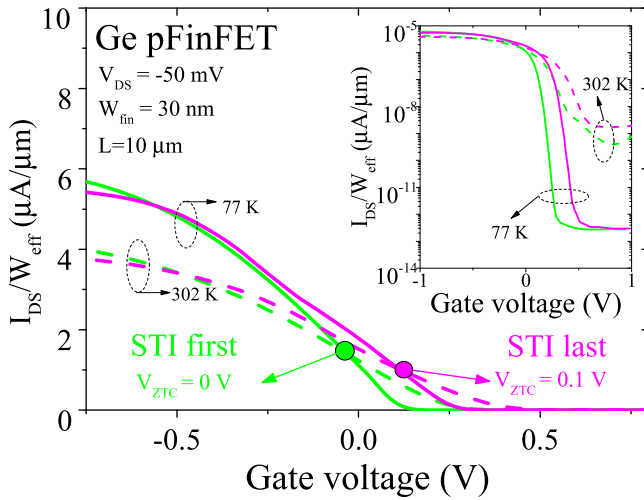


Figure 3. Normalized drain current as a function of gate voltage for STI first and last sGe pFinFETs, from room temperature down to 77 K for a channel length of 10 μm and fin width of 30 nm.

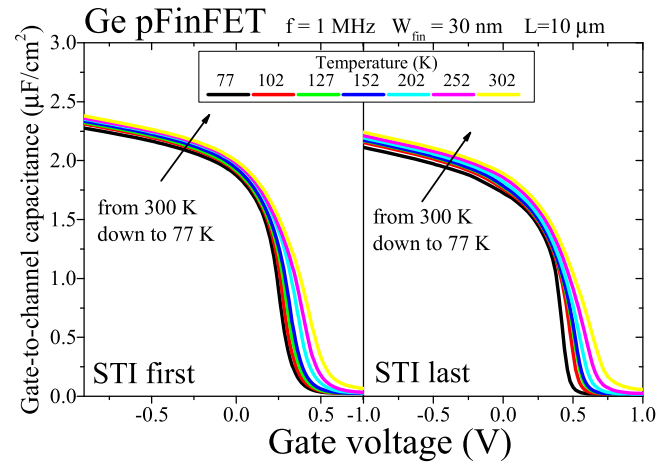


Figure 4. Normalized gate-to-channel capacitance as a function of gate voltage at inversion regime for STI first and last processes, from room temperature down to 77 K for a channel length of 10 μm and fin width of 30 nm.

Table 1. Main device dimensions for both STI processes.

	STI first	STI last
$\text{Si}_{1-x}\text{Ge}_x$	$x = 75\%$	$x = 70\%$
Gate stack	0.7 nm SiO_2 + 2.5 nm HfO_2	1 nm SiO_2 + 1.8 nm HfO_2
Metal gate	5 nm TiN + W	
W_{fin} (nm)	20 nm to 100 nm (planar-like)	
H_{fin} (nm)	20	30
L (μm)		10
Fins in parallel		4
$\text{Si}_{1-x}\text{Ge}_x$ doping concentration (cm^{-3})		5×10^{18}

Moreover, the high output was connected to the gate contact, while the low one was attached to drain and source contacts

$$Q_{\text{INV}} = \int C_{\text{GCD}} dV. \quad (3)$$

Figure 4 shows the gate-to-channel capacitance as a function of gate voltage for sGe STI first and last pFinFETs from room temperature down to 77 K.

Figure 5 depicts the inversion charge as a function of voltage for strained STI first and last processes at 77 K. According to equation (2), the slope of figure 5 represents the C_{OX} value, allowing the extraction of the oxide thickness

(t_{OX}), normally called the capacitance equivalent thickness (CET) with the t_{OX} being obtained from a CV curve in the inversion regime. Moreover, the oxide capacitance density is given by the oxide permittivity (ϵ_{ox}) over the t_{OX} ratio, where SiO_2 has been taken as the oxide material in order to extract the CET values. Figure 5 noticeably shows that the STI first process presents a thinner CET compared to the STI last one.

The combination of equations (1) and (3) allows us to determine the effective carrier mobility, as outlined in (4) [26]

$$\mu_{\text{eff}} = \frac{I_{\text{DS}}}{V_{\text{DS}}} \frac{1}{Q_{\text{INV}}} \frac{L}{W_{\text{eff}}}. \quad (4)$$

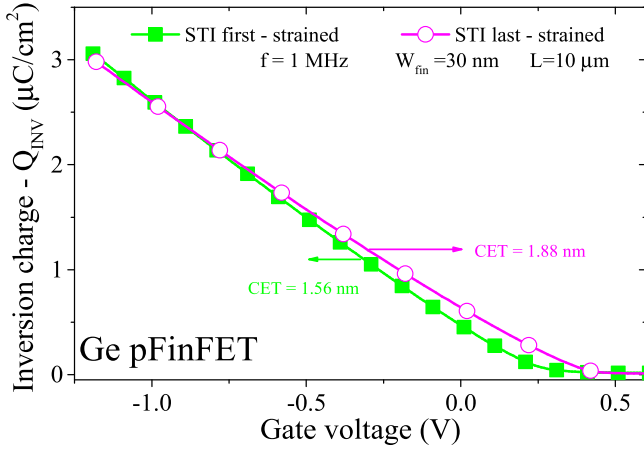


Figure 5. Inversion charge density as a function of gate voltage for STI first and last processes at 77 K for a channel length of 10 μm and fin width of 30 nm.

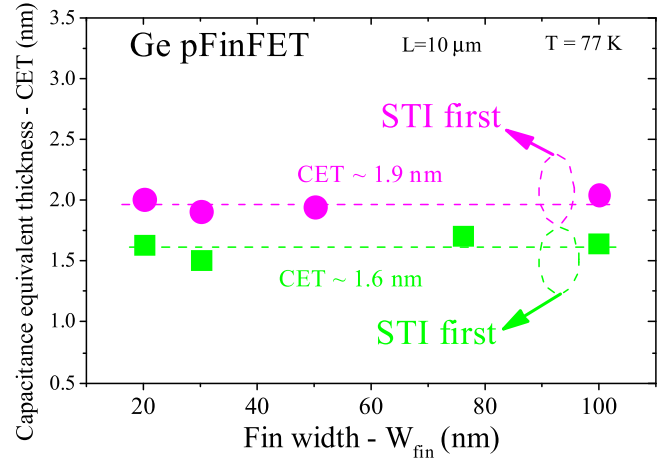


Figure 7. CET as a function of fin width for STI first and last processes at 77 K for a channel length of 10 μm .

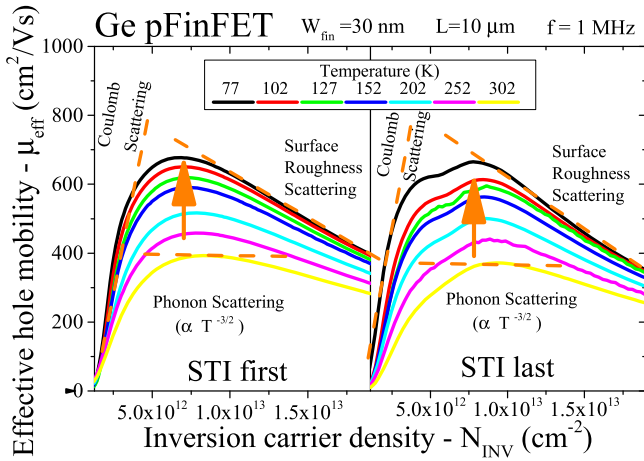


Figure 6. Effective hole mobility as a function of inversion carrier density for STI first and last processes from room temperature down to 77 K for a channel length of 10 μm and fin width of 30 nm.

Figure 6 presents the effective hole mobility as a function of inversion carrier density for strained STI first and last processes at room temperature down to 77 K.

Results

Figure 7 presents the CET as a function of fin width for both STI first and last processes at low temperature. The fact that there is no clear gate width dependence demonstrates a reasonably uniform gate dielectric layer around the fin for both evaluated processes. In other words, there is a conformal gate stack around the fin, both in the top plane and at the (110) sidewalls. This demonstrates a good processing control and the uniformity of the gate stack formation. Moreover, the STI first approach has a thinner CET layer compared with STI last one.

Figure 8 depicts the peak of the effective hole mobility (μ_{eff}) as a function of fin width at low temperature. The mobility for the STI first approach is fin width-independent,

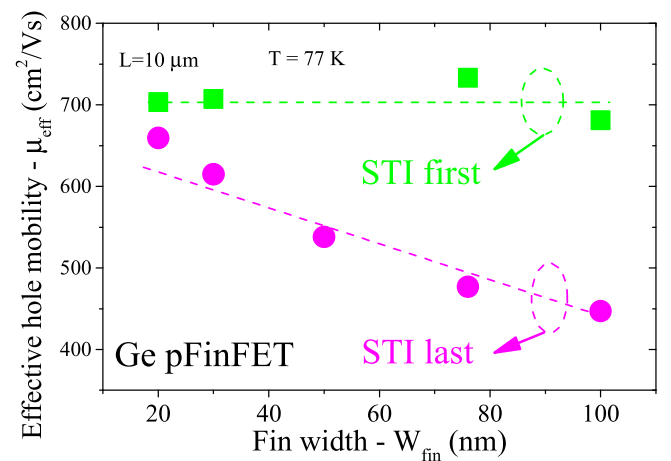


Figure 8. Peak of the effective hole mobility as a function of fin width for STI first and last processes at 77 K for a channel length of 10 μm .

as already presented in [27] at room temperature. On the other hand, for STI last the μ_{eff} is clearly fin width-dependent, revealing that there is a strong sidewall contribution, since the narrower the fin, the stronger is the electrostatic control inside the fin by the sidewall [28]. Additionally, the low-field hole mobility value for the $\langle 100 \rangle$ plane is inferior to the $\langle 110 \rangle$ one [29]. In FinFET devices, $\langle 100 \rangle$ is found on top of the fin and $\langle 110 \rangle$ at the sidewalls.

Figure 9 shows the peak of the effective hole mobility and the effective hole mobility at $N_{\text{INV}} 5 \times 10^{12} \text{ cm}^{-2}$ as a function of temperature, ranging from room temperature down to 77 K, for both STI first and last processes. The increase of the peak mobility indicates that the phonon scattering mechanism is strongly reduced as the temperature decreases [30]. Additionally, the effect of the compressive strain becomes obvious at lower temperature, resulting in μ_{eff} boosting [31]. In contrast, at room temperature, the μ_{eff} of $400 \text{ cm}^2 \text{ V s}^{-1}$ for the sGe pFinFETs studied here is similar to the effective hole mobility found for pFinFETs fabricated in relaxed Ge layers. Clearly, one has to study the mobility at

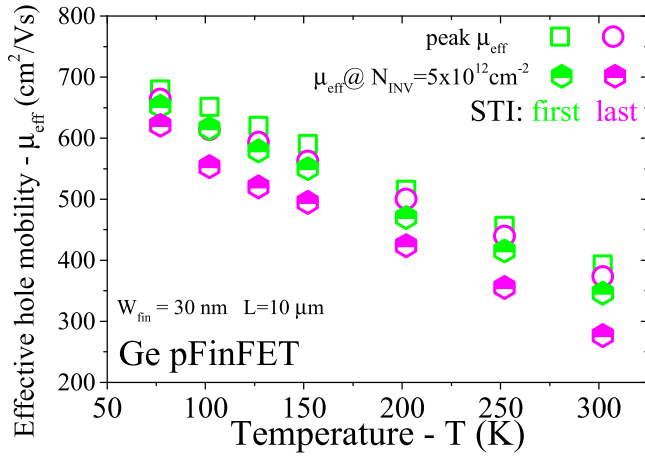


Figure 9. Peak of the effective hole mobility and μ_{eff} at $N_{\text{INV}} = 5 \times 10^{12} \text{ cm}^{-2}$ as a function of temperature for STI first and last processes for a channel length of $10 \mu\text{m}$ and fin width of 30 nm .

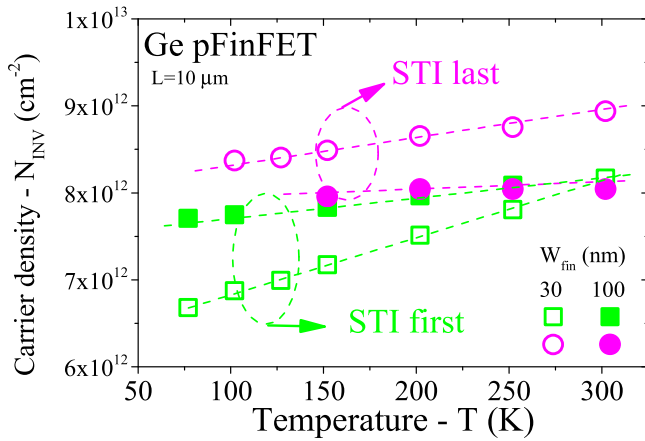


Figure 10. Inversion carrier density as a function of temperature for STI first and last processes for a channel length of $10 \mu\text{m}$ and fin width of 30 nm and 100 nm , respectively.

lower T in order to reveal the impact of the compressive strain.

Figure 10 presents the inversion carrier density at the peak of the effective hole mobility as a function of the temperature. The STI last approach shows a rather weak variation of N_{INV} as the temperature goes down to 77 K for both narrow and planar-like devices. On the other hand, the STI first approach shows a N_{INV} variation even for wide devices and it significantly increases for narrow ones, meaning that the peak of the effective mobility shifts towards a lower inversion carrier density owing to the Coulomb scattering mechanism [32].

Discussion

The drain current difference between STI first and last in figure 3 is associated to two facts: the hole mobility and the oxide thickness. The latter is thinner for STI first pFinFETs, as presented in figure 7; this results in higher C_{OX} values, which contributes to a superior drain current, as observed in

figure 3. Additionally, the STI first approach also presents a higher hole mobility, as shown in figures 6 and 8; this mobility further increases the drain current.

Closer inspection shows that the STI last pFinFETs are susceptible to the presence of a hump preceding the true peak in the effective mobility, as presented in figure 6; however, this is not clearly observed at room temperature. This could be explained by considering a Ge over-recess during the fin formation that results in a thinner layer of the SiGe SRB as part of the channel at the bottom of the fin, indicating a critical fabrication step that should be further optimized. The clear width dependence for the STI last sGe pFinFETs could be explained by several factors. It could point to the impact of the TDs on the hole mobility, which should increase with wider devices, resulting in a higher probability to contain a number of threading defects, which can act as scattering centers [32]. In addition, for narrower fins, the contribution of the (110) sidewalls to the transport over the top surface becomes more pronounced. Finally, the presence of compressive strain on the effective hole mobility could also show up a width dependence, where the biaxial strain for wide transistors becomes more uniaxial for narrow ones, by the relaxation of the strain in the transverse (width) direction. In principle, uniaxial compressive strain is more effective in hole mobility boosting than biaxial strain. In this context, the absence of a width dependence of μ_{eff} for the STI first case in figure 8 is rather unusual and points to a clearly different dominant scattering mechanism(s) compared with STI last.

Concerning the scattering mechanisms determining the hole mobility, the STI last approach shows that the phonon scattering remains present even at low temperature. On the other hand, the mobility behavior of the STI first devices demonstrates that it is strongly influenced by another mechanism, i.e. Coulomb scattering. The latter has already been derived from the low-frequency noise behavior, reported elsewhere [33]. The thicker layer of the high- κ dielectric material (HfO_2) might contribute to the Coulomb scattering mechanism [34] for the STI first approach, since charged traps into the HfO_2 can affect the Ge/ SiO_2 interface, facilitating the Coulomb scattering. At high electric fields—in other words, an inversion carrier density higher than $1.5 \times 10^{13} \text{ cm}^{-2}$ —the surface roughness scattering can be observed for both STI processes, where the effective mobility is pinned at one value for different temperatures, as is clearly seen in figure 6 at low temperatures, i.e. below 127 K .

Conclusion

Low temperature split CV studies are shown to be an important tool that allow the evaluation of the effective mobility, strain effect and scattering mobility mechanisms for Ge pFinFETs fabricated with both STI first and last process flows. Furthermore, the low temperature study gives important feedback about the fabrication process, since at room temperature it is not possible to detect, for instance, an over-recess issue of the Ge layer in the STI last process.

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