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Middle Electrode in a Vertical Transistor Structure Using an Sn Layer by Thermal Evaporation

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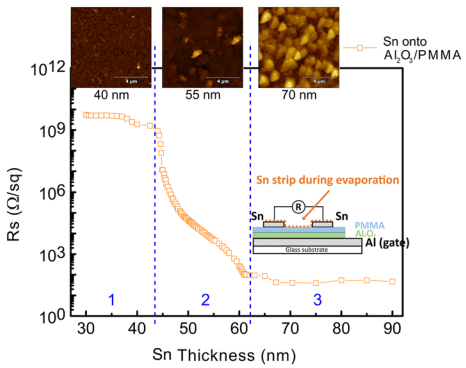
Abstract

We report a process for performing the middle electrode for a vertical field effect transistor (VOFET) by the evaporation of a tin (Sn) layer. Bare aluminum oxide (Al_2O_3), obtained by anodization, and Al_2O_3 covered with a polymethylmethacrylate (PMMA) layer were used as the gate dielectric. We measured the electrical resistance of Sn while the evaporation was carried out to find the best condition to prepare the middle electrode, that is, good lateral conduction associated with openings that give permeability to the electric field in a vertical direction. This process showed that 55 nm Sn thick is suitable for use in a VOFET, being easier to achieve optimal thickness when the Sn is evaporated onto PMMA than onto bare Al_2O_3. The addition of a PMMA layer on the Al_2O_3 surface modifies the morphology of the Sn layer, resulting in a lowering of the threshold voltage. The values of threshold voltage and electric field, $V_{TH} = -8$ V and $E_{TH} = 354.5$ MV/m respectively, were calculated using an Al_2O_3 film 20 nm thick covered with a 14 nm PMMA layer as gate dielectric, while for bare Al_2O_3 these values were $V_{TH} = -10$ V and $E_{TH} = 500$ MV/m.

Graphical Abstract



Keywords Vertical transistor · Permeable electrode · AL_2O_3/PMMA · Thermal evaporation

1 Introduction

Interest in vertical organic transistors has increased significantly during recent years and offered good potential for the development of large area printed electronics processed by solution [1]. These devices are formed by thin films stacked vertically where the current flows perpendicularly to the films. The main advantages of vertical transistors are their high output current, easy manufacture, low voltage and

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high frequency operation. There are several types of vertical transistor, the permeable base transistor (PBT), static induction transistor (SIT) and vertical field effect transistor (VFET) standing out. While they have different operational principles, all possess at least two common features: (i) the charge transport in these devices takes place in a vertical direction, i.e. perpendicular to the film, the channel length being given by the thickness of the semiconductor films; and (ii) an intermediate electrode is required permeable to the electric field to enable drain-source current modulation. It is worth emphasizing that the nomenclature, characteristics and function of the layers depend on the transistor type, but, for all of them, the crucial point is the middle electrode.

Different approaches to creating a permeable electrode can be found in the literature. Some groups have demonstrated the possibility of using a highly ordered nanometer pore structure, performed by laser holographic photolithography [2]. Tessler et al., proposed some alternatives for obtaining the patterned electrode using block copolymer nanotemplates [3]. These methods are important for good control of pore size, necessary for theoretical investigation and modeling of the current modulation [4], however, the process can be expensive. In some approaches, polystyrene spheres are strewn onto the substrate followed by the electrode deposition and the removal of the spheres, resulting in patterned openings [5]. Another possibility is the deposition of an organic material blend followed by the etching of one of its components, for example, the deposition of doped PANI film mixed with polyester followed by the etching of the polyester [6]. Porous materials, or those not forming a continuous film, such as carbon nanotube and metallic nanowires, can also be used. For example, excellent control of electrode porosity is achieved by changing the density of single wall carbon nanotube networks [7, 8]. Also, metallic nano-wires originating from a variety of metals (for instance copper, silver, gold) are attractive, mainly because of their low sheet resistance [9, 10]. Graphene is another material that has been used as a permeable electrode in VFETs, for both experimental and theoretical study [11, 12].

Apart from the approaches referred to before to produce porous electrodes, some authors use simple strategies of metal evaporation in one-step. One example in this is the first organic VFET, proposed by Ma and Yang, in which a copper(20 nm)/aluminum(10 nm) source electrode is used, evaporated onto a lithium fluoride layer [13]. A permeable electrode was also obtained by co-evaporation of aluminum with pentacene, where the ratio of the two materials defines the pores size [14]. In this process, the aluminum evaporation is suspended and the pentacene continues being evaporated to form a continuous semiconductor film. Another possibility is to co-evaporate aluminum and calcium followed by thermal annealing in air. The calcium is oxidized during the annealing, leaving regions of insulating oxide that gives the field permeability characteristics [15]. Finally, Hummelgen et al. report a VOFET prepared using a single tin (Sn) layer as the intermediate electrode. The use of Sn, when the optimal deposition conditions are reached, simplifies the intermediate electrode preparation procedure due to the grain growth characteristics of this material [16].

In this work, we report a simple strategy of controlled evaporation of Sn in one single step, to make the deposition of the middle electrode in a vertical organic field effect transistor (VOFET). The Sn was evaporated onto bare Al_2O_3, and Al_2O_3 covered with a PMMA layer, forming a metal-insulator-metal structure. The addition of PMMA changes the middle electrode morphology improving the characteristics of the device. Poly(3-hexylthiophene), P3HT, a solution-processed semiconductor, was also used as the active layer.

2 Experimental Procedure

For the manufacture of the devices, first of all an Al layer ~ 150 nm thick was evaporated onto cleaned glass substrate delimited by a shadow mask, forming a strip 3 mm × 20 mm. The evaporation procedure was carried out using an Edwards auto 306 thermal evaporator. Substrate temperature was kept constant (300 K) in all experimental runs. The gate dielectric was obtained by anodization of the Al layer, growing an Al_2O_3 film 20 nm thick. The basic structure for the VOFET, which are the gate electrode and dielectric layers (Al/Al_2O_3), named capacitive cells, was made using this procedure. The steps taken to perform the anodization process were: (i) an electrolytic solution was prepared dissolving 0.3 g of tartaric acid in 10 ml of ultrapure water (Milli-Q) and 50 ml of ethylene glycol was added. The pH was set to ~ 8 adding some drops of a low-concentration ammonium hydroxide solution; (ii) the substrate with the Al film and a gold electrode was immersed in a home-made electrochemical cell containing the electrolytic solution; (iii) a constant current of 0.8 mA/cm^2 was applied and the voltage was recorded; (as the oxide layer grows, the voltage increases according to the anodization factor, $f_a = {}^{d}/_{V_a}$; that adopted here was as 1.2 nm/V); (iv) when the thickness reaches the desired value (20 nm), the voltage is held constant for 120 s, improving the uniformity of the oxide.

Two gate dielectrics were used, the first was bare Al_2O_3, and the second was Al_2O_3 covered with a thin PMMA layer (Al_2O_3/PMMA). The methyl ethyl ketone solution of PMMA (10 mg/ml) was spun with 4000 rpm for 60 s. In the next step, the middle electrode, used as "source" in this work, was formed by evaporating Sn onto the dielectrics layer through a shadow mask. Different evaporation rates were used: (i) 0.5 Å/s between beginning and 4 nm; (ii) 1 Å/s, between 4

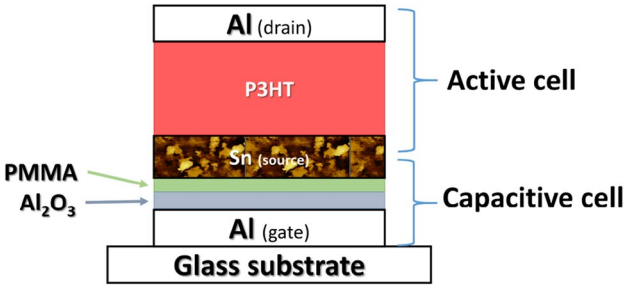

Fig. 1 Diagram illustrating the VOFET. As seen in the Figure, the capacitive and active cells are formed by Al-Al_2O_3-PMMA-Sn and Sn-P3HT-Al, respectively. The Sn source electrode, deposited by evaporation, is represented by an AFM image

and 10 nm; and 2 Å/s, between 10 and 30 nm. At this point the basic structure of the device, named capacitive cell, was concluded. For the solution-processed semiconductor layer, regioregular P3HT (Sigma-Aldrich) was used. A chloroform solution of P3HT (15 mg/mL) was spun onto the Sn layer, at 700 rpm for 60 s. After the deposition of P3HT, the samples were submitted to annealing at 100 °C in a dark vacuum for the removal of residual solvent. The manufacture of the device was completed by the evaporation of ~ 80 nm Al thick at the top, forming the "drain electrode". The active area of the transistor, determined by the region where gate, source and drain overlap, is 9 mm^2. Figure 1 shows the diagram representing the device.

The transistor electrical characteristics were carried out using a Semiconductor Parameter Analyzer (Keithley 4200), inside a vacuum chamber with 10^{-4} kPa, in the dark. The surface morphology was characterized using a Nanosurf atomic force microscope (AFM), operating in tapping mode.

3 Results and Discussion

3.1 Analysis of Sn Layer Evaporation

Figure 2a shows the sheet resistance (R_S) against Sn film thickness, measured during the film deposition onto a glass surface (triangles), Al_2O_3 (circles) and Al_2O_3/PMMA (squares). The thickness of the Sn layer was estimated by using a quartz crystal microbalance and, simultaneously, the electrical resistance was measured using an electrometer Keithley 617. To facilitate the measurements of the electrical resistance, two Sn strips (3 mm × 10 mm) separated by 7 mm were previously evaporated onto the substrate, as shown in Fig. 2b, where the electrometer is connected. While the Sn evaporation process was being carried out, the resistance was measured in a 3 mm × 10 mm strip perpendicularly positioned to the first strips, as indicated by the orange dotted line in Fig. 2b.

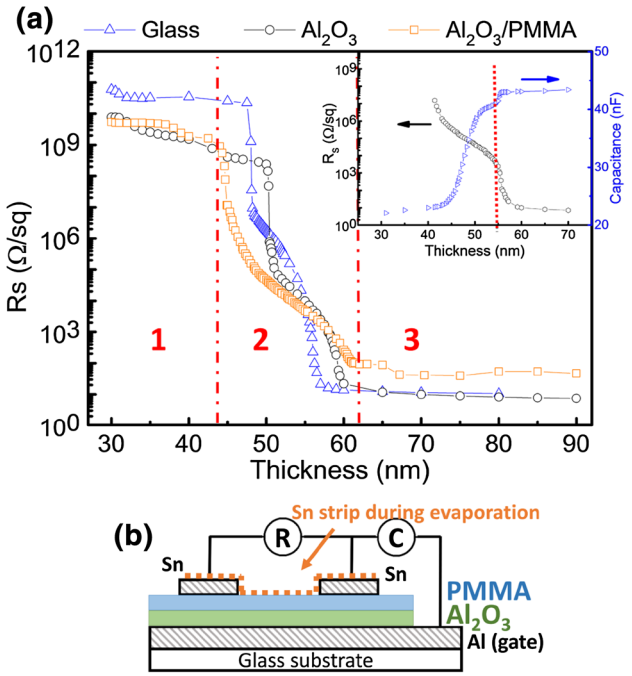

Fig. 2 **a** Curve of sheet resistance (R_S) versus thickness, during Sn evaporation, onto glass, bare Al_2O_3 and Al_2O_3/PMMA. Inset: another curve of sheet resistance and capacitance, during Sn evaporation onto Al_2O_3/PMMA. **b** Diagram representing lateral view, to illustrate the samples utilized for the resistance and capacitance measurement

Similar to the study of in situ measurements of the film resistance during deposition of metallic thin films by Evans and Xu [17], the behavior shown in Fig. 2a can be explained considering the theory of nucleation and growth of thin films [18]. This mechanism takes place in the vacuum evaporation process, and is well known that substrate temperature is an important factor [19]. However, as shown by Li et al. [20], surface morphology of Sn thin-film obtained by sputtering can be controlled only modulating the deposition parameters. Here, in a similar approach, we focused in Sn film thickness onto different substrate. The R_S curves in Fig. 2a have a similar shape for all surfaces, showing three main regions, as approximately indicated in the Figure. At region 1, the Rs remains almost constant, exhibiting the greatest R_S value (~ 10^{10} Ω/sq). The deposition is not uniform, instead, a small amount of material is sprinkled onto the surface and only isolated clusters are formed at the beginning of the process. The resistance then prevails in region 1 of the insulator surface (glass, Al_2O_3 or PMMA). In region 3, the resistance decreases by about 9 orders of magnitude, from values in the order of 10^{10} ~ 10^{11} to ~ 10^1 Ω/sq, as the thickness changes from about 45 to 60 nm. The thickness of the Sn film in region 1 and region 3 is not adequate to fabricate the source electrode of VOFET. In the first, the resistance is too high to be used as an electrode. In the last it is very low, but the film is thick, completely shielding the gate electric field.

Thus, to obtain the source electrode, it was necessary to use a thickness in the intermediate region, before the evaporation had covered the entire surface, so open areas remained in the Sn electrode. The exact points where region 2 begins and ends depends on the substrate surface characteristics, this region being broader for evaporation on the Al_2O_3/PMMA than onto bare Al_2O_3. At the beginning of region 2, the clusters start to percolate, shooting down the resistance, and this finishes when the surface is completely covered.

A better analysis of this process can be obtained performing a capacitance measurement simultaneously with the resistance, both during evaporation. The setup for this experiment is shown in Fig. 2b, c. The inset of Fig. 2a shows curves of resistance and capacitance measurements. The most important information of this measurement is the indication of the thickness when the evaporation covered the entire surface, as indicated by the dashed line in the inset. Capacitance does not increase after this point, because the whole area is already covered, but resistance continues decreasing because the film is thickening.

It can be concluded, based on results showed in Fig. 2, that thickness of about 55 nm is suitable for the manufacture of source electrode for VOFET. The advantage of this approach is the easy determination of the optimum thickness of the Sn layer necessary carry out the measurement of resistance and capacitance during evaporation, at least once for each substrate. As already discussed, the Sn layer has openings which are permeable to the electric field situated between the beginning of percolation and the total coverage, for the intermediate value. Analyses of AFM images give better support for this statement. Figure 3 shows AFM images of bare Al_2O_3 (a and b) and Al_2O_3/PMMA (c and d) surfaces. Figure 3b, d shows a three-dimensional view for a better spatial comprehension. The Al_2O_3 films grown by anodization has a quite irregular surface, that depend on the fabrication parameters [21]. The roughness is reduced by covering the Al_2O_3 film with a PMMA thin layer, as can be seen in Fig. 3, from which were obtained a root mean square (RMS) surface roughness of 24.2 and 3.6 nm for bare Al_2O_3 and Al_2O_3/PMMA, respectively.

Figure 4 shows the AFM images (10 μm × 10 μm) of Sn layer evaporated onto bare Al_2O_3 and Al_2O_3/PMMA surfaces. The thickness of the evaporated Sn electrodes, chosen for the AFM analyses, were 40, 55 and 70 nm, taking a representative sample of each region illustrated in Fig. 2. For an Sn film 40 nm thick, the image shows the formation of small clusters onto both substrates. The very rough Al_2O_3 surface (Fig. 3a, b) was smoothed by the Sn layer, decreasing the roughness to 12.2 nm. The evaporation of a 40 nm Sn film onto Al_2O_3/PMMA results in a

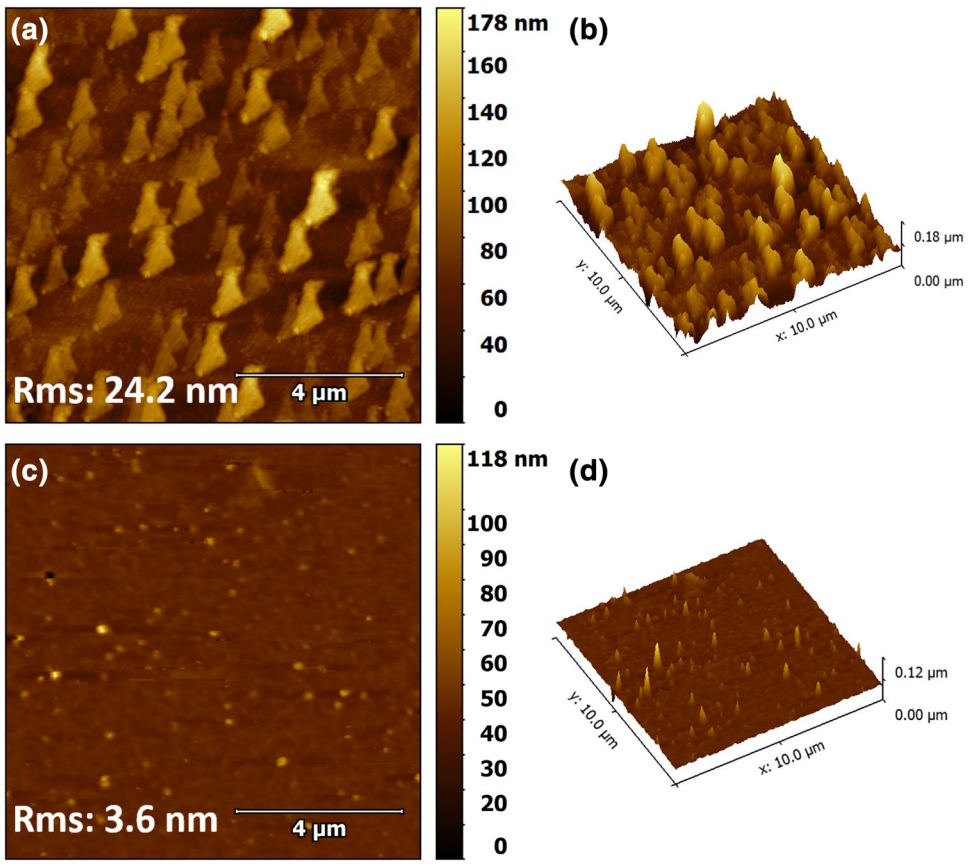

Fig. 3 AFM imagens of bare Al_2O_3 (**a** and **b**) and Al_2O_3/PMMA (**c** and **d**), all for 10 μm × 10 μm. Images **b** and **d** shows a 3D view of the surfaces. The roughness value are shown in respective insets

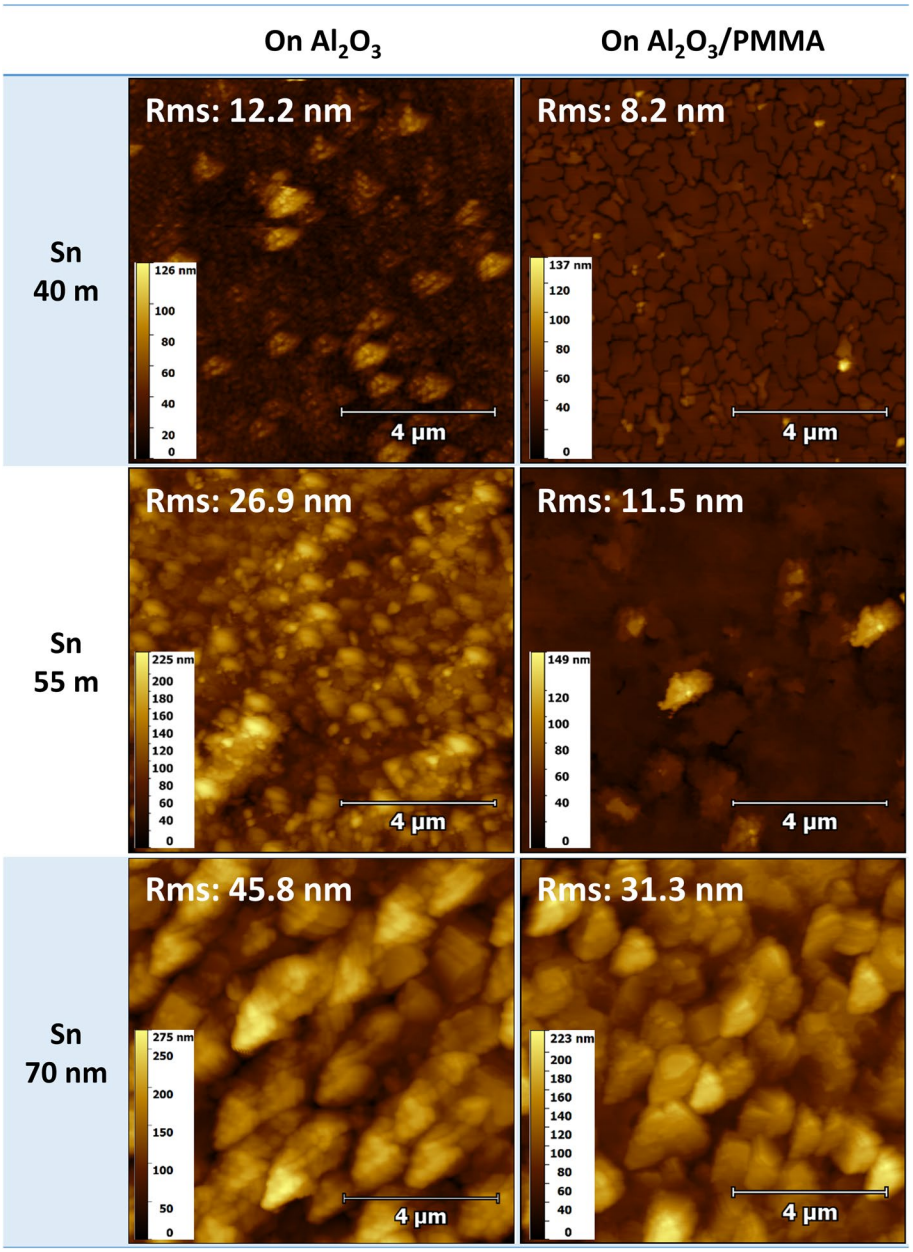

Fig. 4 AFM images of Sn layer onto bare Al_2O_3 and Al_2O_3/PMMA, for 40, 55 and 70 nm, representing each region of resistance curve in Fig. 2. Area of 10 µm × 10 µm. Values of surface roughness are indicated in the upper left corner of each image

non-continuum film, i.e. the clusters are not yet connected. For the 55 nm Sn thick film, the images show an increase of film roughness for each surface, being lower on the Al_2O_3/PMMA (11.5 nm) than on bare Al_2O_3 (26.9 nm). For the 70 nm Sn thick film, the morphology of both films, on bare Al_2O_3 and PMMA surfaces, are similar and there is no longer dependence on the substrate.

A careful analysis of the AFM image in Fig. 3 was performed using *Gwyddion Software* (not shown here) of the 55 nm Sn thick films, concluding that the Sn clusters coalesce forming a percolated path like a grid. These morphologies are consistent with the resistance curves shown above (Fig. 2) and, in a global view of AFM images, the Al_2O_3/PMMA can be evaluated showing a better condition for obtaining an electrode permeable to electric field.

Figure 4 shows the capacitance versus frequency from 1 to 10^5 Hz for the bare Al_2O_3 and Al_2O_3/PMMA dielectrics sandwiched between two electrodes, forming a metal-insulator-metal (MIM) capacitor. The Al, remaining from the anodization process, was used as the bottom electrode. The upper electrode was performed by Sn metallization 55 and 70 nm thick.

A capacitance of ~ 24 nF would be expected when using bare Al_2O_3 as dielectric in a MIM capacitor for high frequency (> 1 kHz). This estimation was made considering the dielectric constant ~ 7 when the electrodes cover the

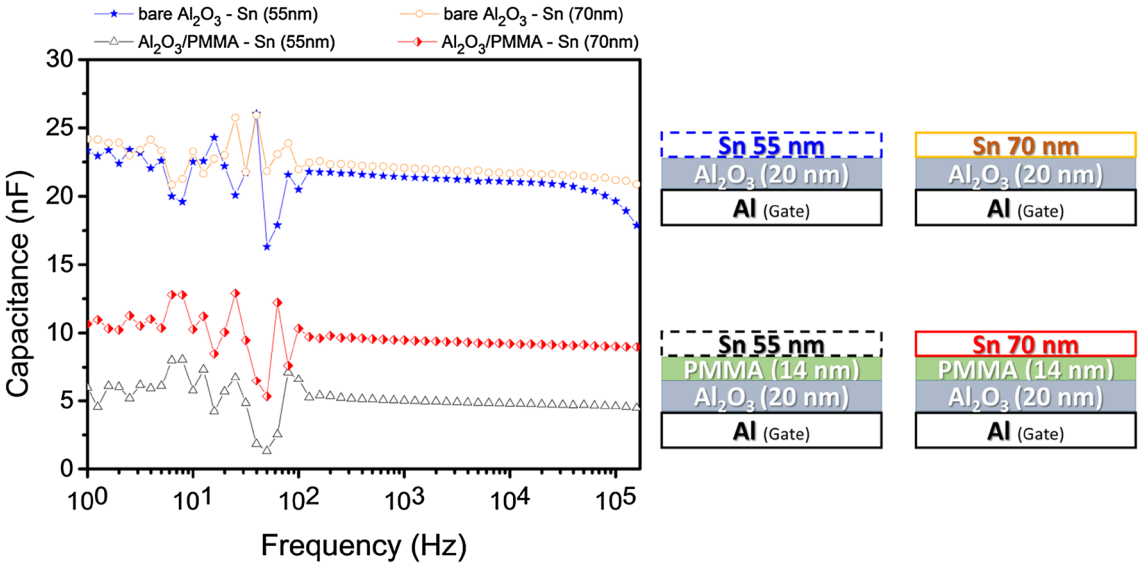

Fig. 5 Curves of capacitance versus frequency, for 55 and 70 nm of Sn, onto bare Al_2O_3 and Al_2O_3/PMMA insulators. These curves are useful in analyzing the covering of the electrode surface. Diagrams on the right side of the curve illustrate each MIM structure used for this measurement

whole surface. In Fig. 5, the capacitance of bare Al_2O_3 is 22.1 and 21.4 nF at 1 kHz for 55 and 70 nm thick Sn electrodes, respectively, which is to say, a value very close to that expected was obtained, meaning that the Sn electrode covered the entire surface. The capacitance for Al_2O_3/PMMA was 9.50 and 5.02 nF for the Sn electrodes with 70 and 55 nm, respectively, which is smaller than for bare Al_2O_3, as the dielectric becomes thicker when PMMA is added. The PMMA thickness can be estimated as 14 nm bearing in mind that the Sn was metalized onto the PMMA to a thickness of 70 nm to cover the whole surface, as observed in the AFM image analyses (Fig. 4). The capacitance for Sn at a thickness of 55 nm is lower than for 70 nm because, in this case, the evaporation does not cover the whole PMMA surface since the dimensions of the sample are the same. As stated, in this case the decrease in the capacitance is originated only by variations on the covering of the surface. Thus, the ratio of the capacitances enables the fill factor (FF) to be determined. The values obtained for the FF were ~ 3 and ~ 47% for bare Al_2O_3 and Al_2O_3/PMMA, respectively.

The combination of electrical measurements (capacitance and resistance) and morphological characterization (AFM images) provide an interesting way to study the Sn electrode. The results discussed above show that an Sn layer of 55 nm thickness is the proper choice for the middle electrode for the VOFET. We will show, in next section, the results of the VOFET using Sn/P3HT/Al stacked on the MIM capacitor of Al/Al_2O_3/PMMA/Sn will be shown, where the Sn electrode with a thickness of 55 nm was deposited by evaporation as discussed in this section.

3.2 Transistor Electrical Characteristics

Figure 6 shows the output characteristic curves for the VOFET using a capacitive cell based on Al_2O_3 topped by the active cell with P3HT. Figure 6a shows the curves for a VOFET using bare Al_2O_3, the thickness layers being specified inset. The contact Sn-P3HT and Al-P3HT are both hole blockers, so there is no charge injection in the semiconductor without bias in the gate, a current modulation for gate bias being observed from − 12 V. Figure 6b shows the output curves for the VOFET using Al_2O_3/PMMA as the gate dielectric where the modulation for the gate bias starts around − 8 V. The current modulation can be seen more clearly in the insets of Fig. 6a, b, where the curves are plotted with the current in log-scale.

The results above (Fig. 6) show that the current modulation seems easier for Al_2O_3/PMMA than bare Al_2O_3. The analyses of the electric field at the lower interface of P3HT (through the PMMA layer) can be valuable for evaluating the effect of the PMMA layer on the VOFET. The electric field at the PMMA layer has to overpass the Sn electrode coming into the P3HT layer. The value of the electric field at this interface, in this work named E_i, can be useful for comparing both devices. While the value of E_i for bare Al_2O_3 is obtained directly, the value of E_i for PMMA can be obtained by

$$E_i = \frac{\varepsilon_1}{\varepsilon_2 d_1 + \varepsilon_1 d_2} V$$

where ε_1, d_1, ε_2 and d_2 are the dielectric constant and thickness for the Al_2O_3 and PMMA, respectively. The values of E_i correspondent to the threshold voltage is 500 and

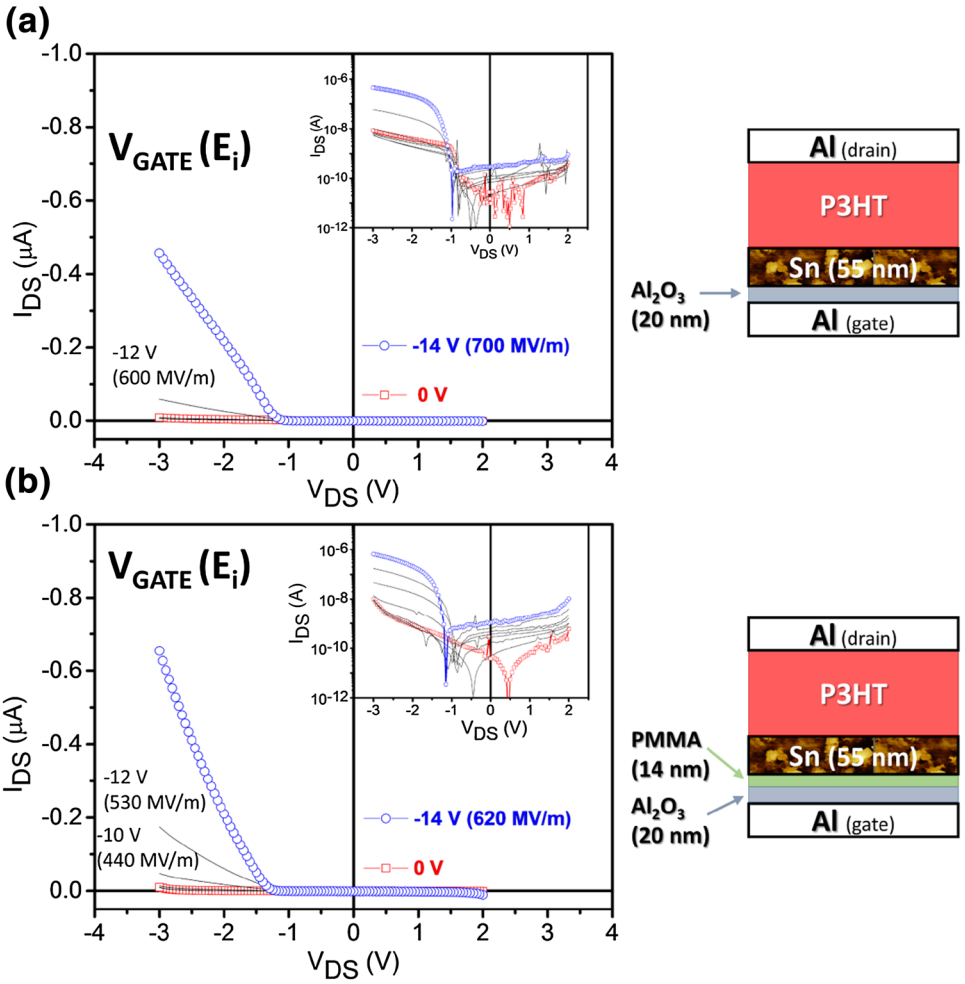

Fig. 6 Output curves for: **a** 20 and 55 nm, for bare Al_2O_3 and Sn, respectively, and **b** 20, 14 and 55 nm, for Al_2O_3, PMMA and Sn, respectively. Inset shows the output curves with current in log-scale. The device diagram for the two output curves are shown on the right side of each curve

Table 1 Comparison between V_{TH} and E_{TH} of the VOFETs, when using bare Al_2O_3 and Al_2O_3/PMMA as dielectrics layer

Transistor	Dielectric layer	Thickness (nm)	V_{TH} (V)	E_i (MV/m)
I	Al_2O_3	20	− 10	500
II	Al_2O_3/PMMA	34	− 8	354.4

354.4 MV/m for bare Al_2O_3 and for Al_2O_3/PMMA VOFETs. This value was calculated considering the date shown in Table 1. The field needed to start the current modulation is about 30% lower when the Al_2O_3 is covered by PMMA. In addition, it can be seen that the drain current is bigger for the Al_2O_3/PMMA VOFET when all other parameters are kept constant. For purposes of comparison, the value of E_i correspondent to V_G is shown in parentheses beside each curve in Fig. 6. Figure 7 shows the transfer curves for both devices, extracted directly from the output curves of Fig. 6, but E_i was used instead of gate voltage (V_G). The transfer curves for Al_2O_3/PMMA showed a lower threshold field and a bigger drain current than bare Al_2O_3. The red

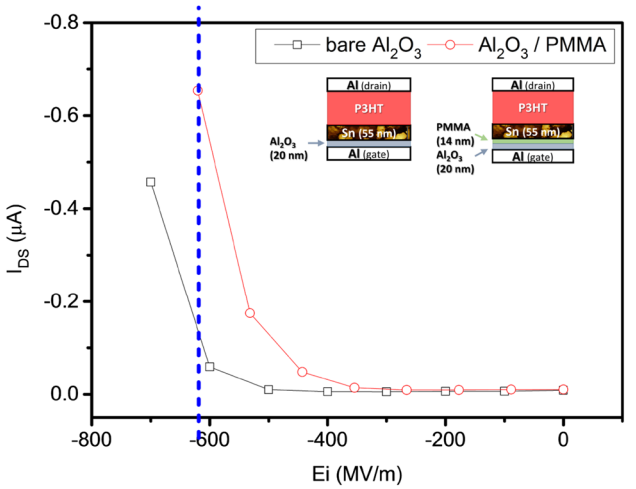

Fig. 7 Transfer curve for VOFET using bare Al_2O_3 (squares) and Al_2O_3/PMMA (circles) as the insulating layers. It can be observed that the use of the PMMA layer improves the performance of the devices

dashed line in Fig. 7 highlights the difference of current at 620 MV/m between the two devices. This is almost one order of magnitude.

Some electrical characteristics shown above should be highlighted. There is not current saturation in the output curves as would be expected for a VOFET [22]. Unfortunately the calculation of P3HT mobility was not possible, because the V_{DS} was not large enough to ensure the space-charge-limited-charge (SCLC) regime required for the *Ben-Sasson* approach [4, 23]. The value of drain current was lower than expected for a VOFET. For this reason, it is worth mentioning that P3HT is not a good semiconductor because the mobility in a direction perpendicular to the surface is about two orders of magnitude lower than in the horizontal direction [24]. However, our results confirm that covering the Al_2O_3 with PMMA is beneficial because it enables an Sn electrode permeable to the electrical field to be obtained in just one evaporation procedure.

It has been reported that adding a PMMA layer, a low-k insulator, covering the Al_2O_3 can modify the organic field effect transistor (OFET) performance mainly by improving the mobility because of decreasing the insulator roughness [25, 26]. In this work, it seems that the main effect is the modification in Sn electrode morphology leading to a bigger FF. Of course, the VOFET can be prepared with a bigger FF using bare Al_2O_3 but it is much more difficult to control the process. In addition, it is important to consider that the roughness of PMMA is much lower than that of Al_2O_3, being 24.2 and 3.6 nm, respectively (Fig. 3). As the roughness produces a great decrease of the conductivity of a metallic film deposited on it, when the conductivity reaches a value suitable for use as an electrode, the surface is already almost covered. The main PMMA role is to smooth the Al_2O_3 surface to the range in which optimal thickness is achieved, showing good resistance and openings to allow electric field permeability, which is wider for Al_2O_3/PMMA than for bare Al_2O_3, easing the control of the thickness during the metallization.

4 Conclusion

A VOFET manufactured using a capacitive cell formed of Al/Al_2O_3/PMMA/Sn topped by an active cell of Sn/P3HT/Al has been demonstrated. For this device, the most important layer is the middle electrode, which has to be permeable to an electric field. It has been shown in this work that the current modulation by gate bias depends on Sn electrode morphology, which is modified by the characteristics of the substrate where the deposition is done. The most important factor is determining the appropriate thickness, which, for this device, was 55 nm. The addition of one layer of PMMA onto an Al_2O_3 surface is an important procedure to improve the morphology of the Sn electrode deposited on it. This statement is based on the fact that the roughness of the Sn film decreases and the fill factor (FF) increases, becoming more suitable for working as electrode permeable to an electric field. For this reason, the results obtained confirm that the deposition of one layer of PMMA onto Al_2O_3 improves the performance of the VOFET. Here, the characteristics of Sn film, forming clusters when evaporated, are combined to with the low surface roughness of the PMMA for obtaining a good middle electrode in only one evaporation procedure.

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