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Separating interface state response from parasitic effects in conductance measurements on organic metal-insulator-semiconductor capacitors

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A simple model is developed for the admittance of a metal-insulator-semiconductor (MIS) capacitor which includes the effect of a guard ring surrounding the Ohmic contact to the semiconductor. The model predicts most of the features observed in a MIS capacitor fabricated using regioregular poly(3-hexylthiophene) as the active semiconductor and polysilsesquioxane as the gate insulator. In particular, it shows that when the capacitor is driven into accumulation, the parasitic transistor formed by the guard ring and Ohmic contact can give rise to an additional feature in the admittance-voltage plot that could be mistaken for interface states. When this artifact and underlying losses in the bulk semiconductor are accounted for, the remaining experimental feature, a peak in the loss-voltage plot when the capacitor is in depletion, is identified as an interface (or near interface) state of density of $\sim 4\times 10^{10}\ \mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$. Application of the model shows that exposure of a vacuum-annealed device to laboratory air produces a rapid change in the doping density in the channel region of the parasitic transistor but only slow changes in the bulk semiconductor covered by the gold Ohmic contact. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2844435]

I. INTRODUCTION

In the early days of silicon technology, small-signal admittance measurements on metal-oxide-semiconductor capacitors proved particularly useful for understanding and improving the properties of the silicon-silicon dioxide interface. For example, capacitance-voltage (C-V) measurements provided a direct measure of the insulator thickness and the doping density profile in the semiconductor, while the frequency and voltage dependences of the loss (conductance/angular frequency) were shown[1] to be very sensitive to the presence of trapping states at the semiconductor-insulator interface. Using these techniques, we[2,3] and others[4] have shown that interface states are also present at the semiconductor/insulator interface of organic metal-insulator-semiconductor (MIS) devices. In some of the measurements reported to date, a common feature in the loss-voltage (G/ω-V) plots is the appearance of a double maximum. The frequency dependence of both peaks was consistent with two distributions of localised states present at the insulator-semiconductor interface.[3] One peak clearly occurred when depletion voltages were applied to the device and could be attributed unambiguously to interface states. However, the second peak occurred in a voltage region in which the device was expected to be in accumulation. In this contribution, we investigate these effects further and show that this "accumulation" peak is an artifact arising from the use of a guard electrode which, nevertheless, is essential for undertaking measurements at the low frequencies necessary to observe interface state effects.

In Sec. III, we present experimental results extending our original study[3] to investigate the effect of laboratory air on the devices. In Sec. IV, we present a theoretical model of the MIS diode which includes the effects of a parasitic MIS field effect transistor (MISFET) formed by the guard ring and the electrode it surrounds. In Sec. V, we present numerical simulations based on the theoretical model which demonstrate the main features of the results presented in Sec. III. Following a short discussion in Sec. VI, we present our conclusions.

II. EXPERIMENTAL

MIS capacitors (Fig. 1) were formed on indium tin oxide coated glass substrates using polysilsesquioxane (PSQ), thermally converted from a spin-coated film of phenylmethylsils-

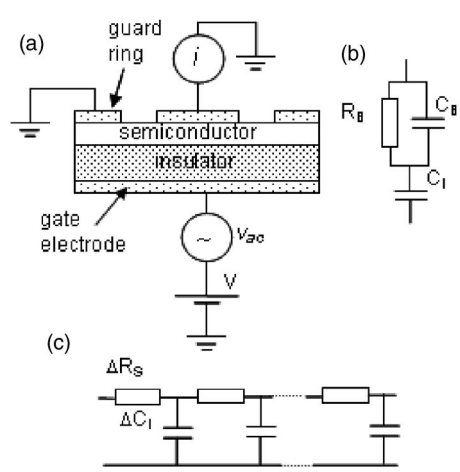

FIG. 1. (a) Cross section through the guarded MIS capacitor structure studied in this work and the configuration used for the admittance measurements. Equivalent circuits of (b) an ideal MIS capacitor in accumulation and (c) the parasitic MISFET channel formed by the top electrode, guard ring, and bottom electrode.

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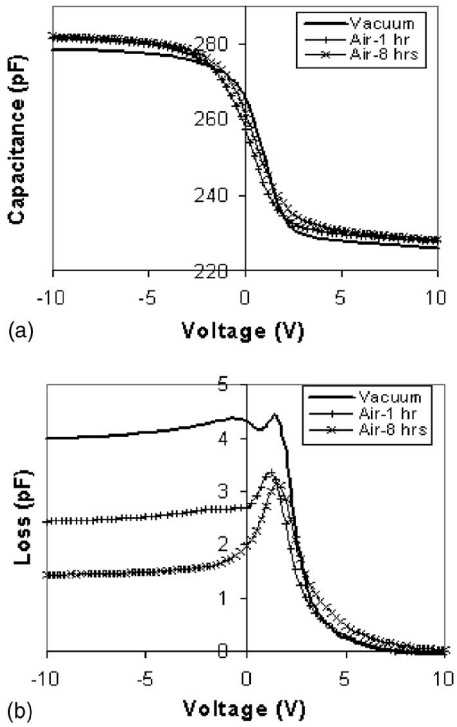

FIG. 2. Voltage dependence of (a) capacitance and (b) loss of a MIS diode measured at 1 kHz after a 10 h anneal under vacuum at 100 °C, and then after exposure to ambient air for 1 h and 8 h. The measurement temperature was 20 °C.

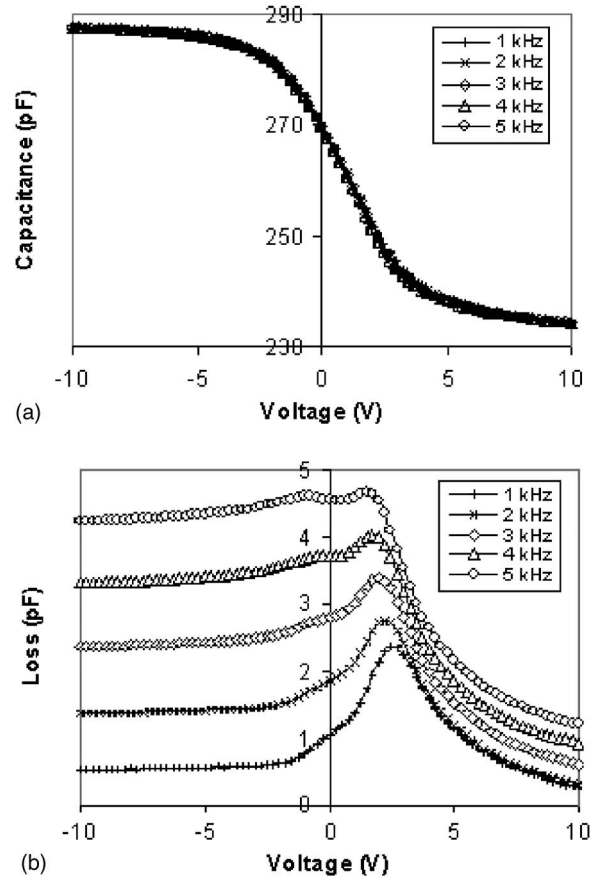

FIG. 3. Effect of signal frequency on the voltage dependence of (a) capacitance and (b) loss for a MIS diode left in air for 78 h.

esquioxane (Gelest, Inc.) in butanone, as the gate insulator and regioregular poly(3-hexylthiophene) (P3HT) (Sigma-Aldrich) as the active semiconductor following our previously reported technique.[3] After spin coating a P3HT film of ~80 nm thick onto the ~300 nm thick PSQ layer, a circular gold top electrode with associated guard ring was formed by vacuum evaporation through a shadow mask. The top electrode diameter was ~2 mm and the gap to the guard ring was nominally 50 μm. Optical microscopy, confirmed by atomic force microscopy, suggested that this gap was much shorter in places due to the difficulty in keeping the shadow mask in contact with the surface during evaporation. After preparation, the samples were annealed at 100 °C under vacuum for times ranging from several hours to several days. After cooling to room temperature, device admittance was measured under vacuum as a function of applied voltage over a wide range of frequencies using a Solartron frequency response analyzer (model 1255 with model 1296 dielectric interface). As shown in the Fig. 1(a), a predetermined voltage V with a superimposed small-signal voltage v_{ac} was applied to the bottom electrode. The small-signal current i was measured at the top electrode while the guard ring was earthed. In the absence of the guard ring, lateral currents flow along the semiconductor in an attempt to charge the whole of the gate capacitance. The effect becomes especially marked at the low frequencies[5] necessary for investigating interface state effects and can only be limited using a guard ring.

Upon completing a sequence of measurements under vacuum, supplementary data were collected under a normal laboratory ambient to determine the effect of air on device properties.

III. RESULTS

In Fig. 2, we show the voltage dependence of (a) the capacitance and (b) the loss of one of our devices measured at 1 kHz, following a vacuum anneal of ~10 h. The C-V plots have the expected form. For negative voltages, the device is in accumulation when the almost constant capacitance is determined by the insulator layer. When driven into depletion with positive applied voltages, the capacitance falls as the depletion region expands. At punch-through, which corresponds to complete depletion of the semiconductor, the capacitance again becomes constant and is determined by the series sum of the insulator and semiconductor capacitances. The loss-voltage plot shows the previously reported double maximum albeit that the relative magnitudes of the peaks here are different. As before, though, one peak occurs when the device is well into depletion, while the other occurs at low negative voltages just before the capacitance saturates. When the vacuum was released and the diode exposed to laboratory air, changes to the C-V plot were minimal [Fig. 2(a)]. This is in contrast with the loss-voltage plots where (i) the almost constant loss observed for negative voltages decreases significantly and (ii) the accumulation peak disappears as the time in air increases.

After 78 h in air, the device admittance was remeasured, initially at 1 kHz, but then with increasing signal frequency. The results are presented in Fig. 3. Apart from (a) a slight threshold voltage shift to more positive voltages and (b) a

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further reduction in loss for negative voltages, the 1 kHz plots are similar to those given in Fig. 2. With increasing signal frequency, the C-V plots were virtually identical [Fig. 3(a)]. However, in Fig. 3(b), we see that the background loss increased and the accumulation peak reappeared. As observed in our previous work,[3] both peaks shift slightly to less positive (more negative) voltages as the frequency increases, a characteristic feature of a distribution of interface states.[6] In the following sections, though, we show that only the more prominent "depletion" peak can be ascribed to the presence of such states. All other features observed in the plots are a consequence of the device geometry employed and changes in doping density in the semiconductor induced by exposure to air.

IV. THEORETICAL MODEL

The small-signal behavior of an ideal organic MIS capacitor is readily determined from its equivalent circuit, shown in Fig. 1(b), where the parallel combination R_B and C_B represents the bulk semiconductor and C_I the gate insulator. When the device is in accumulation, the admittance Y_{diode} of the circuit may be represented by[7]

$$Y_{\text{diode}} = G_{\text{diode}} + j\omega C_{\text{diode}}, \tag{1}$$

where ω is the angular frequency, $j=\sqrt{-1}$,

$$C_{\text{diode}} = C_g + \frac{C_I - C_g}{1+(\omega\tau)^2}, \tag{2}$$

and

$$\frac{G_{\text{diode}}}{\omega} = \frac{\omega R_B C_I^2}{1+(\omega\tau)^2}. \tag{3}$$

Here, C_g is the series sum of C_I and C_B and τ the circuit relaxation time given by

$$\tau = R_B(C_I + C_B). \tag{4}$$

When biased into depletion, then C_I must be replaced by C_S the series sum of C_I and C_D the depletion capacitance. C_S is readily computed from the standard equation[8] for a MIS capacitor, i.e.,

$$\frac{C_S}{C_I} = \left(1 + \frac{2C_I^2}{A^2 q N_A \varepsilon_S \varepsilon_0} V\right)^{-1/2}, \tag{5}$$

where A is the diode area defined by the upper electrode, q the electronic charge, N_A the doping density in the semiconductor, ε_S the relative permittivity of the semiconductor, ε_0 the permittivity of free space, and V the applied voltage. This equation can then be used to determine C_D and hence the width of the depletion region $d_D = A\varepsilon_S\varepsilon_0/C_D$. With the growth of a depletion region, R_B and C_B must be suitably modified to account for the reduction in the effective thickness of the bulk semiconductor,[3] i.e.,

$$R_B = (d_S - d_D)/AN_A q\mu_b \quad \text{and } C_B = A\varepsilon_S\varepsilon_0/(d_S - d_D),$$

where d_S is the thickness of the semiconductor and μ_b the mobility of carriers in the bulk of the semiconductor.

Although necessary for limiting lateral conduction along the semiconductor,[5] the guard ring in combination with the top and bottom electrodes act as a parasitic MISFET with zero source-drain bias. Consequently, it also will have a small-signal response that contributes to the total device admittance. Following the recent publication by Jung *et al.*[9] for the accumulation channel in pentacene, the transistor may be represented by a distributed RC network [Fig. 1(c)] with an admittance

$$Y_T = G_T + j\omega C_T.$$

Assuming that the gap L between the guard ring and top electrode is much smaller than the radius of the latter, then approximately half the small-signal current to charge the transistor channel flows from the top contact with the remainder flowing from the grounded guard ring. Consequently, the measured contribution of the MISFET channel to the overall device admittance is given by

$$C_T = \frac{C_i LW}{2\alpha}\frac{\sinh\alpha + \sin\alpha}{\cosh\alpha + \cos\alpha}, \tag{6}$$

and

$$\frac{G_T}{\omega} = \frac{C_i LW}{2\alpha}\frac{\sinh\alpha - \sin\alpha}{\cosh\alpha + \cos\alpha}, \tag{7}$$

where

$$\alpha^2 = \tfrac{1}{2}\omega C_i R_S L^2 \tag{8}$$

is the measurement frequency normalized to the relaxation frequency (inversely proportional to the transit time) of the device, W the channel width, C_i the capacitance per unit area of the insulator, and R_S the sheet resistance of the channel. At low frequencies, when $\alpha \sim 0$, then $C \sim WLC_i/2$ and $G/\omega \sim 0$.

In a recent publication,[10] we point out that in real devices, the response of the MISFET will be modified by parasitic conduction from source to drain through the bulk semiconductor. This gives rise to an additional sheet resistance R_b in parallel with the channel resistance R_{ch}, so that $R_S = R_{\text{ch}}R_b/(R_{\text{ch}}+R_b)$. When the device is in the linear regime, the channel resistance may be written as

$$R_{\text{ch}} = (C_i V \mu_{\text{ch}})^{-1}, \tag{9}$$

where μ_{ch} is the field effect mobility in the channel and

$$R_b = (N_A q \mu_b d_S)^{-1}. \tag{10}$$

Using different mobilities for the bulk and channel regions is justified in view of the hopping nature of charge transport in semiconducting polymers: the higher charge concentration in the accumulation channel fills the deeper states leading to an increase of several orders of magnitude in the channel mobility over bulk values.[11]

When operating in depletion, R_{ch} becomes infinite (the channel disappears) and R_b increases owing to the growth of a depletion region into the semiconductor which results in a reduced cross section for transport [d_S in Eq. (10) is replaced by $(d_S - d_D)$]. Also, C_i in Eqs. (6)–(8) must be replaced by the series combination of C_i and C_d, where $C_d = \varepsilon_S\varepsilon_0/d_D$ is the capacitance per unit area of the depletion region and may be determined from Eq. (5) as for the diode. To a reasonable

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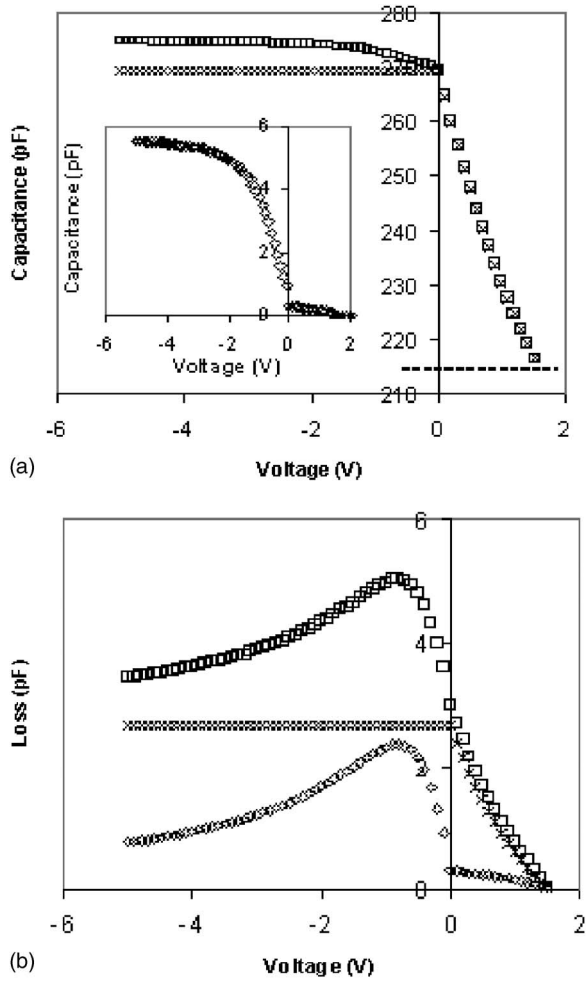

FIG. 4. Calculated voltage dependence of (a) capacitance and (b) loss of a MIS diode employing a guarded top electrode. The overall admittance (□) is composed of contributions from the diode (×) and the parasitic MISFET (◇). The parameters used in the calculation were $L=20\ \mu$m, $W=6$ mm, $\varepsilon_S=3.5$, $\varepsilon_i=3.2$, $d_i=300$ nm, $d_S=80$ nm, $N_A=1\times10^{22}$ m^{-3}, $\mu_{ch}=3\times10^{-7}$ m^2/V s, $\mu_b=3\times10^{-9}$ m^2/V s, and $f=1$ kHz. The horizontal dotted line indicates full depletion of the semiconductor when the capacitance becomes constant.

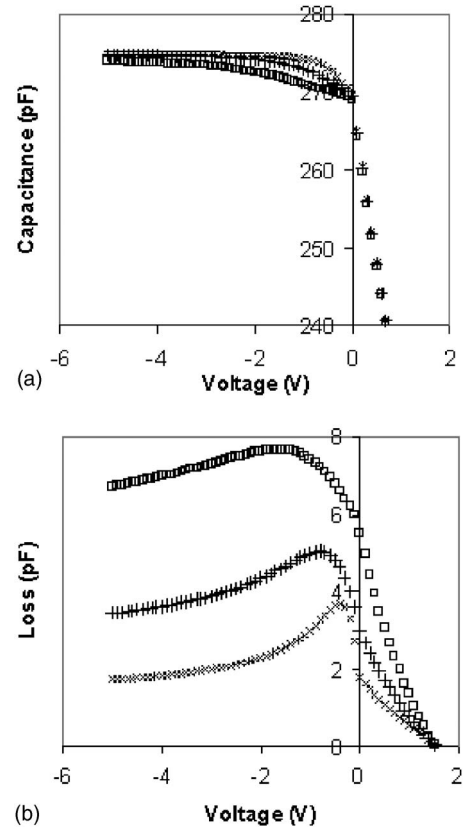

FIG. 5. Calculated voltage dependence of (a) capacitance and (b) loss of a MIS diode employing a guarded top electrode for signal frequencies of 500 Hz (×), 1 kHz (+), and 2 kHz (□). All other parameters were the same as in Fig. 4.

approximation and assuming no interaction between the two regions of the device, the total device admittance Y is then given by

$$Y = Y_{\text{diode}} + Y_T = (G_{\text{diode}} + G_T) + j\omega(C_{\text{diode}} + C_T). \qquad (11)$$

The suite of Eqs. (1)–(11) can now be used to calculate the voltage dependence of the device admittance for a range of measurement frequencies.

V. NUMERICAL SIMULATIONS

Using the relations given in the previous section, the overall admittance of a diode was calculated at 1 kHz and is plotted as a function of applied voltage in Fig. 4, together with the individual contributions from the diode and transistor. Values for the various parameters used in the calculations are given in the figure caption. The geometrical factors were chosen to be relevant to the device geometry used in the study, while the doping density N_A was close to that estimated from the experimental C-V curve measured under vacuum and given in Fig. 2(a). The intention here is not to attempt an exact fit to the experimental data (this would require more accurate geometric data, inclusion of any flatband voltage shift, and a more refined description of transport in the bulk semiconductor and accumulation channels). Rather, we wish to show that for the parameter values chosen, the model not only predicts reasonable values for capacitance and loss but also reproduces the experimentally observed dependences on voltage and frequency.

As seen in Fig. 4, the capacitance and loss of the diode are both constant in accumulation and decrease when in depletion ($V>0$) until the semiconductor becomes fully depleted. Hence, for $V>1.6$ V, the capacitance will become constant. When the device is driven into accumulation, the parasitic transistor response shows a capacitance increasing to a final value of ~5.7 pF. This rise in capacitance is accompanied by a loss which passes through a maximum before decreasing to zero at high negative voltages. When the device is driven to full depletion, both components decrease to zero. If the doping density is increased, for example, by prolonged air exposure as is the case for Fig. 3, then Eqs. (3), (4), (7), (9), and (10) predict an increase in the relaxation frequency of both the diode and the parasitic MISFET when the device is in accumulation. Thus, the experimental results in Fig. 3 will exhibit the behavior predicted by Fig. 4 but at a correspondingly higher frequency. In Fig. 5, we show the effect of frequency on the admittance-voltage characteristics. Of interest here is the broadening and shift of the loss peak to

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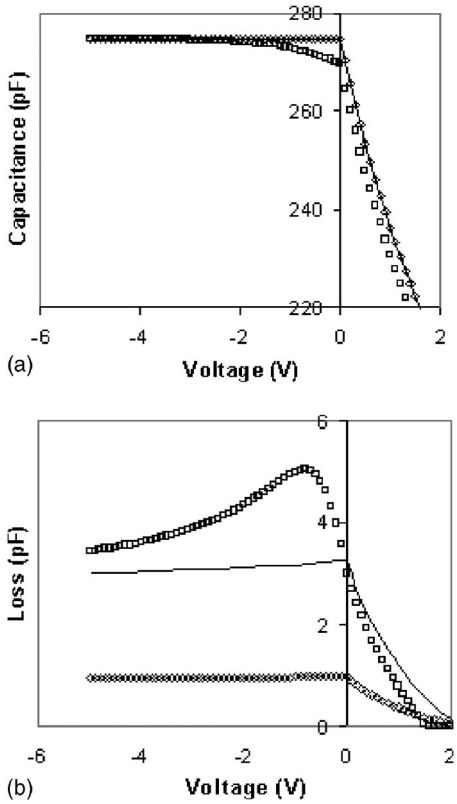

FIG. 6. Calculated voltage dependence of (a) capacitance and (b) loss of a MIS diode with guarded electrode. The vacuum-annealed device (□) is represented by the 1 kHz data from Fig. 4. The effect of air doping is simulated by increasing N_A in the parasitic MISFET to 5×10^{24} m^{-3} (—), all other parameters including N_A in the diode remaining the same. A reduction in the diode resistance R_B is simulated (◇) by increasing μ_b to 3×10^{-9} m^2/V s while retaining the low doping density in the bulk diode region.

negative voltages as the frequency increases. It should also be noted that the loss maximum occurs in a voltage region where the transistor response contributes an increasing capacitance with increasing accumulation voltage. Such behavior is similar to that of the accumulation peak in Fig. 3(b). We conclude, therefore, that this feature is an artifact arising from the parasitic transistor created by the guarded electrode structure used in the experiments.

Further simulations were undertaken to test whether the model can explain the effect of air exposure seen in Fig. 2(b). In Fig. 6, to represent the vacuum annealed case, the total device response is reproduced from Fig. 4. It is expected that oxygen in the air will act as an additional dopant[12] in the P3HT. However, there is little difference between the experimental *C-V* plot for the vacuum annealed device and that obtained after 8 h of air exposure. Therefore, we may conclude that during this time little diffusion of air occurred through the gold electrode into the bulk of the diode. Any observed changes in behavior must then be due to changes in the exposed semiconductor between the top contact and the guard ring. Accordingly, using Eqs. (6)–(10), we simulated the effect of increasing the doping density in this region only, from 1×10^{22} to 5×10^{24} m^{-3}. The results are given by the solid curves in Fig. 6 from which it is seen that this large increase in doping density had little effect on the *C-V* plot. In accumulation, the small transistor contribution to the capacitance simply rises faster, while the contribution to the loss becomes negligible. However, the underlying loss arising from the diode component is unaffected and remains much higher than seen experimentally. To reduce this underlying loss requires a reduction in R_B while maintaining the same low doping density as for the vacuum case. This can be achieved by increasing μ_B, as shown in Fig. 6(b). However, justifying such an increase is difficult when air is apparently unable to penetrate to any great extent into the bulk semiconductor under the gold electrode. It is more likely that the reduction in R_B is effected by conduction through the more highly doped semiconductor regions at the periphery of the top electrode, suggesting that some refinement of the basic model presented here is required to allow for interaction between the two regions of the device.

VI. DISCUSSION

The computer calculations based on the device model presented in Sec. III, predict all the essential features observed in the experimental measurements. Particularly encouraging is that upon using reasonable device parameters even the magnitudes of the capacitance and loss are close to experimental values. In particular, good agreement is found when using a residual doping density (1×10^{22} m^{-3}) similar to values we have reported previously[3] after vacuum annealing. Similarly, exposing our devices to laboratory air increases the doping density in the uncovered semiconductor between top electrode and guard ring. Diffusion into the bulk semiconductor under the gold top contact appears to be much slower.

The model readily explains effects such as the disappearance of the accumulation peak when the device is exposed to air and its reappearance by increasing the signal frequency. Oxygen in the air preferentially increases the doping density in the parasitic transistor. This reduces R_b and hence R_S in Eq. (8), thus shifting the relaxation frequency of the MISFET to higher values with a consequent reduction in loss. In Fig. 3, this reduction in R_S is overcome by increasing the signal frequency so that operation is again closer to the transistor relaxation frequency, thereby increasing the loss. A similar effect occurs in the diode element of the device. The underlying loss in accumulation now depends on R_B which determines the relaxation frequency of the diode [see Eq. (4)]. As for the parasitic transistor contribution, operating at frequencies well below the relaxation frequency leads to low loss; when the signal frequency approaches the relaxation frequency, a significant increase in loss occurs.

Since no combination of parameter values predicts a double maximum in the loss, we can confidently assign the depletion peak to the presence of interface states (or insulator states close to the interface). After correcting for the effects of the substrate and the depletion capacitance, the magnitude of this peak yields the interface state density D_{it},[1] which is normally obtained following time-consuming calculations from G/ω versus ω plots at different voltages. Hill and Coleman[13] have demonstrated a simpler approach using *C-V* and G/ω-*V* plots which obviates such calculations while still

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yielding reasonably accurate values. Essentially, the method relies on the assumption that the measurement frequency is significantly lower than the diode relaxation frequency discussed above, so that the main contribution to the loss arises from majority carrier interaction with the interface states. The relation which they derive, namely,

$$D_{it} = \frac{2(G/\omega)_m}{qA}\left[\left(\frac{(G/\omega)_m}{C_I}\right)^2 + \left(1 - \frac{C_m}{C_I}\right)^2\right]^{-1}, \qquad (12)$$

where $(G/\omega)_m$ and C_m are the magnitudes of the loss peak maximum and the corresponding capacitance at which it occurs are easily applied to the 1 kHz plot in Fig. 3 for the air-exposed device. Here, the maximum loss is $\sim$2.5 pF which, after correcting for the small residual background, gives a peak height of $\sim$2 pF. The maximum loss occurs at 2.75 V corresponding to a capacitance of 247 pF in Fig. 3(a). Thus, with C_I=287 pF, D_{it} is estimated to be $\sim 4 \times 10^{10}$ eV^{-1} cm^{-2} and similar to values deduced from loss-frequency plots from similar devices[3] but considerably lower than observed recently in copper phthalocyanine devices[4] using Eq. (12). Interestingly, the density of these relatively "fast" states are about two orders of magnitude less than the density of the "slow" states responsible for the gate-bias stress instability which has been reported by several groups using different insulators and/or different semiconductors.[2,14–17]

Careful device modeling coupled with appropriate device geometry should enable accurate values for $(G/\omega)_m$ to be obtained for a range of signal frequencies, thus allowing different energy states at the interface to be probed. Hence, a density of states profile could be deduced for the interface traps allowing the effects of different processing conditions to be evaluated.

VII. CONCLUSIONS

We have shown that care is required when interpreting admittance data from MIS diodes with *unpatterned* gates. While a guard electrode surrounding the Ohmic contact to the semiconductor is essential for minimizing the effects of lateral currents at the low frequencies necessary for investigating interface states, nevertheless, the presence of such an electrode introduces a parasitic MISFET into the structure.

When the distributed RC equivalent circuit for the parasitic transistor is combined with that for an ideal MIS diode, good agreement is obtained between the predicted voltage and frequency dependences of the device admittance and experimental observations. In particular, the model shows that for a given range of device parameters and measurement frequency, a maximum may be observed in the loss component of the admittance when accumulation voltages are applied to the device. In addition, the model readily explains experimental observations such as the effect of air doping on device behavior—not surprisingly, air doping occurs more rapidly in the exposed semiconductor between the Ohmic contact and guard ring than in the bulk semiconductor protected by the Ohmic contact.

By identifying experimental conditions where the major contribution to loss arises from the presence of interface states, it becomes possible to estimate the interface state density, i.e., $\sim 4 \times 10^{10}$ eV^{-1} cm^{-2}. However, it should be noted that this value was deduced at a single frequency (1 kHz) for a device exposed to air for several days and is likely to reflect the density well into the band gap at the interface. Measurements need to be made over a range of frequencies to determine the density of interface states throughout the bandgap.

Finally, we note that in view of the prevalence of oxidized silicon wafers as the substrate for fabricating and testing organic MIS devices, common-gate device structures with unpatterned semiconductor films such as those studied here are generally the norm. While the present study concentrated on understanding the behaviour of MIS capacitors it, nevertheless, also has relevance to MIS transistors. For example, the model presented in Sec. IV can be used to calculate the voltage and frequency dependence of the admittance of MISFETs including the effects of parasitic overlap capacitance in bottom contact, staggered electrode devices.

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