Grid-Connected Symmetrical Cascaded Multilevel Converter for Power Quality Improvement

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***Abstract*—This paper discusses the use of a cascaded multilevel converter for flexible power conditioning in smart-grid applications. The main feature of the proposed scheme is the use of independent dc links with reduced voltages, which makes such a topology an ideal candidate for medium- and high-power applications with increased reliability. The developed control strategy regulates independent dc-link voltages in each H-bridge cell, and allows the selective and flexible compensation of disturbing currents under a variety of voltage conditions without requiring any reference frame transformation. The selective control strategies are based on the decompositions proposed in the conservative power theory, which result in several current-related terms associated with specific load characteristics. These current components are independent of each other and may be used to define different compensation strategies, which can be selective in minimizing particular effects of disturbing loads. Experimental results are provided to validate the possibilities and performance of the proposed control strategies, considering ideal and deteriorated voltage conditions.**

***Index Terms*—Active power filters, compensation strategies, multilevel inverter, reactive compensation, selective compensation, unbalance compensation.**

I. Introduction

ELECTRONIC systems and several nonlinear loads have been increasingly used since the advent of power electronics. Such devices are usually more efficient and flexible in a wide range of applications, such as ac and dc motor drives, battery chargers, power supplies, uninterruptible power supplies, rectifiers, etc. However, the current quality deterioration due to harmonic pollution from switching devices has been penetrating the utility grid and causing great concerns for the utility companies, operators, or even regular consumers in the local grid.

Several power conditioning topologies have been used for harmonic, reactive, and unbalanced current compensation [1]–[4] and their control strategies [5]–[9]. Regarding the choice of compensation strategies to be applied, a great number of possibilities have been addressed, highlighting the important contributions based on the instantaneous power (PQ) theory [10], [11] and synchronous reference frame (DQ) control method [12], [13]. However, there are alternative methodologies that may prove more flexible than the ones mentioned above, providing a simpler way to compensate for disturbances selectively, and simplifying our understanding of the related electrical characteristics. In this context, this paper proposes to use conservative power theory (CPT) [14]–[16] as an alternative framework for the development of electronic power processors (EPP), especially to the design of physical elements and to the definition of selective compensation strategies for multifunctional grid-tied inverters or shunt active filters. This is because the proper choice of which portions should be compensated is a critical factor for the project since the actual nominal value directly influences the requirements of the active and passive elements of the EPP, and thus, the financial cost of their installations.

From the converter's topology point of view, multilevel inverters have several merits over conventional inverters, such as low total harmonics distortion, low switching losses, good power quality, reduced electromagnetic interference, modularity, and low switch voltage stress of electronic components [17], [18]. Among different topologies of multilevel converters, such as the neutral point clamped or diode clamped and the flying capacitor, cascaded multilevel converter is one of the most popular [18]. It is composed of multiple H-bridge power cells. In practice, the number of power cells in a cascaded H-bridge inverter is mainly determined by its operating voltage and manufacturing cost. Cascaded H-bridge multilevel inverter (CHMI) requires the least number of components for the same voltage level as compared to other types of multilevel inverters [19], [20]. The CHMI consists of individual H-bridge cells, which are fed by individual dc source. Each H-bridge cell generates three different voltage levels at the output. The series connection of the H-bridge cells generates output voltage waveforms that are synthesized by the combination of each output of the H-bridges at

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certain switching states. For shunt active power filter (SAPF) and static synchronous compensator (STATCOM) applications, capacitors might be used at the CHMI dc-links, instead of dc sources, and a variety of strategies for controlling the CHMI dc-link voltage is reported in the literature [21]–[26].

This paper proposes the control of a seven-level SAPF CHMI with individual H-bridge dc-link voltage regulation, applied for selective compensation or minimization of particular load disturbances, under a variety of voltage conditions. The presented control method is modular, and it can be adapted to any number of modules in series. CPT is used as an alternative for generating a variety of current references in the stationary frame for selective disturbances mitigation, and if needed active power injection. Compared to the initial proposal in [27], new findings and experimental results were included to support the theoretical analysis.

The remainder of this paper is organized as follows. In Section II, a brief review of the cascaded multilevel shunt converter system and its modulation is presented. Section III presents a brief review of the CPT for three-phase circuits. Section IV presents the derivation of the developed control scheme of CHMI system in the stationary reference frame. In Section V, the performance and robustness of the control strategy for a three-phase CHMI unit are experimentally verified under different ac grid voltage conditions through a real-time hardware-in-the-loop (HIL) setup. Section VI discusses the similarities and differences of applying CPT, PQ, and DQ decompositions for shunt compensation, and finally, Section VII indicates the main conclusions of this paper.

II. CHMI Structure and Modulation

The CHMI is composed of a series of cascaded H-bridges, each fed by independent dc sources [19]. Each H-bridge, as a power cell, is capable of generating three different voltage levels at the output. The series connection of the H-bridges generates output voltage waveforms that are synthesized by the combination of each output of the H-bridges at certain switching states. This topology offers many advantages such as the feature of modularity, control, and protection requirements of each bridge cell. The cascaded multilevel shunt converter is shown in Fig. 1, where it is also possible to see the network loads connected at the point of common coupling (PCC). The PCC loads are constituted by both balanced and unbalanced linear and nonlinear devices.

The output voltage waveform in each phase is obtained by adding the H-bridge cells output voltages as follows:

$$v_o(t) = v_{o,1}(t) + v_{o,2}(t) + \cdots + v_{o,N}(t) = \sum_{k=1}^{N} v_{o,k}(t) \quad (1)$$

where N is the number of H-bridge cells.

If all dc-voltage sources in Fig. 1 are equal to V_{dc}, the inverter is then known as a symmetric CHMI. The number of output levels (N_L) in a symmetric CHMI is related to the number of H-bridges (N) by the following equation:

$$N_L = 1 + 2N. \quad (2)$$

The maximum output voltage $V_{o,\mathrm{MAX}}$ is then obtained as

$$V_{o,\mathrm{MAX}} = N V_{\mathrm{dc}}. \quad (3)$$

Unequal magnitudes of the dc voltage sources in Fig. 1 would result in an asymmetric CHMI with an increased number of output levels generated by the same number of H-bridge cells [28].

Modulation strategies for CHMI are an extension of the traditional two-level switching schemes [29]. Various modulation strategies have been presented for CHMI to switch the transistors in each cell. By their switching frequency, they can be mainly classified either as fundamental or high switching frequencies. The first approach suggests lower switching losses, but the harmonics in the output voltage waveform appear at lower frequencies. Low-frequency strategies, such as selective harmonic elimination [30] and space vector control [31], are applied to high-power and low-dynamic systems. For the second approach, the harmonics are multiples of the switching frequency and their sidebands. Space vector modulation [32] and carrier-based pulse-width modulation (PWM) [33], [34] are examples of high-frequency strategies. The carrier-based modulation schemes can be divided into two categories: 1) phase-shifted PWM (PS-PWM); and 2) level-shifted PWM (LS-PWM).

In this paper, PS-PWM is used to switch the cascaded H-bridge cells. Since each H-bridge cell is a three-level converter, the traditional unipolar PWM switching schemes are adopted. The series-connected H-bridge cells of the converter are modulated with individual carrier waveforms while sharing the same reference signals. A phase shift among the carrier waveforms is applied to adjacent H-bridge cells. The angle of the phase shift depends on the level of the converter and is tailored to the specific switching scheme, which is implemented in each H-bridge cell. Optimum harmonic cancellation can be achieved when the phase shift between the carriers is $180^\circ/N$, where N is the number of series-connected H-bridge cells [35]. In this paper, the CHMI is composed of three modules, synthesizing a seven-level output voltage waveform. The triangular carriers with a phase shift of 60° are compared with two sinusoidal references for the presented seven-level CHMI, as illustrated in Fig. 2.

The implementation of a 60° phase shift among the three PWM triangular carriers inside the TMSF28335 DSP microcontroller for the seven-level CHMI is shown in Fig. 3.

Their implementations are listed as follows.

1) Counter register on PWM 1, PWM 2, and PWM 3 modules (which are carriers) counts from 0 to 6249. Note that period at each counter step for TMS320F28335 DSP board is 1/150 MHz, and the value 6249 is calculated as 6249 = (150 MHz/24 kHz)–1, where 24 kHz is twice of the switching frequency (see Table I).
2) Each PWM waveform has a 60° degree phase shift, which is achieved inside the DSP by the synchronization of PWM 1, PWM 2, and PWM 3 waveforms.
3) Each time PWM 1 counter counts to 0, event trigger introduced the synchronization process, which makes PWM 2 and PWM 3 counters load the saved numbers into their counters, at which time PWM 2 and PWM 3 counters will count from those saved numbers. Note that at the end of

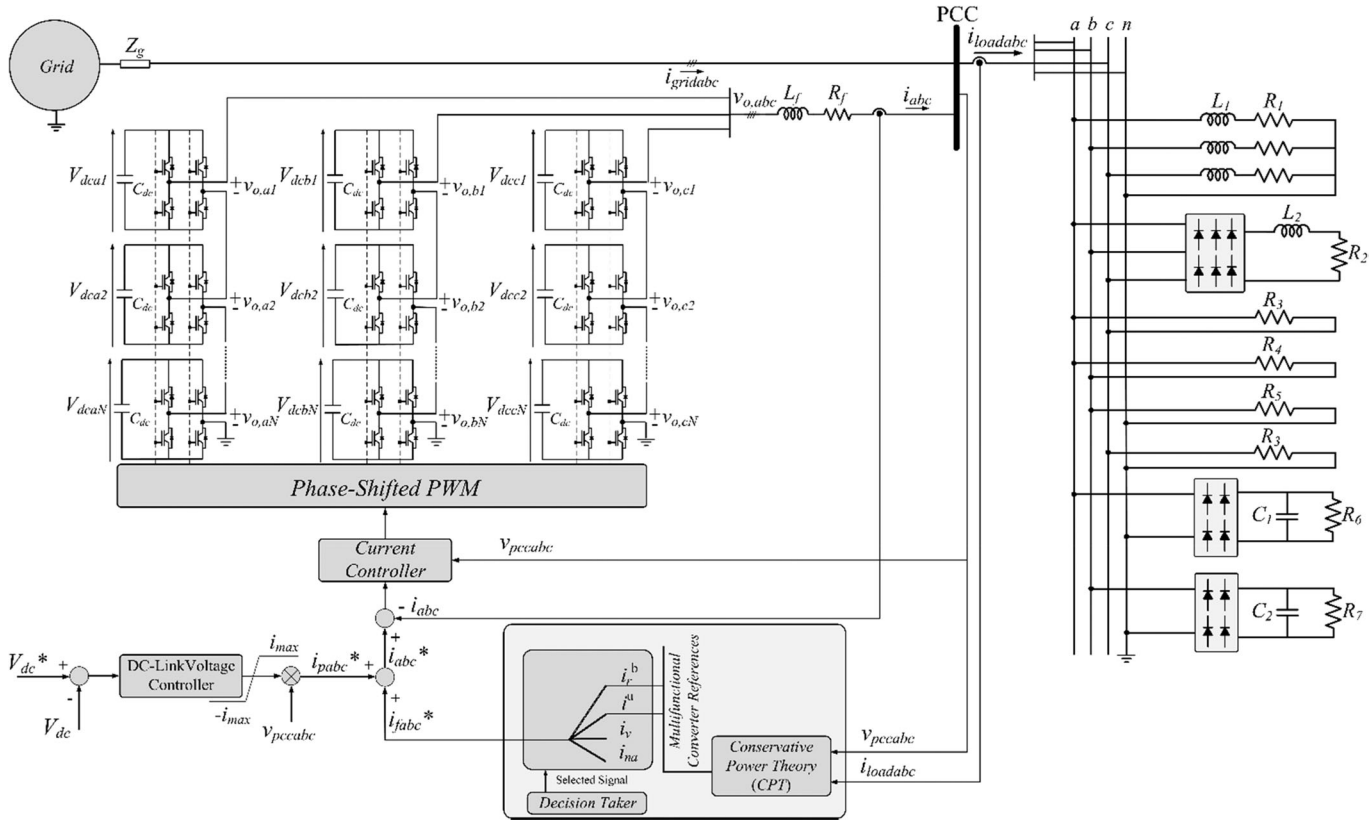

Fig. 1. Block diagram of the power circuit, control scheme, and loads to the power grid.

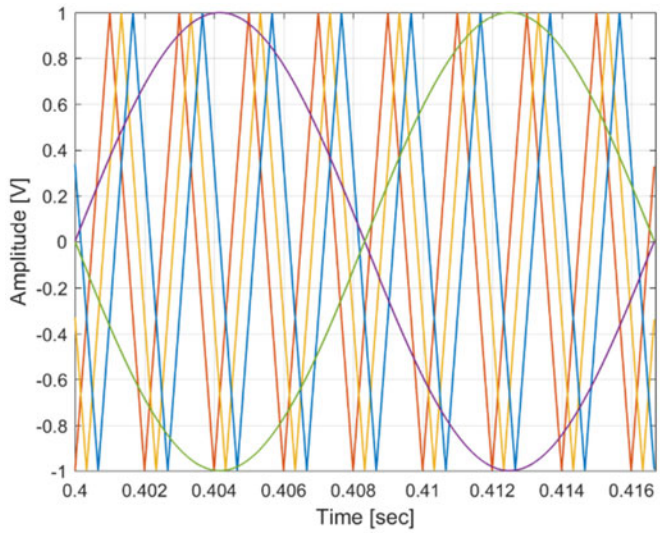

Fig. 2. Reference and carrier signals for one phase of the seven-level CHMI.

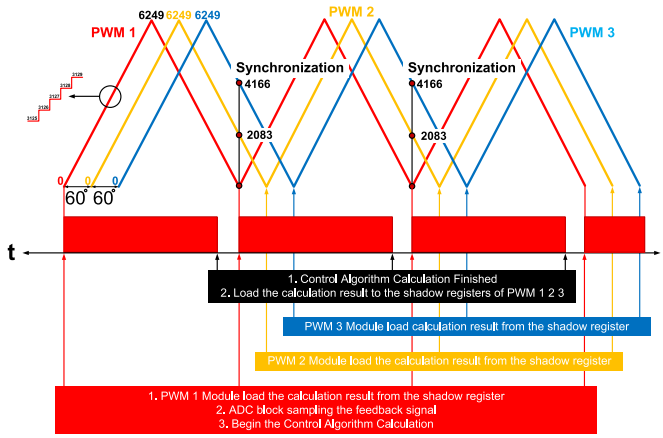

Fig. 3. DSP implementation of the PS-PWM for the seven-level CHMI.

each cycle, PWM 1 block sends out a command to begin interrupt function. This action is independent of the synchronization process.

4) The saved numbers are calculated in (4) as

$$2083 = \frac{1}{3} \times 6249 \text{ and } 4166 = \frac{2}{3} \times 6249. \quad (4)$$

5) At the beginning of each cycle (where the red arrow points showing the counter reaches zero and interrup function begins), the PWM 1 module will send out a signal to analog-to-digital conversion block to let it read the feedback sampled results, then CPU compares the results with references and errors will be proccessed through control algorithm; the output of the control algorithm will be then sent out to the shadow mode of compare register of PWM 1, PWM 2, and PWM 3 modules (where the black arrow points show that all the calculations are finished). At the

TABLE I
CHMI PARAMETERS

Parameter	Value
Nominal grid phase voltage, $v_{\rm rms}$	127 V
Grid frequency, f	60 Hz
Maximum power output	5 kVA
Switching frequency, f_s	12 kHz
Sampling period, T_s	(1/12000) s
Output filter inductor, L_f	1 mH
Output filter resistor, R_f	0.1 Ω
DC-link voltages, $V_{\rm dc1}$, $V_{\rm dc2}$, $V_{\rm dc3}$	70 V
DC-link capacitor, $C_{\rm dc}$	5 mF

beginning of next cycle (when PWM 1 module's counter counts to zero again), the PWM 1 compare register will load the shadow mode value. The PWM 2 and PWM 3 modules will load from their shadow registers when their counters count to zero (represented by yellow and blue line points, respectively).

III. CURRENT AND POWER DECOMPOSITIONS IN A MULTIPHASE CIRCUIT USING CPT

The CPT [14] allows for the decomposition of the instantaneous currents into different orthogonal current terms, valid for single- and multiphase systems, independent of the voltage conditions. Such components can be applied as reference signals to shunt active filters [15], [16], multifunctional converters [28], [36], [37], or for the design of filter elements, such as semiconductor switches, inductors, and capacitors. Moreover, the resulting compensation strategies are highly flexible since the decompositions allow for the selective identification and minimization of different disruptive effects (nonlinearities, unbalances, and reactive power). Thus, assuming a multiphase circuit where each phase of the system is denoted by the subscript "*m*," one may have the following:

1) balanced active currents (i^b_{am}), which are related to the active power consumption;
2) balanced reactive currents (i^b_{rm}), which are related to the reactive power circulation;
3) void currents (i_{vm}), which are related to the nonlinear (distortion) behavior between voltages and load currents;
4) unbalanced currents ($i^u_m = i^u_{am} + i^u_{rm}$), which are related to the unbalanced load behavior;
5) nonactive currents (i_{nam}), which represents all the unwanted terms of the load currents ($i_{nam} = i^b_{rm} + i_{vm} + i^u_m$).

By definition, the collective RMS current can be split into

$$I^2 = I_a^{b2} + {I_{na}}^2 = I_a^{b2} + I_r^{b2} + I^{u2} + {I_v}^2 \tag{5}$$

indicating that all current components are orthogonal to each other, and they could be controlled or minimized selectively. Thus, the apparent power may be calculated as

$$A^2 = V^2 \cdot I^2 = P^2 + Q^2 + N^2 + D^2 \tag{6}$$

where

- $P = V \cdot I^b_a$ is the active power (7.a)
- $Q = V \cdot I^b_r$ is the reactive power (7.b)
- $N = V \cdot I^u$ is the unbalance power (7.c)
- $D = V \cdot I_v$ is the void power. (7.d)

From the CPT, the global power factor is defined in (8), and it can be calculated in any generic circuit, independent of waveform distortions or asymmetries, representing the global efficiency of the load.

$$\lambda = \frac{P}{A} = \frac{P}{\sqrt{P^2 + Q^2 + N^2 + D^2}}\,. \tag{8}$$

IV. CONTROL STRATEGY

The proposed seven-level CHMI is controlled to regulate the dc-link voltages of each H-bridge cell, and to compensate current load terms related to disturbing effects. The voltage controller output, from H-bridge cells, is multiplied by the PCC voltage ($v_{{\rm pcc}abc}$), so as to define an additional current reference (i^*_{pabc}) to be added to the reference of the disturbance currents (i^*_{fabc}). The resulting current reference (i^*_{abc}) is directed to the current controller output of the active filter. Thus, the active filter must act as a high power factor controlled rectifier during transient load conditions, and as a current compensator under steady-state conditions. Notice that there is no need for any type of coordinate transformation or synchronization algorithm to provide the reference signals. Assuming one phase (a) of the CHMI, the control strategy for dc voltage controllers of each H-bridge cell is illustrated in Fig. 4, which is comprised of inner and outer control loops. The inner loop regulates the inverter output current at the desired reference (i^*_a), and the outer loop regulates the dc-link voltages in each H-bridge cell. The desired inverter current is the sum of the dc-link voltage regulation currents (i^*_{pa}) and the compensation references from the CPT decomposition (i^*_{fa}).

The currently proposed controller is designed in the *abc* frame based on frequency response requirements. Consider the CHMI of Fig. 1, the parameters of the converter are provided in Table I. The PCC voltages ($v_{{\rm pcc}abc}$) are dictated by the grid [38].

A. Current Controller Derivation

The dynamics of the ac-side current i_a is described by (9). It represents a system in which i_a is the state variable, $v_{o,ak}$ are the control inputs, and $v_{{\rm pcc}a}$ is the disturbance input

$$L_f \frac{di_a(t)}{dt} + R_f i_a(t) = \sum_{k=1}^{N} v_{o,ak}(t) - v_{{\rm pcc}a}(t)\,. \tag{9}$$

The H-bridge converter terminal voltages can be written as

$$\begin{bmatrix} v_{o,a1}(t) \\ v_{o,a2,}(t) \\ \vdots \\ v_{o,aN}(t) \end{bmatrix} = \begin{bmatrix} m_{o,a1}(t)\, V_{\rm dc} \\ m_{o,a2}(t)\, V_{\rm dc} \\ \vdots \\ m_{o,aN}(t)\, V_{\rm dc} \end{bmatrix} \tag{10}$$

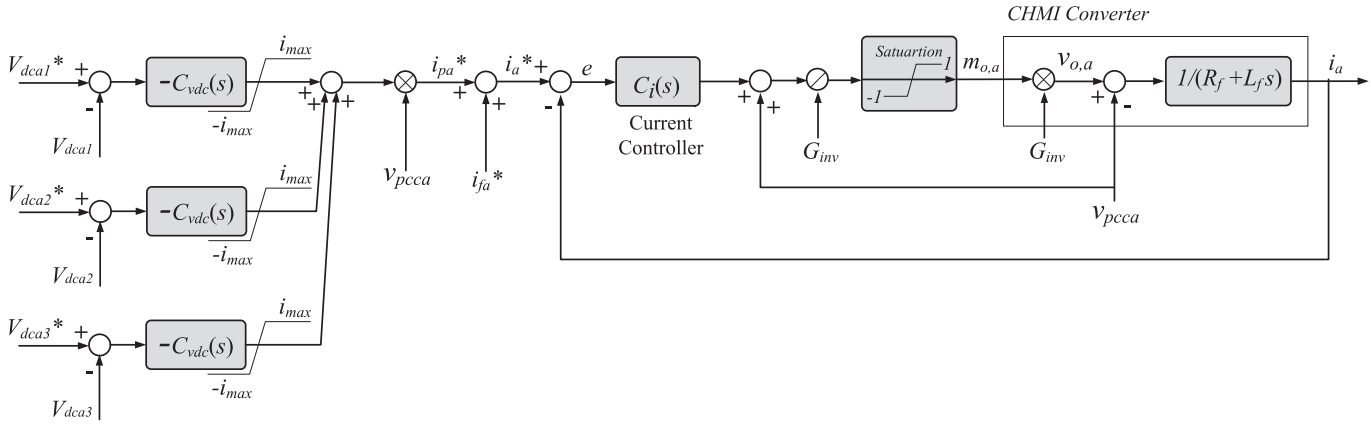

Fig. 4. Block diagram of the proposed control scheme with dc voltage controllers of H-bridge cells in phase a.

where $m_{o,a1}(t)$, $m_{o,a2}(t)$, $\ldots$, $m_{o,aN}(t)$ denote the modulation signals for each H-bridge converter. Their signals are continuous and their values are in the range [−1 1]. In order to facilitate the controller design and to reduce the model expressions, it is convenient to transform (10) by the definition given the following equation [22]:

$$m_{o,a}(t) = m_{o,a1}(t) = m_{o,a2}(t) = \cdots = m_{o,aN}(t). \tag{11}$$

Therefore, (9) can be rewritten as

$$L_f \frac{di_a(t)}{dt} + R_f i_a(t) = N V_{\rm dc}\, m_{o,a}(t) - v_{{\rm pcc}a}(t). \tag{12}$$

Assuming the CHMI of Fig. 1

$$v_{o,a}(t) = G_{\rm inv}\, m_{o,a}(t) = N V_{\rm dc}\, m_{o,a}(t). \tag{13}$$

Therefore, the dynamics of the ac-side current i_a is determined as (14). Based on (13), the control input $v_{o,a}$, can be controlled by the modulating signal $m_{o,a}$

$$L_f \frac{di_a(t)}{dt} + R_f i_a(t) = v_{o,a}(t) - v_{{\rm pcc}a}(t). \tag{14}$$

The last term in (14) $v_{{\rm pcc}a}(t)$ will be compensated by the feedforward action. The voltage feedforward compensation is employed to mitigate the dynamic couplings between the CHMI and the ac system, enhancing the disturbance rejection capability of the converter system. By applying the perturbation and linearization technique and taking the Laplace transformation, the CHMI output filter transfer function is determined as

$$G_i(s) = \frac{i_a(s)}{v_{o,a}(s)} = \frac{1}{L_f s + R_f}. \tag{15}$$

For the implementation of the control system inside the DSP, the system transfer function of (15) is converted from the continuous domain "s" to the discrete domain "z." The z-transformation of the transfer function in s domain, combined with a zero-order hold block, is provided by (16). The transformation is made using the relation $z = e^{s.T_s}$. So, $G_i(z)$ can be defined as follows:

$$G_i(z) = Z\left\{\frac{\left(1 - e^{-s.T_s}\right) G_i(s)}{s}\right\} \tag{16}$$

$$G_i(z) = \left(1 - z^{-1}\right) Z\left\{\frac{G_i(s)}{s}\right\}. \tag{17}$$

To allow the use of the frequency response design method, the conversion of $G_i(z)$ transfer function from "z" plane to "w" plane is performed using the bilinear transform

$$G_i(w) = G_i(z)\big|_{z=\frac{1+\frac{T_s}{2}w}{1-\frac{T_s}{2}w}} = \frac{-0.04167w + 1000}{w + 100}. \tag{18}$$

To perform the controller design, the open-loop current control transfer function $G_{oi}(w)$ is obtained as expressed in (19). $C_i(w)$, the controller of the current control loop, consists of a lag compensator as (20), where the parameters of ω_z, ω_p, and k_c are the zero, pole, and the gain of the compensator, respectively

$$G_{oi}(w) = C_i(w)\, G_i(w) \tag{19}$$

$$C_i(w) = \frac{k_c\ (1 + s/\omega_z)}{\left(1 + s/\omega_p\right)}. \tag{20}$$

Fig. 5 presents a comparison between the frequency response of the system transfer function $G_i(s)$ and digitized plant $G_i(w)$. In Fig. 5(a), the magnitude Bode diagram and in Fig. 5(b), the phase Bode diagram of the current control plant in both "s" and "w" planes are illustrated, respectively. From Fig. 5(a), it is noticeable that the frequency response magnitude presents conformity up to 2 kHz, whereas from Fig. 5(b), the phase shows substantial error caused by the zero added because of the digitization process.

Table II presents the requirements chosen for the control scheme of the CHMI output current. The bandwidth is chosen to be one-tenth of the switching frequency to limit the current loop response to the switching noises. However, it is high enough to achieve a fast dynamic response. The desired phase margin is selected based on the approach introduced in [39] for determining the parameters of the lag compensator in a digitized system.

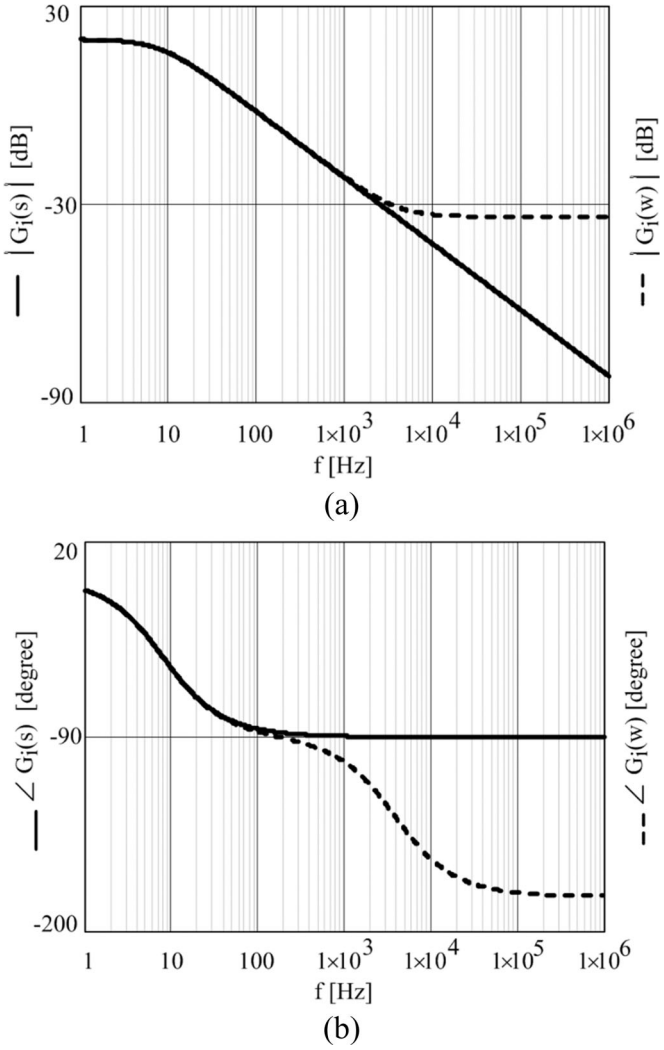

Fig. 5. Bode diagram of the current control plant in both "s" and "w" planes: (a) magnitude response; and (b) phase response.

TABLE II
REQUIREMENTS CHOSEN FOR CURRENT CONTROL SCHEME

Symbol	Quantity	Value
$\varphi_{\mathrm{PM}i}$	Desired phase margin	72°
f_{ci}	Desired cutoff frequency	1.2 kHz

Based on this technique, we choose $f_z = 0.1 f_{ci}$ to ensure that little phase lag is introduced at f_{ci}. In (22), the lag controller reduces the system phase by 1.31°.

The gain and the phase are used to calculate the lag controller design parameters as given by (21) and (22), respectively

$$G_{ci} = -\left|G_i\left(f_{ci}\right)\right| \mathrm{dB} = 17.13 \mathrm{\ dB} = 7.19 \tag{21}$$

$$\varphi_{ci} = \varphi_{\mathrm{PM}i} - \angle G_i\left(f_{ci}\right) - 180^\circ = -1.31^\circ. \tag{22}$$

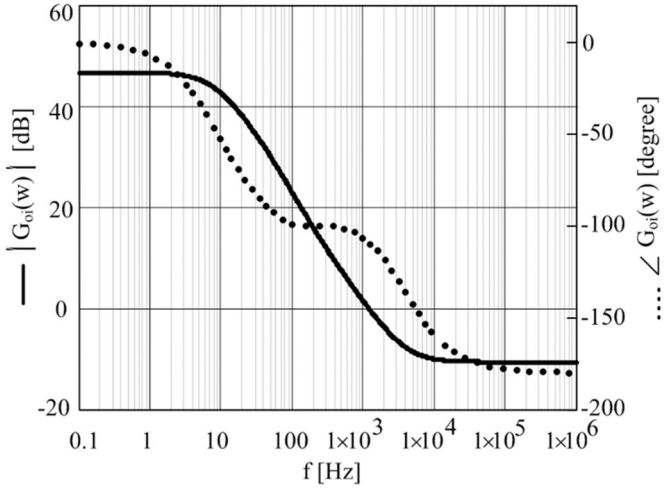

Fig. 6. Bode plot of the open-loop current transfer function.

Therefore, the zero, pole, and the gain of the lag controller are given by (23)–(25), respectively

$$f_z = \frac{f_{ci}}{10} = 120 \mathrm{\ Hz} \tag{23}$$

$$f_p = \frac{\left(2\pi f_z + 2\pi f_{ci} \times \tan\left(\varphi_{ci}\right)\right)}{2\pi \times \left[1 - \left(2\pi f_z\right) \times \frac{\tan(\varphi_{ci})}{2\pi f_{ci}}\right]} = 92.17 \mathrm{\ Hz} \tag{24}$$

$$k_c = \sqrt{\frac{G_{ci}^2}{\frac{\left(2\pi f_p\right)^2 \times \left[\left(2\pi f_z\right)^2 + \left(2\pi f_c\right)^2\right]}{\left(2\pi f_z\right)^2 \times \left[\left(2\pi f_p\right)^2 + \left(2\pi f_c\right)^2\right]}}} = 9.34. \tag{25}$$

Fig. 6 presents the Bode diagram of the open-loop current transfer function. As observed, at the crossover frequency $f_{ci} =$ 1.2 kHz, the open-loop gain of 0 dB and the phase margin of 72° are achieved. The digital implementation of the lag controller (20) in the "z" domain is obtained by transformed back to "z" plane with a sampling time of T_s, which is also the switching period

$$C_i\left(z\right) = C_i\left(w\right)\big|_{w=\frac{2}{T_s}\frac{z-1}{z+1}}. \tag{26}$$

Therefore, the controller transfer function $C_i(z)$ can be expressed as

$$C_i\left(z\right) = \frac{n_1 + n_0 z^{-1}}{d_1 + d_0 z^{-1}}. \tag{27}$$

The numerator parameters of (27) are calculated as follows:

$$n_1 = \frac{k_c\left(2\omega_p + T_s\omega_z\omega_p\right)}{2\omega_z + T_s\omega_z\omega_p},\ n_0 = \frac{k_c\left(-2\omega_p + T_s\omega_z\omega_p\right)}{2\omega_z + T_s\omega_z\omega_p} \tag{28}$$

and the denominator parameters are calculated as

$$d_1 = 1,\ d_0 = \frac{\left(-2\omega_z + T_s\omega_z\omega_p\right)}{2\omega_z + T_s\omega_z\omega_p}. \tag{29}$$

Having a sampling period $T_s = (1/12000)$ s, the controller transfer function $C_i(z)$ can be expressed as

$$C_i(z) = \frac{7.23 - 6.79z^{-1}}{1 - 0.952z^{-1}}. \tag{30}$$

B. DC-Link Controller Derivation

The dimensioning of the dc-link voltage controller is based on the transfer function between the defined current reference value and the dc-link voltage in each H-bridge cell [40]. Thus, considering phase a from the power balance of the inverter in this phase one may have

$$P_{\text{cap}} + P_{ac} = 0 \tag{31}$$

$$3V_{\text{dc}}I_{\text{cap}} + \frac{V_a I_a}{2} = 0 \tag{32}$$

where factor 3 represents the number of H-bridge cells in phase a, V_{dc} is the regulated dc-link voltage for each H-bridge cell, I_{cap} is the respective capacitor current, V_a and I_a represent the peak value of the ac-side voltage and current of phase a respectively, and factor 1/2 comes from the average ac power flow using peak values.

From (32), the current through each H-bridge cell capacitor is

$$I_{\text{cap}} = -\left(\frac{V_a I_a}{6V_{\text{dc}}}\right). \tag{33}$$

And the same current regarding voltage across the capacitor is given by

$$C_{\text{dc}}\frac{dV_{\text{dc}}}{dt} = I_{\text{cap}}. \tag{34}$$

From (33) and (34), the differential equation for the dc voltage becomes

$$\frac{dV_{\text{dc}}}{dt} = \frac{1}{C_{\text{dc}}}\left(\frac{-V_a\ I_a}{6V_{\text{dc}}}\right). \tag{35}$$

Based on (35), the dc-link voltage for one H-bridge cell is regulated by controlling the inverter current reference (i_a^*). The selected bandwidth of the dc voltage loop is reduced to avoid interaction with the current controller. This means that the individual capacitor voltage controllers are decoupled from the current controller as their dynamics are slowed down. Therefore, the closed current loop can be assumed ideal for designing purposes and replaced by unity. The transfer functions of the dc voltage control scheme $G_{v\text{dc}}(s)$ is presented in (36). The dc-link voltage controller $C_{v\text{dc}}(s)$ is multiplied by –1 to compensate for the negative sign of dc bus voltage dynamics

$$G_{v\text{dc}}(s) = \frac{V_a^2}{6V_{\text{dc}}}\frac{1}{C_{\text{dc}}s}. \tag{36}$$

For the DSP implementation of the dc voltage control scheme, the system transfer function of (36) is converted from the continuous plane "s" to the discrete plane "z." The plant transfer function in "z" domain is achieved in (37). To allow the use of the frequency response method design, the conversion of $G_{v\text{dc}}(z)$ transfer function from "z" plane to "w" plane is performed using the bilinear transform in (38)

$$G_{v\text{dc}}(z) = \left(1 - z^{-1}\right) Z\left\{\frac{G_{v\text{dc}}(s)}{s}\right\} \tag{37}$$

$$G_{v\text{dc}}(w) = G_{v\text{dc}}(z)\big|_{z=\frac{1+\frac{T_s}{2}w}{1-\frac{T_s}{2}w}} = \frac{-0.6429w + 15430}{w}. \tag{38}$$

TABLE III
REQUIREMENTS CHOSEN FOR DC VOLTAGE CONTROL SCHEME

Symbol	Quantity	Value
$\varphi_{\text{PM}v\text{dc}}$	Desired phase margin	60°
$f_{cv\text{dc}}$	Desired cutoff frequency	5 Hz

Table III presents the requirements chosen for the control scheme of the dc voltage loop. The dc-side capacitor voltages are sensed and compared to a set of voltage references. The target phase margin can be negotiated depending on the requirements for the transient settling time and the stability. When a system has a larger phase margin it will be more robust because the parameter variation will not affect the stability. On the other hand, a bigger phase margin makes the feedback response more sluggish and the system may take a longer time for settling down; therefore, a high frequency noise can propagate on the closed-loop transfer function. Typically, a desired phase margin to meet the stability criterion is greater than 45° [41].

The open-loop transfer functions of the dc voltage control loop $G_{ov\text{dc}}(w)$ is presented in (39). A proportional integral (PI) compensator is intended for $C_{v\text{dc}}(w)$ as in (40) for dc-link voltage regulation, where the parameters of k_p and T are the proportional gain and time constant of the compensator, respectively

$$G_{ov\text{dc}}(w) = C_{v\text{dc}}(w)\,G_{v\text{dc}}(w). \tag{39}$$

$$C_{v\text{dc}}(w) = k_p\left(\frac{wT\ +\ 1}{wT}\right). \tag{40}$$

The gain and the phase to be used for calculating the PI controller parameters are obtained according to (41) and (42), respectively

$$G_{cv\text{dc}} = -\left|G_{v\text{dc}}(f_{cv\text{dc}})\right|\ \text{dB} = -53.82\ \text{dB} = 0.002 \tag{41}$$

$$\varphi_{cv\text{dc}} = \varphi_{\text{PM}v\text{dc}} - \angle G_{v\text{dc}}(f_{cv\text{dc}}) - 180^\circ = -29.92^\circ. \tag{42}$$

Therefore, the time constant and proportional gain of the PI controller are given by (43) and (44), respectively

$$T = \frac{\tan(\varphi_{cv\text{dc}} + 90^\circ)}{2\pi f_{cv\text{dc}}} = 0.055\ \text{s} \tag{43}$$

$$k_p = \sqrt{\frac{G_{cv\text{dc}}^2}{\frac{T^{-2} + (2\pi f_{cv\text{dc}})^2}{(2\pi f_{cv\text{dc}})^2}}} = 0.0017. \tag{44}$$

The frequency response of the open-loop dc voltage transfer function is illustrated in Fig. 7. At the crossover frequency $f_{cv\text{dc}} = 5$ Hz, an open-loop gain of 0 dB and a phase margin of 60° are obtained.

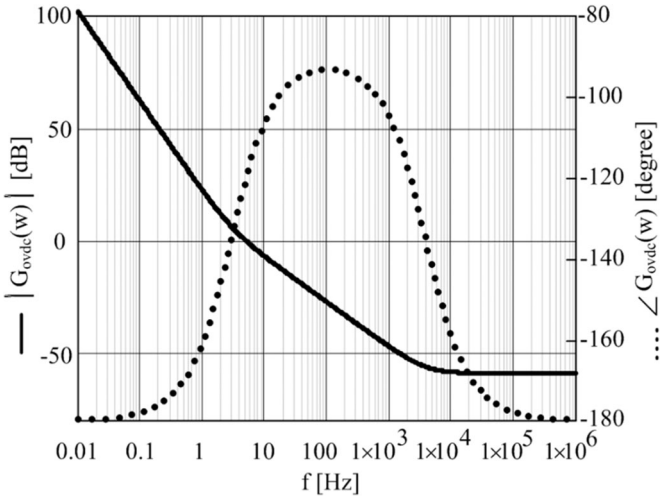

Fig. 7. Bode plot of the open-loop dc-link voltage transfer function.

The digital implementation of the PI controller (40) in the "z" domain is obtained by transforming it back to "z" plane with a sampling time of T_s, which is also the switching period

$$C_{vdc}(z) = C_{vdc}(w)|_{w=\frac{2}{T_s}\frac{z-1}{z+1}}. \tag{45}$$

Therefore, the controller transfer function $C_{vdc}(z)$ can be expressed as

$$C_{vdc}(z) = \frac{n_1 + n_0 z^{-1}}{d_1 + d_0 z^{-1}}. \tag{46}$$

The numerator and denominator parameters of (46) are calculated as

$$n_1 = \left(\frac{k_p}{2T}\right) T_s + k_p,\ n_0 = \left(\frac{k_p}{2T}\right) T_s - k_p,\ d_1 = 1$$
$$d_0 = -1. \tag{47}$$

Having a sampling period $T_s = (1/12\,000)$ s, the controller transfer function $C_{vdc}(z)$ can be expressed as

$$C_{vdc}(z) = \frac{0.0017 - 0.0017 z^{-1}}{1 - z^{-1}}. \tag{48}$$

V. Experimental Results

To evaluate the performance of selective compensation strategies by using the cascaded multilevel shunt converter, the three-phase system of Fig. 1 is experimentally verified under different voltage conditions using a real-time HIL system. The power plant was built inside MATLAB/Simulink. Then, the system was compiled inside the real-time simulator "Opal-RT." The control algorithm was implemented in a TMSF28335 digital signal processor (DSP) microcontroller with the switching and sampling frequencies set at 12 kHz. The load parameters are listed in Table IV. The nonlinear loads were composed of three- and single-phase full-bridge rectifiers feeding capacitive and resistive loads. The results were captured using a HAMEG HMO724 four-channel oscilloscope.

Fig. 8 presents the PCC voltage and grid current waveforms measured at the PCC, before implementing any compensation strategy, and the grid supplies the entire load current. Notice that the currents are unbalanced and significantly distorted. Sections V-A–V-C present and discuss three possible scenarios (1, 2, and 3).

TABLE IV
Load Parameters

Parameter	Value
Grid inductor, L_g	1 mH
Grid resistor, R_g	0.1 Ω
Load inductor, L_1	58 mH
Load inductor, L_2	4 mH
Load capacitor, C_1	220 μF
Load resistor, R_1	5 Ω
Load resistor, R_2	110 Ω
Load resistor, R_3	30 Ω
Load resistor, R_4	35 Ω
Load resistor, R_5	40 Ω
Load resistor, R_6	50 Ω
Load resistor, R_7	25 Ω

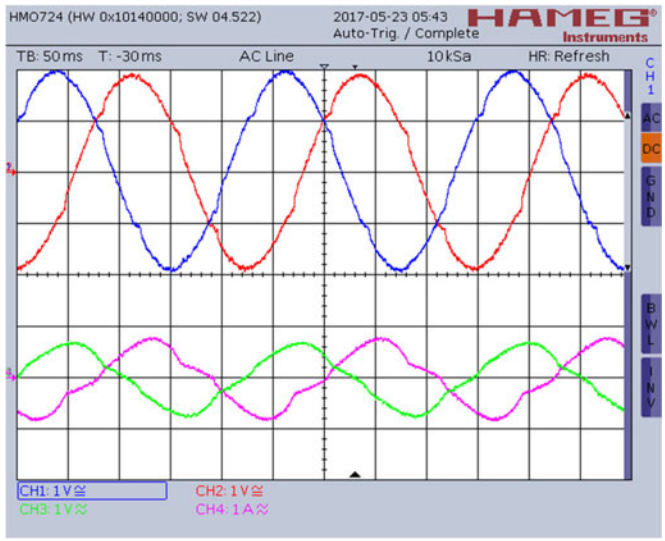

Fig. 8. Before implementing any compensation strategy: PCC voltage (90 V/div) and grid current (40 A/div) of phases *a* and *b*.

A. Scenario 1: Symmetrical and Sinusoidal Voltage Source With $v_a = 127\angle 0°$, $v_b = 127\angle -120°$ and $v_c = 127\angle 120°$

Fig. 9 presents the waveforms of voltages and currents measured at the PCC of Fig. 1, under symmetrical and sinusoidal voltage conditions. In Section V-A1–V-A5, the CHMI starts operating as an active filter showing the waveforms and their quantitative values for some of the more elucidative compensation strategies. Note that the current circulating in the CHMI differs in each strategy.

1) Reactive Current Compensation: In this case, the aim is to attenuate the reactive power, as defined in (7b). Thus, the current references for the SAPF should be (i_r^b), added the charging current of the H-bridge dc-side capacitors (i^*_{pabc}). From the CHMI terminal voltages and currents, shown in Fig. 9(a), the inverter is supplying reactive power or the reactive current component of the load since the CHMI currents are orthogonal to the terminal

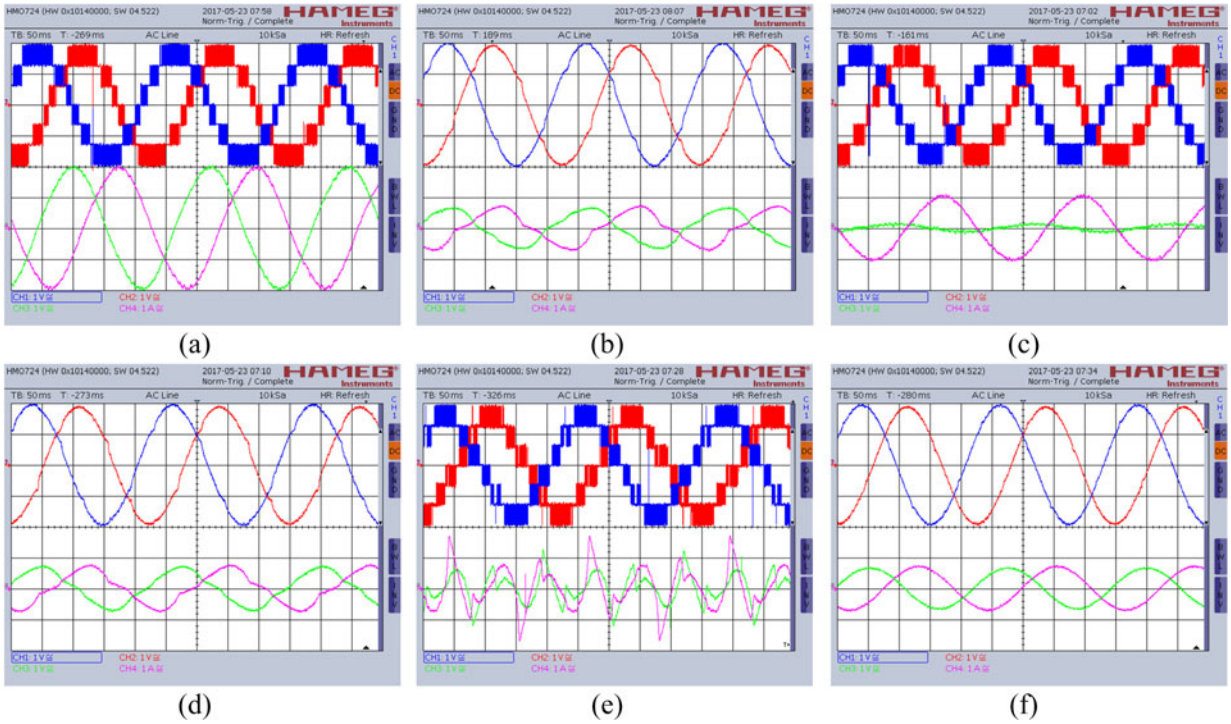

Fig. 9. (a) Compensation of i_r^b current: CHMI terminal voltage (110 V/div) and inverter current (5 A/div) of phases a and b. (b) Compensation of i_r^b current: PCC voltage (90 V/div) and grid current (40 A/div) of phases a and b. (c) Compensation of i^u current: CHMI terminal voltage (110 V/div) and inverter current (5 A/div) of phases a and b. (d) Compensation of i^u current: PCC voltage (90 V/div) and grid current (40 A/div) of phases a and b. (e) Compensation of i_v current: CHMI terminal voltage (110 V/div) and inverter current (5 A/div) of phases a and b. (f) Compensation of i_v current: PCC voltage (90 V/div) and grid current (40 A/div) of phases a and b.

voltages. In other words, when the terminal voltages reach zero, the corresponding phase inverter currents reach their peak value. The resulting compensated PCC voltage and grid current waveforms are shown in Fig. 9(b). Notice that the compensated grid currents are unbalanced, distorted, and slightly out of phase with the voltages. The unbalance and nonlinearity can be explained due to the fact that the current reference sent to the active filter (i_r^b) is not related to these disturbances. There could be a minor remaining lag in the compensation because of the components of unbalanced reactive currents, which were not compensated, since reactive power is determined only by balanced reactive currents. If the total reactive currents ($i_r = i_r^b + i_r^u$) were applied as current references for the active filter, both the lag and the unbalance phenomena would be compensated.

2) Unbalanced Current Compensation: The load considered in the system imposes unbalance component to the grid's current. Therefore, the CPT, proposed in this paper, is used to extract the unbalance current/power component of the load. In this case, the goal is to compensate only the components of unbalanced current (i^u). The CHMI terminal voltages and currents are shown in Fig. 9(c).

Notice that the resulting compensated currents, shown in Fig. 9(d), remain nonsinusoidal and out of phase with the voltages, i.e., distorted and lagging behind the PCC voltages, but are practically balanced (same amplitude in all the phases).

3) Harmonic Current Compensation: At this case study, the CHMI starts compensating only the void currents (i_v). From Fig. 9(e), the inverter currents are nonlinear, whereas the compensated currents in Fig. 9(f) are quasi-sinusoidal, unbalanced, and not in phase with their corresponding voltages, indicating that the balanced active, balanced reactive, and unbalance current components of the load are supplied by the grid.

TABLE V
PCC POWER COMPONENTS, INVERTER AND GRID CURRENTS, AND POWER FACTOR UNDER POSSIBLE SELECTIVE COMPENSATION STRATEGIES

	Without Com.	Com. i_v	Com. i_r^b	Com. i^u
A(VA)	7302	7263	7144	7247
P(W)	6676	6700	7011	6683
Q(VA)	2654	2623	14	2649
N(VA)	931	937	977	5
D(VA)	916	185	962	914
I_{grid}(A)	36.6	36.4	34.9	36.3
I_{inv}(A)	0.0	5	13.7	4.7
λ	0.914	0.922	0.981	0.922

To simplify the quantitative analysis of the compensation strategies, Table V illustrates the values of the grid power portions from the CPT decomposition, the collective RMS values of the grid currents and SAPF, and the power factor of the three-phase system.

Notice that the currents circulating through the CHMI are different in each strategy, with the highest current for (i_r^b) compensation and the lowest for (i^u) compensation. As a result, if only current nonlinearities or current unbalances must be compensated, the installed filter (converter) can have almost three-fold lower power (in this particular case) than if it was designed to compensate balanced reactive current, which would directly

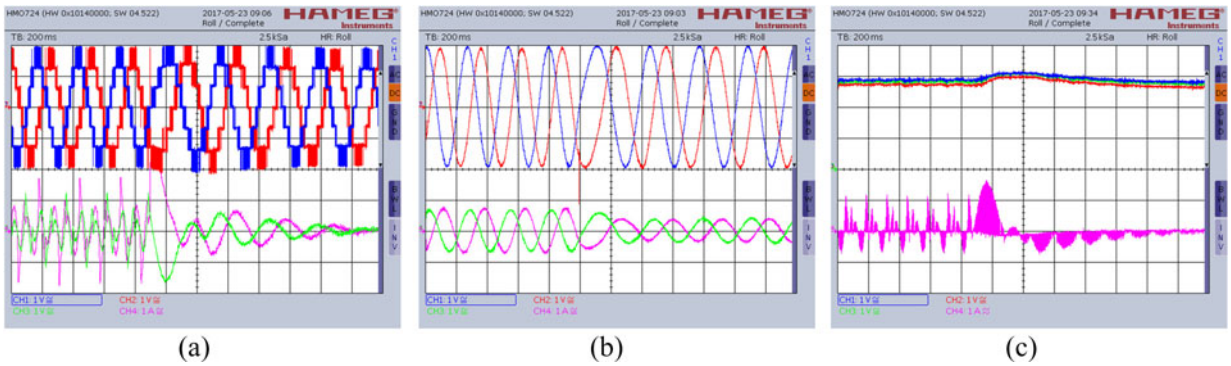

Fig. 10. Dynamic response of the SAPF CHMI to sudden changes in the load. (a) CHMI terminal voltage (110 V/div) and inverter current (5 A/div) of phases *a* and *b*. (b) PCC voltage (90 V/div) and grid current (40 A/div) of phases *a* and *b*. (c) H-bridge dc-link regulated voltages (25 V/div) of phase *a* and dc-link current (12 A/div) of H-bridge *a*1.

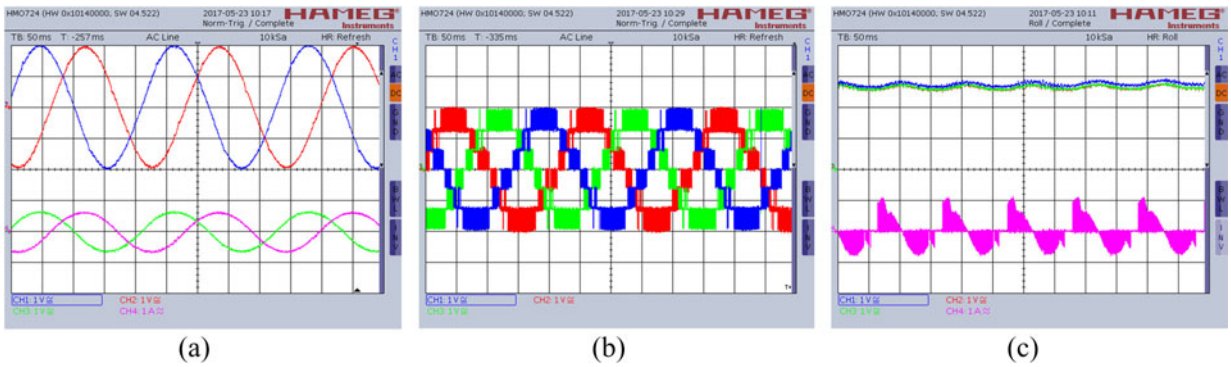

Fig. 11. Compensation of i_{na} current under symmetrical and sinusoidal voltage source. (a) PCC voltage (90 V/div) and grid current (40 A/div). (b) CHMI terminal voltages (110 V/div). (c) H-bridge dc-link regulated voltages (25 V/div) of phase *a* and dc-link current (12 A/div) of H-bridge *a*1.

affect the financial cost of an active filter. It is important to indicate that for each case of compensation, only the portion of power selected for compensation underwent significant changes in value, which establishes the selectivity and decoupling of the current components due to the orthogonality of the CPT decompositions.

From Table V, it seems that the compensation of (i_v) still leaves some deviation in the value of the *D* component. The explanation for this behavior is because the load used for verification of our system is highly distorted. The harmonic current has sharp peaks of 8 A, shown in Fig. 9(e), and leaves some distortion on the PCC voltages after compensation in Fig. 9(f). Therefore, this deviation is mainly due to the limits imposed by the current controllers, not the CPT decomposition.

4) Dynamic Performance of the CHMI Under a Load Switching Event: The dynamic performance of the SAPF CHMI in response to a sudden change in the load is depicted in Fig. 10. Originally, the system is under the load configuration illustrated in Fig. 1. From the CHMI terminal voltages and currents, shown in Fig. 10(a), the inverter is originally supplying the load void currents (i_v). The resulting compensated PCC voltage and grid current waveforms, shown in Fig. 10(b), are quasi-sinusoidal, unbalanced, and not in phase with their corresponding voltages. Suddenly, the nonlinear part of the load is switched OFF and the corresponding void current supplied by the CHMI decreases to zero. The compensated currents in Fig. 10(b) are also reduced by almost half since the provided current components by the grid only belong to the linear part of the load. Fig. 10(c) presents the H-bridge dc-link voltages of phase *a* (channels 1, 2, and 3) and the dc-link current of H-bridge *a*1 (channel 4). The three module dc-link voltages are controlled at the reference value, whereas the inverter supplies void load power. After the load step occurs, the dc-link voltages undergo very little variations during the transient time and reach the steady-state condition. Therefore, the dc-link voltages are well regulated despite the load switching event, and the disturbances are damped immediately. Hence, the closed-loop system is robust to the changes in the load configuration and dynamic properties. The dc-link current of H-bridge *a*1 in Fig. 10(c) has subsequently positive and negative values, which shows that its dc-link capacitor $C_{\rm dc}$ is charging and discharging all the time in order to regulate its dc bus voltage at 70 V. However, the dc-link current reaches zero after the nonlinear part of the load is switched OFF since the CHMI supplies zero current in Fig. 10(a) after the transient as there is no load distortion or void currents.

5) Nonactive Current Compensation: In Fig. 11, the CHMI is set to compensate nonactive current components of the load current. This current component is associated with all the disturbances created by the load (reactive currents, asymmetries,

TABLE VI
PCC POWER COMPONENTS, INVERTER AND GRID CURRENTS, AND POWER FACTOR THROUGH THE NONACTIVE COMPENSATION—CASE 1

	Without compensation	With compensation of i_{na}
A(VA)	7302	7052
P(W)	6676	7044
Q(VA)	2654	12
N(VA)	931	11
D(VA)	916	188
I_{grid}(A)	36.6	34.5
I_{inv}(A)	0.0	15.2
λ	0.914	0.999

imbalances, and nonlinearities), and is formed by $(i_r^b + i^u + i_v)$. Fig. 11(a) depicts the PCC voltages and the resulting compensated grid current waveforms under symmetrical and sinusoidal voltage condition. The source currents in this compensation strategy are the load balanced active current components (i_a^b), which are practically sinusoidal, balanced, and in phase with the voltages, describing the proper condition for an electric system. In Fig. 11(b), the CHMI terminal voltages $(v_{o,abc})$ are presented. The scaling for terminal voltages is 110 V per division. The CHMI terminal synthesizes a seven-level output voltage with symmetrical modules. Fig. 11(c) presents the H-bridge dc-link voltages of phase a (channels 1, 2, and 3) and the dc-link current of H-bridge $a1$ (channel 4). The three module dc-link voltages are controlled at the reference value, whereas the CHMI contains nonactive current component under symmetrical and sinusoidal voltage condition. The dc-link voltages have higher ripples as the CHMI supplies unbalance power component of load.

The dc-link current of H-bridge $a1$ in Fig. 11(c) has pulsating shape showing its dc-link capacitor C_{dc} is charging and discharging in order to regulate its corresponding dc bus voltage at 70 V.

Table VI illustrates the values obtained through the compensation of nonactive current, in which all the electrical disturbances are compensated (nonlinearities, unbalances, and reactive power). As it is shown, the current of the compensated system shows a lower value than that of the system without compensation, as the undesirable components of currents have been attenuated. Notice that the current that flows through the active filter may be up to three times higher than that of the compensation strategy for void or nonlinear current. This information is important from a financial perspective.

B. Scenario 2: Asymmetrical and Sinusoidal Voltage Source With $v_a = 106\angle 0^\circ$, $v_b = 127\angle -120^\circ$ and $v_c = 116\angle 120^\circ$

To evaluate the proposed compensation strategies for a case in which the source voltages have not been idealized, an asymmetrical and sinusoidal voltage source is considered. The CHMI operates as an active filter using the CPT, supplying all the undesirable components of the load (balanced reactive, unbalanced, and harmonics), that is $(i_r^b + i^u + i_v)$. Fig. 12 illustrates the voltages and currents at the PCC, after the compensation of nonactive currents, whereas the grid supplies the balanced active current components of the load (i_a^b). The compensated currents are sinusoidal, unbalanced due to the asymmetrical

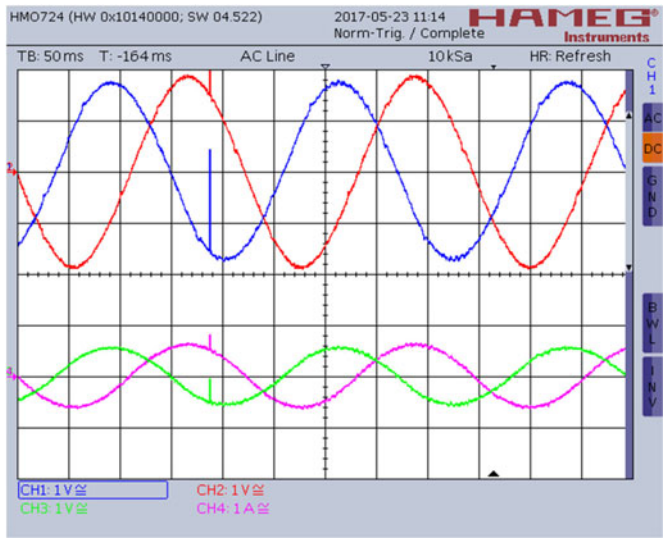

Fig. 12. Compensation of i_{na} current under asymmetrical and sinusoidal voltage source: PCC voltage (90 V/div) and grid current (40 A/div).

TABLE VII
PCC POWER COMPONENTS, INVERTER AND GRID CURRENTS, AND POWER FACTOR THROUGH THE NONACTIVE COMPENSATION—CASE 2

	Without compensation	With compensation of i_{na}
A(VA)	6005	5811
P(W)	5490	5808
Q(VA)	2169	11
N(VA)	782	12
D(VA)	763	157
I_{grid}(A)	32.9	31.1
I_{inv}(A)	0.0	13.7
λ	0.914	1

voltage source, and in phase with their corresponding voltages, as in the case of a balanced resistive load.

It is because that the CPT decouples the load and supply responsibility and quantifies the number of resistive characteristics of the load under various supply voltage conditions [16].

From Table VII, one can see that all the load disturbances were compensated. Notice that the slight deviations in the values of the powers are due to the limits imposed by the controllers used here.

C. Scenario 3: Symmetrical and Nonsinusoidal Voltage Source With 5% of Fifth and Seventh Harmonics

The evaluation of the proposed compensation strategies for symmetrical and nonsinusoidal voltages is considered in Fig. 13, where the CHMI is set to compensate nonactive or undesirable components of the load (balanced reactive, unbalanced, and harmonics) that is $(i_r^b + i^u + i_v)$. Having the CPT supply, the nonactive currents of the load, the deterioration of the supplied current by the grid is only due to the imposed voltage distortion, because the generated current emulates a balanced resistive load. Fig. 13 illustrates the voltages and currents at the PCC after the compensation of nonactive currents. The source current contains the balanced active current component of the load.

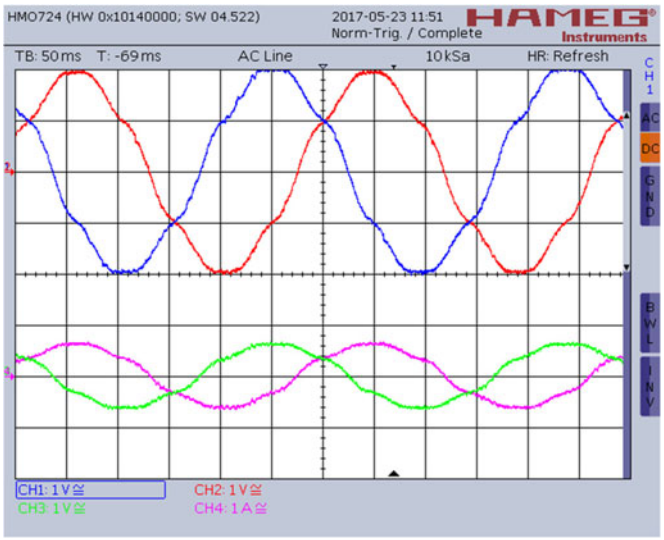

Fig. 13. Compensation of i_{na} current under symmetrical and nonsinusoidal voltage source: (a) PCC voltage (90 V/div) and grid current (40 A/div).

TABLE VIII
PCC POWER COMPONENTS, INVERTER AND GRID CURRENTS, AND POWER FACTOR THROUGH THE NONACTIVE COMPENSATION—CASE 3

	Without compensation	With compensation of i_{na}
A(VA)	7313	7015
P(W)	6631	7008
Q(VA)	2764	12
N(VA)	922	7
D(VA)	1004	162
I_{grid}(A)	36.5	34.2
I_{inv}(A)	0.0	15.8
λ	0.907	0.999

The results illustrated in Table VIII establish the effectiveness of the compensation of nonactive current under extreme voltage condition. It is demonstrated that the portion of the entire disturbance undergoes a significant change in its value when compared with the values of uncompensated loads.

VI. COMPARISON OF CPT, PQ, AND SRF CONTROL METHODS

In this section, the similarities and differences among the CPT and other popular current decomposition strategies, named PQ and DQ, are analyzed from the performance perspective in active power filter for three-phase four-wire loads. For the sake of brevity, the authors refer to related publication [16] for more details regarding the theoretical formulations of PQ, CPT, and DQ, as well as their power and current decompositions.

For symmetrical and sinusoidal operation, choosing one of the considered decomposition methods (CPT, PQ, and DQ) will substantially result in different current injections when using selective compensation strategies, especially when the instantaneous capability of the inverter is limited. In the CPT technique, $(i^u + i_v)$ includes unbalanced and harmonic components associated with single- and intraphase loads, whereas in the PQ theory, $(i_{\tilde{p}} + i_{\tilde{q}})$ includes unbalanced and harmonic components of intraphase loads only, and (i_0) contains linear and nonlinear components of single-phase loads. In other words, the results of applying $(i^u + i_v)$ or $(i_{\tilde{p}} + i_{\tilde{q}} + i_o)$, respectively, from CPT and PQ methods are the same. Note that in the PQ technique, unbalanced and harmonic components of intraphase loads cannot be separated, whereas this is not the case in the CPT technique. On the other hand, in the DQ technique (i_{Ndqf}) is associated with the unbalanced component of the intraphase loads, (i_h) is related to the harmonics of the intraphase loads, and (i_0) contains linear and nonlinear components of single-phase loads. Notice that in the CPT technique, it is not necessary to apply any reference frame transformations.

Under asymmetrical voltages, the results from PQ, CPT, and DQ can be very different, even if considering the compensation of all disturbing components from each method. The resulting currents after compensation of all load undesirable components using the CPT are sinusoidal unbalanced and in phase with the voltages (i_a^b). This occurs because (i_a^b) follows the measured voltages. When using the PQ theory, the resulting currents after compensation of all undesirable load currents $(i_{\tilde{p}})$ is distorted, in order to keep constant real power (average active currents) from the source. On the other hand, if using the DQ method, the resulting currents after compensation of all load undesirable currents are ideally sinusoidal, balanced, and in phase with voltages.

Under symmetrical and nonsinusoidal voltages, if the CPT is used to compensate all the undesirable components of the load current, the deterioration of the resulting compensated currents is only due to the imposed voltage distortion, because the generated current emulates a balanced resistive load (i_a^b). Using the PQ theory, the resulting compensated currents after compensation of all load current disturbing components $(i_{\tilde{p}})$ are not proportional to the voltage waveforms. As previously explained, the resulting currents are distorted, in order to maintain constant real power from the source. Therefore, other harmonic frequencies may appear in the supplied currents, apart from those in the source voltages. Using the DQ control method, the supplied grid currents after compensation of load unwanted current components (i_{Pdf}) are sinusoidal, balanced, and in phase with the fundamental component of their corresponding voltages (fundamental active positive, sequence). Due to nondistorted voltage drops through the line impedances in this case, the magnitudes of the load voltage harmonics are the same as those from the source voltages, forcing the system to sense the load solely at the fundamental frequency. It means at other frequencies, the load behaves as infinite impedance, because no current can flow at those frequencies. In the very common case of power factor correction capacitors, connected close to the active filter, at least one resonant frequency would be defined. Thus, the lack of damping at this frequency may lead to a dangerous condition concerning PCC voltage resonance. Moreover, the accuracy of DQ method is highly dependent on the PLL, especially under distorted voltages.

VII. CONCLUSION

This paper proposes the use of a cascaded multilevel shunt converter as a flexible power conditioner, aiming to selective compensation of disturbing current components extracted using the CPT. Using multilevel converters has several merits, e.g.,

the modularity in the system configuration with increased reliability, also allowing the use of independent dc-link voltages. These features by themselves already made this topology an ideal candidate for medium- and high-power applications. Also, the developed control strategy regulates the output current by tracking references provided by the CPT, without implementing any reference frame transformation.

The results illustrated in Tables V–VIII establish the feasibility and effectiveness of the selective strategies, showing that only the selected current disturbances are subjected to a significant change in its value when compared to the values of uncompensated loads. As a result, the proper choice of which portions should be compensated is a critical factor for the project since the actual nominal value directly influences the requirements of the active and passive elements of the EPP, and thus, the financial cost of its installation. Accordingly, the compensation strategy should meet the overall goals, within limits defined by regulatory standards, electricity operating constraints, and that is still favorable from the viewpoint of cost.

Moreover, CPT-based compensation strategies allow for the specific compensation of disturbances caused by loads (reactive current, asymmetry, unbalances, or nonlinearities). This is important regarding the appropriation of responsibilities in the case of smart microgrids or modern power grids.

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