GR-Noise Characterization of Ge pFinFETs With STI First and STI Last Processes
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Abstract—This letter characterizes the generation–recombination noise of Ge pFinFETs, for three different integration schemes: shallow trench isolation (STI) first strained devices; STI last for relaxed and strained ones. It is shown that many Lorentzians exhibit a VGS-independent and thermally activated characteristic frequency. This points out that the responsible defects are located inside the fin and they are found for all studied process conditions. One type of defect with a time constant value of 10 ms at room temperature is process-independent. Regarding the defects, their activation energies and hole capture cross sections have been extracted for fin widths varying from planar-like devices to narrow ones. It is shown that the STI last strained and relaxed devices yield a surface trap density three orders of magnitude above the typical value obtained for a blanket wafer.

Index Terms—Ge pFinFET, GR-noise characterization, STI first, STI last.

I. INTRODUCTION

THE beyond silicon materials (Ge and III-V) integration on a Si platform is challenging, one of the reasons being the large lattice mismatch with the silicon substrate [1]. Relaxation of the mismatch strain leads to the formation of a high density of misfit (MD) and/or threading dislocations (TD) [2]. When present, dislocations introduce deep states in the band gap, which give rise to generation-recombination of excess carriers [3], degrading several device parameters [4], [5] such as the threshold voltage (VTH), junction leakage current, and the inversion-layer mobility. Considering germanium for future node p-channel transistors, several strategies can be followed to reduce the TD density [6]. The different schemes studied in this work are outlined in Fig. 1. In the case of Shallow Trench Isolation (STI) last integration, post-deposition annealing after epitaxial growth of a thick relaxed Ge-on-Si layer typically yields a TDD in the low 107 cm−2 range. For the STI first case, one can speculate on the aspect-ratio-trapping of dislocations at the STI oxide sidewalls to result in a defect-free top device layer. However, this only works for narrow devices while wide fins should not benefit from the effect. Finally, application of a SiGe relaxed buffer (SRB) layer between the Si substrate and the Ge channel may yield a low TDD in the range of a few 106 cm−2 [7].

This letter provides a first comparison of the impact of the different Ge-on-Si integration schemes shown in Fig. 1 on the device performance, using GR noise as an evaluation tool. It is demonstrated that the Lorentzian parameters, i.e., characteristic frequency (fL) and the plateau amplitude (A0) can be used to study the lattice defects in the Ge fins, which are either grown-in (TDs) or processing-induced point defects. It is shown that the strained-Ge (sGe) fins on SiGe SRBs yield the lowest trap densities. At the same time, there is a tendency for smaller GR noise in narrow fins compared with more planar-like devices.

II. DEVICE CHARACTERISTICS

The p-type Ge FinFETs have been fabricated at imec/Belgium on 300 mm Si (100) wafers. The basic fabrication steps can be found in [8]. The FinFET device dimensions...
are a fin width ($W_{\text{fin}}$) that varies from 20 nm to 100 nm, geometric channel length ($L_G$) of 77 nm and fin height ($H_{\text{fin}}$) of 20 nm and 30 nm, STI first and last, respectively. The n-type in-situ doped relaxed buffers for both STI first ($\text{Si}_1-x\text{Ge}_x$, $x=75 \%$) and last ($\text{Si}_1-x\text{Ge}_x$, $x=70 \%$) have a doping concentration around $5 \times 10^{18} \text{ cm}^{-3}$. Except for the fabrication of the Ge channel, the device processing was identical. The gate stack is composed of a partially oxidized silicon passivation layer, HfO$_2$, and a TiN metal gate, the Capacitance Equivalent Thickness (CET) is $\sim 1.5 \text{ nm}$ for both STI first strained and STI last relaxed devices and $\sim 1.8 \text{ nm}$ for STI last strained.

### III. METHODOLOGY

A low-frequency noise spectrum is basically composed by three elements, i.e., white noise at high(er) frequency $f$; $1/f^\gamma$ (or flicker noise) and a sum of Lorentzian components, also known as generation-recombination noise (GR). The latter can originate from traps in the gate oxide (so-called Random Telegraph Signals - RTSs) or in the depletion region of the transistor. Roughly speaking, RTS and bulk defects correspond with gate voltage ($V_{GS}$) dependent and independent Lorentzian parameters, respectively [9]. In the case of trap centers in the depletion region, one can derive an effective surface trap density for the GR centers $N_{\text{eff}}$ from the plateau amplitude of the gate voltage spectral density $A_i$, as in (1) [10]

$$A_i = \frac{q^2 N_{\text{eff}}}{W_{\text{eff}} L_G C_{\text{ox}}} \tau_i$$  

where $q$ is the elementary charge, $W_{\text{eff}}$ is the effective width (defined as the sum of $W_{\text{fin}}$ and two times the fin height), $L_G$ is the channel length and $C_{\text{ox}}$ is the capacitance density. Finally, the GR center time constant ($\tau_i$) is defined as $1/(2\pi f_{ci})$ [11]. The $f_{ci}$ can be easily extracted from the observed bumps in the noise power spectra multiplied times $f$. The $N_{\text{eff}}$ can be calculated from (1), considering the plateau from the gate voltage spectral density ($S_{VG}$), which is obtained from the ratio of the current power spectral density ($S_{ID}$) over the transconductance squared ($S_{ID}/\gamma^2$).

The temperature dependence of the GR characteristics can be expressed by using (2) [12]

$$\ln(\tau T^2) = \frac{E_T - E_V}{kT} + \ln\left(\frac{h^3}{4\pi^2 \sigma_p 6x^3 M_c m_e^5 m_h^{3/2} m_e^{1/2}}\right)$$

where $h$ is the Planck constant; $m_e^*, m_h^*$ are the effective mass of electrons and holes respectively, and $M_c$ is the number of conduction band energy minima. From the $\ln(\tau T^2)$ as a function of $(1/kT)$ one extracts the trap activation energy ($\Delta E$) and the hole capture cross section ($\sigma_p$), from the slope and y-intercept, respectively.

### IV. DISCUSSION AND RESULTS

Fig. 2 shows the GR-noise time constant ($\tau$) as a function of the gate voltage bias ($V_{GS}$) for different fin widths. One can observe that $\tau$ is $V_{GS}$-independent for the three different Ge pFinFETs processes, which strongly indicates that the defects are located in the depletion region, in other words: inside the fin. In addition, it is worth mentioning that the 30 nm wide STI-first strained pFinFET presents two different $V_{GS}$-independent GR centers, a fast and a slow one.

The latter dominates the weak inversion region ($\sim 10 \text{ ms}$), while the other the strong inversion one ($\sim 1 \text{ ms}$). Furthermore, it is possible to identify at least four $\tau$ values with the one around 10 ms not correlated with the Ge integration on silicon. As the front-end processing was the same for the different types of pMOSFETs, this could point to some common processing induced GR centers, i.e., related to S/D ion implantation and annealing, for example. Reference [13]
TABLE I

DEVICE PARAMETERS FOR DIFFERENT Ge pFinFET STI PROCESSES

<table>
<thead>
<tr>
<th>Process</th>
<th>$W_{fin}$ (nm)</th>
<th>$V_{GS}$ (V)</th>
<th>$V_{THR}$ (V)</th>
<th>$\Delta E$ (eV)</th>
<th>$\sigma_p$ (cm$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>STI first</td>
<td>30</td>
<td>0.2</td>
<td>0.45</td>
<td>0.47</td>
<td>$1.4 \times 10^{13}$</td>
</tr>
<tr>
<td></td>
<td>50</td>
<td>0.3</td>
<td>0.40</td>
<td>0.47</td>
<td>$1.5 \times 10^{19}$</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>0.5</td>
<td>0.10</td>
<td>0.15</td>
<td>$1.5 \times 10^{22}$</td>
</tr>
<tr>
<td>STI last</td>
<td>30</td>
<td>0.2</td>
<td>0.32</td>
<td>0.41</td>
<td>$1.7 \times 10^{18}$</td>
</tr>
<tr>
<td></td>
<td>50</td>
<td>0.3</td>
<td>0.23</td>
<td>0.23</td>
<td>$7.8 \times 10^{18}$</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>0.1</td>
<td>0.16</td>
<td>0.16</td>
<td>$1.2 \times 10^{18}$</td>
</tr>
<tr>
<td>STI last</td>
<td>30</td>
<td>-0.3</td>
<td>0.47</td>
<td>0.23</td>
<td>$1.4 \times 10^{16}$</td>
</tr>
<tr>
<td></td>
<td>50</td>
<td>-0.3</td>
<td>0.44</td>
<td>0.44</td>
<td>$1.7 \times 10^{17}$</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>-0.5</td>
<td>0.37</td>
<td>0.37</td>
<td>$3.5 \times 10^{16}$</td>
</tr>
</tbody>
</table>

* @ room temperature

The $\Delta E$ values in Table I are derived from LFN measurements and there is some scatter for the different processes, one might correlate the defect origin with TDs. Additionally, it should be remarked that the weak inversion is the common and $W_{fin}$-independent operation regime for the studied devices, where the substrate typically affects the GR noise [16].

Fig. 5 shows the impact of the different processes on the surface trap density as a function of fin width. Both STI last approaches (strained and relaxed) clearly present higher surface trap density ($N_{eff}$) levels compared to the threading dislocation density (TDD) for blanket wafers $\sim 2 \times 10^{10}$ cm$^{-2}$ [17] and $\sim 1 \times 10^{9}$ cm$^{-2}$ [18], respectively. The STI-last relaxed devices show the lowest $N_{eff}$ values thanks to the lower surface area compared to the other approaches.

The surface area values used for the $N_{eff}$ extraction are $2.5 \sim 5 \times 10^{3} \text{cm}^2$, $3.3 \sim 6.6 \times 10^{-9} \text{cm}^2$, $1.1 \sim 2.1 \times 10^{-9} \text{cm}^2$ for STI first, STI last strained and relaxed devices, respectively.

For the STI first process, there is no significant difference of $N_{eff}$ levels between narrow and wide devices, indicating that the SRB defect density value is lower than the obtained ones. Since most of the defects are trapped at the bottom of the trench due to the aspect ratio trapping (ART) and more efficiently in narrow trenches compared with the wide ones [19], the latter should present a higher trap density than for the narrow case. Furthermore, the STI-first devices present similar $N_{eff}$ values than the STI-last counterpart, indicating that threading dislocations may not be the predominant GR centers in this case, which suggests processing-induced point defects as the responsible GR centers.

V. CONCLUSIONS

From the GR noise observed in Ge pFinFETs fabricated by three different STI processes, it is concluded from the gate-voltage independence of the Lorentzian parameters that the responsible defects reside in the fin region. The trap density is is most likely not related to the better crystalline quality of the SiGe SRB. Furthermore, the ART effect, in the case of STI first, cannot be seen in the trap density. Finally, the responsible GR centers seem to originate from processing-induced point defects.
REFERENCES


