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Low Temperature Effect on Strained and Relaxed Ge pFinFETs STI Last Processes

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Ge pFinFETs, fabricated either with an STI last process on a Ge-on-Si virtual substrates or a SiGe strain-relaxed buffer, have been systematically evaluated at temperatures from 200 K down to 77 K. In the first cases, the Ge channel is relaxed, while in the second case, compressively strained fins have been obtained. Cryogenic testing shows to be an important tool for evaluating the static device performance parameters and it helps to resolve the impact of strain on the drain current. Apart from that, the off-state leakage in the subthreshold region can be evaluated as a function of temperature, showing that besides thermal Shockley-Read-Hall generation, other field-assisted mechanisms play a role.

Introduction

The lower effective mass of germanium compared to silicon makes it a reasonably attractive material for future high-performance applications, since high hole mobility material is required for p-type channel devices (1). In combination with the FinFET architecture, which presents a strong electrostatic coupling (2), it gives rise to a promising future device, namely, a Ge pFinFET. In order to reach the industry standards, Si-platform integration must be achieved for the Ge pFinFET devices. In this scenario, one of the main issues is keeping the extended defect density in the channel, i.e., of threading (TD) and misfit dislocations (MD), as low as possible, since they can play an import role in the device performance, i.e. the off-state leakage (I_{off}) (3). The presence of dislocations in the Ge layers results from the heterogeneous integration on a silicon substrate, giving rise to lattice and thermal mismatch between Si and Ge (4).

Focusing on hetero-epitaxy on Si, different techniques have been developed, such as either a thick strain-relaxed Ge layer directly on a silicon wafer (5) or a $Si_{1-x}Ge_x$ Strain Relaxed Buffer (SRB) layer on a Si substrate (6). The latter can be fabricated in two approaches. In the first case, an SRB is deposited between predefined Shallow Trench Isolation (STI) regions (7) followed by a strained Ge layer growth. In case the SRB is grown with an Aspect-Ratio (AR) greater than 3 most of the TDs will be trapped in the bottom part by the STI oxide sidewalls (8). The second approach is the growth of a thick SRB layer (~1 µm) on the Si wafer, followed by a thin strained Ge layer on the SRB. In that case, an optimized TD density in the SRB layer of ~ 10^6 cm^{-2} can be achieved (9). Active areas are then defined by a STI last process.

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This work analyses the influence of low temperature on static parameters of strained and relaxed Ge STI last pFinFETs, such as the threshold voltage (V_T), transconductance (gm) and subthreshold swing (SS). The temperature is varied from 200 K down to 77 K. A performance comparison between the strained and relaxed counterparts is carried out in order to investigate the strain and defect impact on the off-state leakage and the on-state current.

Device Characteristics

The gate stack was composed of a partially oxidized Si passivation layer, hafnium oxide (HfO_2) and TiN, the Capacitance Equivalent Thicknesses (CET) are 1.55 nm and 2.00 nm for relaxed and strained Ge pFinFETs, respectively. The temperature (T) impact was analyzed from 200 K down to 77 K using a micro-manipulated cryogenic & vacuum probe system for chips, wafers and device testing, i. e., ST-500 model from Janis. The devices used in this work have been fabricated on a p-type silicon substrate at imec/Belgium. There are two different STI last processes under evaluation, where both of them are schematically shown in Figure 1. The first one is the strained channel, whereby a thin Ge layer (~ 30 nm) has been grown on top of a thicker (1 µm) layer of $Si_{1-x}Ge_x$ (x = 70 %) strain-relaxed buffer (SRB) on a silicon wafer. The other is a relaxed channel, where a thicker Ge layer has been grown on top of the Si substrate. The planar device dimensions are fin width (W_{fin}) of 20 nm, geometric channel length (L_G) of 1 µm, fin height (H_{fin}) of 30 nm and 4 fins in parallel. All measurements were carried out in linear operation, i.e., drain voltage bias of (V_{DS}) = – 50 mV.

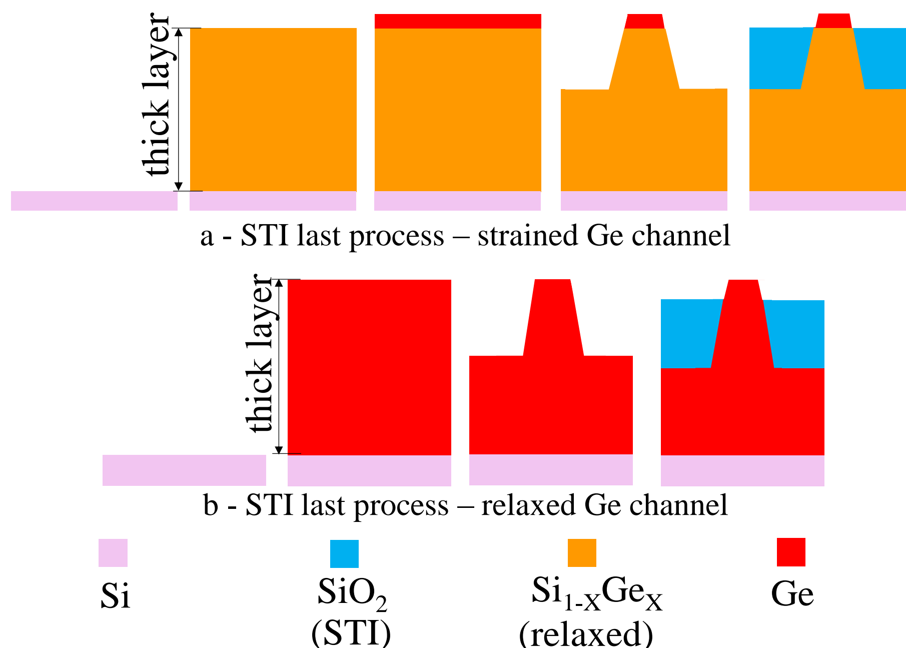

Figure 1. STI last processes schematic: a - strained and b - relaxed.

Results and Analysis

Figure 2 presents the drain current as a function of gate voltage (V_{GS}) for a temperature range from 200 K down to 77 K. One clearly observes that the drain current

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(I_{DS}) increases and the curves shift to more negative gate voltages upon cooling. The temperature reduction causes the Ge intrinsic carrier concentration to drop, which in turn results in a lower Fermi level and, consequently, a threshold voltage (V_T) shift towards positive values (10).

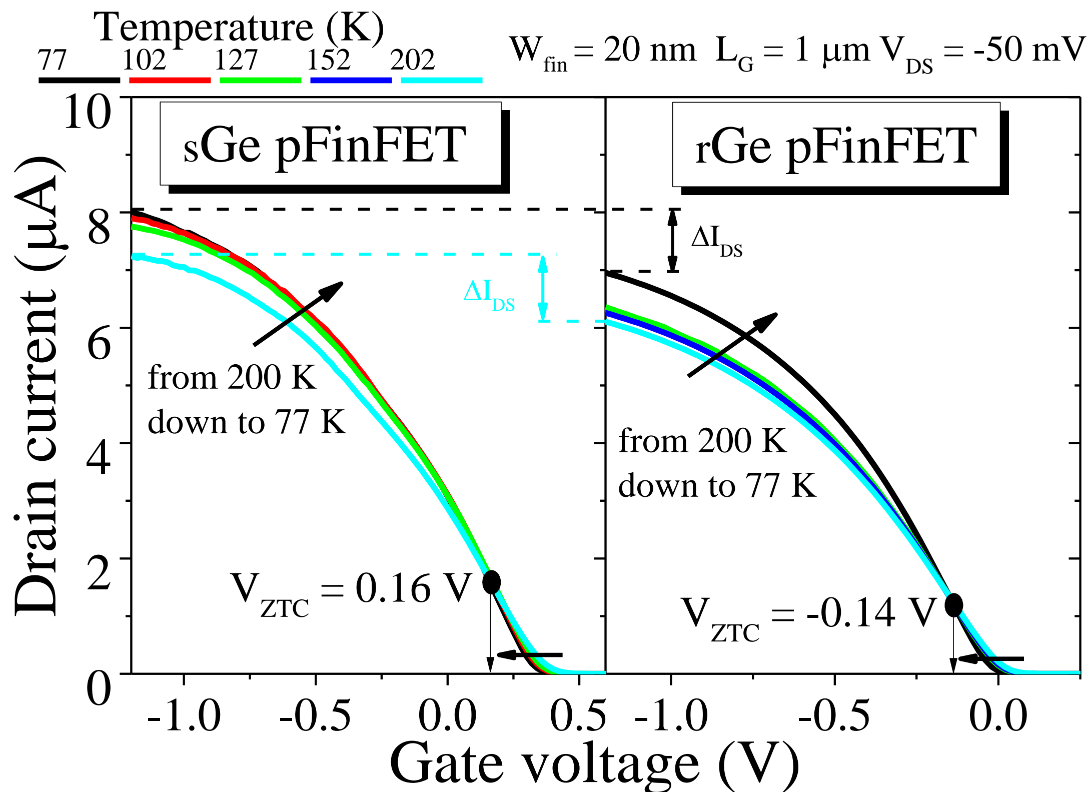

Figure 2. Drain current as a function of gate voltage in linear operation for a strained and relaxed Ge pFinFET, at different temperatures between 77 and 200 K. In the figure, the zero temperature coefficient point V_{ZTC} is indicated.

Figure 2 also reveals that the I_{DS} improves as the temperature reduces, which is associated to the carrier mobility increase, resulting from a lowering of the phonon scattering with T (11). Furthermore, the difference between the I_{DS} levels (ΔI_{DS}) for a strained device and relaxed is relatively constant (~ 1.1 µA) due to the impact of the compressive strain that boosts the hole mobility and the effect remains for different temperatures. Additionally, the Zero Temperature Coefficient (ZTC) is also presented in Figure 2. One shows that the ZTC voltage difference (ΔV_{ZTC}) between the strained and relaxed devices has similar value from the threshold voltage difference (ΔV_T) between the same devices at room temperature, i.e., around 0.3 V, due to the Ge bandgap reduction when a compressive strain is employed in p-channel Ge devices (12).

Figure 3 depicts the threshold voltage (V_T) as a function of the temperature for both strained and relaxed devices. While in Figure 2, the I_{DS} curves shift when the temperature changes, the temperature effect on V_T is not pronounced for both relaxed and strained devices, since the threshold voltage over temperature ratio ($\Delta V_T/\Delta T$) values are quite low and similar, 0.325 mV/K and 0.37 mV/K, respectively.

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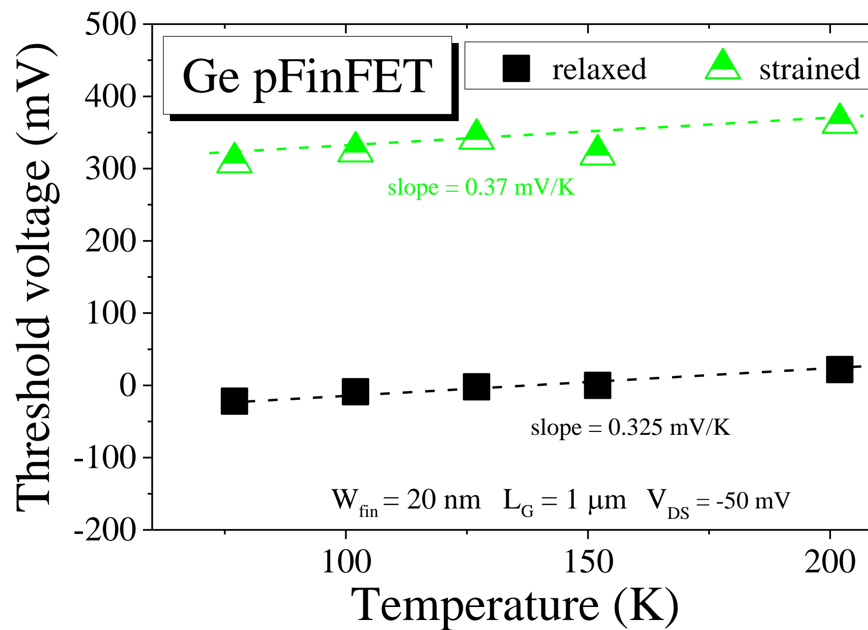

Figure 3. Threshold voltage as a function of temperature for strained and relaxed Ge pFinFETs, fabricated with an STI last process flow.

Figure 4 presents the normalized maximum transconductance (gm_{max}/W_{eff}) as a function of temperature for the studied STI last processes. One clearly observes that both strained and relaxed devices have a similar slope ($\Delta gm/\Delta T$), suggesting that the dominant mobility scattering mechanism is most likely the same. In contrast, the difference of around 1.1 µA in ΔI_{DS} is observed for the two devices in Figure 2, since the on current not only depends on the carrier mobility, but also on the gate capacitance. The latter is lower for the strained devices, which compensates the higher mobility for strained pFinFETs, resulting in gm_{max}/W_{eff} values similar to the relaxed devices.

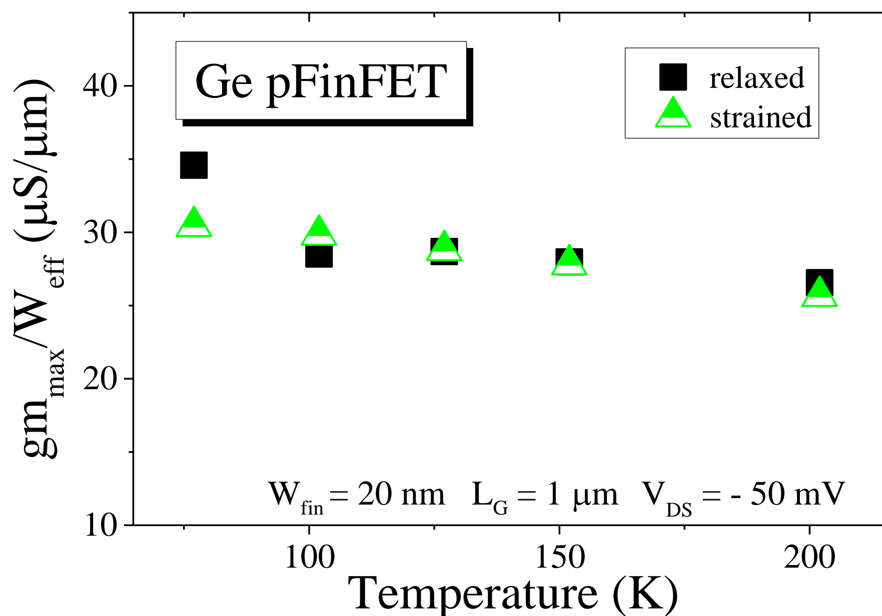

Figure 4. Normalized maximum transconductance as a function of temperature for strained and relaxed Ge pFinFETs, fabricated with an STI last process.

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Figure 5 shows the subthreshold swing as a function of temperature for the strained and relaxed devices. It can be noted that while the I_{DS} in the ON-region increases with lower temperature (Figure 2), the leakage current reduces due to the thermal activation of the carrier generation in the subthreshold region, as depicted in Figure 5. On the other hand, the slope for both strained and relaxed devices is different, pointing out that an additional field-assisted leakage mechanism also plays a role on the subthreshold swing.

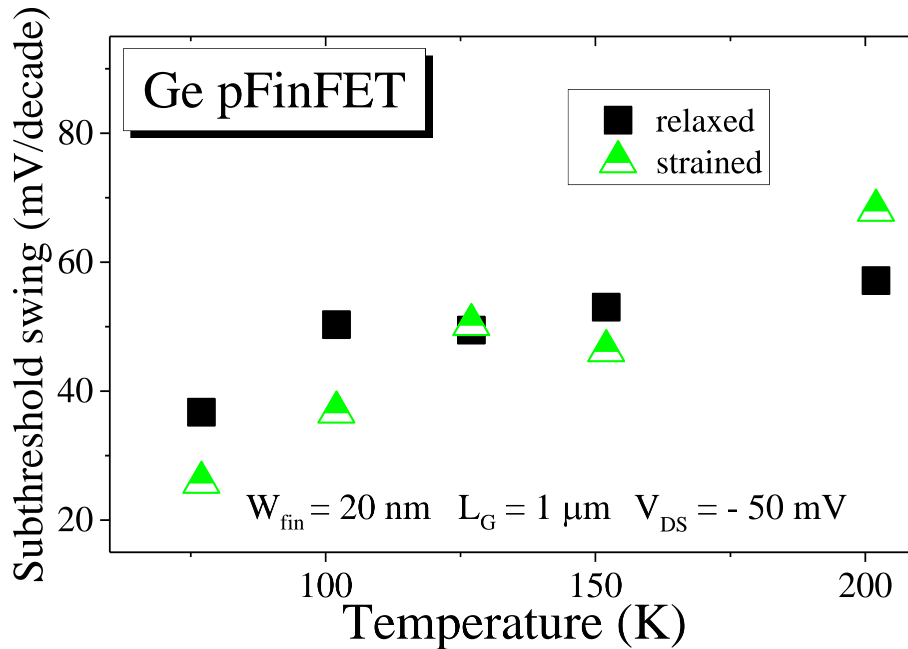

Figure 5. Subthreshold swing as a function of temperature for strained and relaxed Ge pFinFETs.

Conclusions

In summary, strained and relaxed long channel Ge pFinFET devices have been characterized for low temperature operation. The impact of compressive strain is shown on the drive current and threshold voltage, where in both cases the strained devices present higher values compared to the relaxed ones. On the other hand, the mobility scattering mechanism seems to be the same for both types of devices. Furthermore, the temperature dependence of the threshold voltage is similar for both, pointing out that it is a typical Ge coefficient. Finally, the different subthreshold swing behavior in both devices reveals that additional leakage generation mechanisms play a role in the subthreshold region, besides the thermal activation of the carrier generation.

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