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Analog parameters of solid source Zn diffusion $In_xGa_{1-x}As$ nTFETs down to 10 K

C Bordallo[1,2], J A Martino[2], P G D Agopian[2,3], A Alian[1], Y Mols[1], R Rooyackers[1], A Vandooren[1], A S Verhulst[1], Q Smets[1,4], E Simoen[1], C Claeys[1,4] and N Collaert[1]

[1] Imec, Kapeldreef 75, B-3001 Leuven, Belgium

[2] LSI/PSI/USP, University of São Paulo, Av. Prof. Luciano Gualberto, trav. 3, n° 158, 05508-010, Sao Paulo, Brazil

[3] UNESP, Univ. Estadual Paulista, Profa. Isette Correa Fontão, 305, 13876-750, Sao Joao da Boa Vista, Brazil

[4] KU Leuven, Kasteelpark Arenberg 10, B-3001 Leuven, Belgium

E-mail: caiobordallo@gmail.com

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Abstract

The analog parameters of $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ nTFETs with solid state Zn diffused source are investigated from room temperature down to 10 K. The $In_{0.7}Ga_{0.3}As$ devices are shown to yield a higher on-state current than the $In_{0.53}Ga_{0.47}As$ counterparts, and, consequently, a higher transconductance due to the lower bandgap. At the same time, the $In_{0.7}Ga_{0.3}As$ devices present higher output conductance values. The balance between these two factors results in a higher intrinsic voltage gain (A_V) for $In_{0.7}Ga_{0.3}As$ nTFETs at low gate bias and similar A_V for both devices at high gate voltage. The transconductance is reduced at low temperature due to the increase of the bandgap, while the output conductance is decreased (improved) upon cooling, which is related to the reduction of the drain dependence of the BTBT generation rate. The temperature influence is more pronounced in the output conductance than in the transconductance, resulting in an increase of the intrinsic voltage gain at low temperatures for both devices and bias.

Keywords: TFET, low temperature, analog parameters, current conduction mechanisms

(Some figures may appear in colour only in the online journal)

Introduction

In tunnel field-effect transistors (TFET), which are essentially gated p-i-n diodes, the carrier injection mechanism is band-to-band tunneling (BTBT) [1]. TFETs are promising alternatives for low power/low voltage applications due to the fact that the BTBT mechanism can overcome the theoretical sub-threshold swing (SS) limit imposed by thermal diffusion (60 mV dec^{-1} at 300 K) for metal-oxide-semiconductor field-effect transistors (MOSFET) [2–4]. TFETs with a steep SS below 60 mV dec^{-1} have already been experimentally demonstrated in [5].

Despite the fact that BTBT improves the switching speed of a transistor, Si-based TFETs present a very low on-state current (I_{ON}) due to the large and indirect bandgap of Si. The use of different source/channel materials with lower bandgap, as Si_xGe_{1-x} alloys [6–9] and III–V materials [10, 11], has been studied as a method for increasing I_{ON}.

Besides the strong potential for low power digital applications, recent studies have shown promising results for analog applications of TFETs [12–20]. The encouraging analog performance of TFETs is a result of the BTBT mechanism, which results in a very low output conductance (g_D) when compared to the g_D of a MOSFET [21]. For analog applications low values of g_D are important because it implies in lower influence of the drain voltage, resulting in a more constant drain current independent of the output charge. The lower g_D for TFETs holds as long as its channel length is sufficiently long to avoid drain induced barrier thinning [22].

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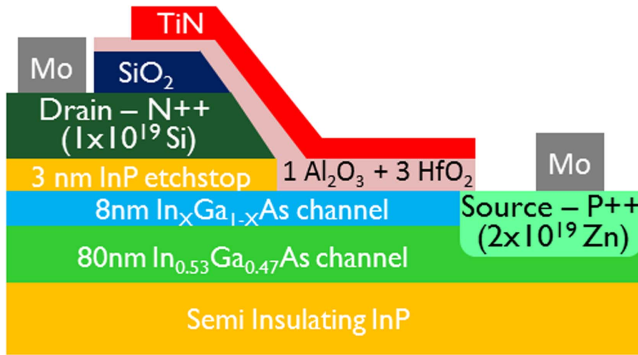

Figure 1. Schematic cross section of the $In_XGa_{1-X}As$ nTFET.

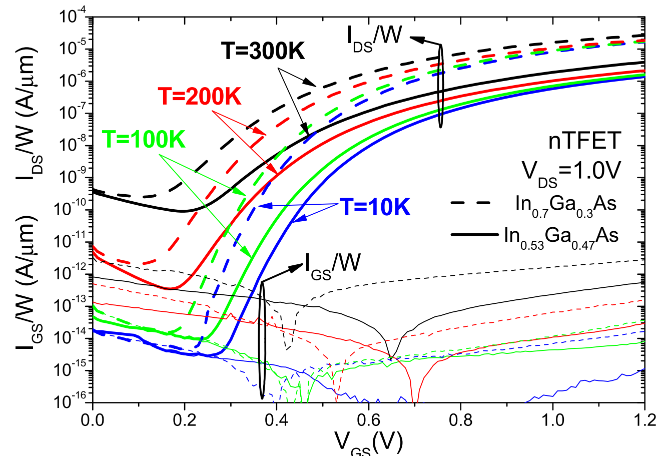

Figure 2. Experimental normalized I_{DS} and I_{GS} as a function of V_{GS}, for the $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ devices at temperatures ranging between 300 and 10 K.

TFETs are typically more sensitive to defects than MOSFETs, since trap-assisted-tunneling (TAT) and Shockley-Read-Hall generation (SRH) are important current components in the off state. A study of the influence of temperature (T) on TFETs enables to identify which of the conduction mechanisms is dominant [23]. SRH and TAT generation are thermally activated, implying that they reduce exponentially with lower T, while BTBT exhibits only a small temperature influence, mainly caused by temperature-dependent bandgap narrowing. At extremely low temperatures the TAT and SRH mechanism are suppressed, making it possible to analyze separately the BTBT.

Aware of the TFETs potential for analog applications, in this work, some important analog parameters of InGaAs TFETs are investigated in order to analyze its performance, from 300 K down to 10 K, for 2 different splits, one consisting of an $In_{0.53}Ga_{0.47}As$ channel, taken as the reference, and the other has an $In_{0.7}Ga_{0.3}As$ channel, with a reduced bandgap to boost I_{ON}. The analog parameters analyzed in this work are the transconductance in saturation (gm), output conductance, transistor efficiency (gm/I_{DS}) and the intrinsic voltage gain (A_V).

Device characteristics

The studied devices are n-type $In_XGa_{1-X}As$ homojunction TFETs with $x = 0.53$, 0.7, fabricated by using Zn solid-source diffusion of the source [25]. The device follows the gate first approach from the University of Tokyo [11, 24], and it was optimized by Alian *et al* [25].

Two different splits were analyzed, one device with an uniform $In_{0.53}Ga_{0.47}As$ channel and the other with an extra 8 nm layer of $In_{0.7}Ga_{0.3}As$ on top of the $In_{0.53}Ga_{0.47}As$ material [25]. A schematic representation of the device is shown in figure 1.

The gate stack is composed of 1 nm Al_2O_3/3 nm HfO_2 with TiN as the metal gate. This results in an estimated equivalent oxide thickness of 1.5 nm. The drain is doped with Si (N++) *in situ* during the MBE growth, and the source is doped with Zn (P++) using spin-on glass diffusion at 500 °C for 1 min. The transistor gate width (W) and length (L) are 400 μm and 5 μm, respectively.

The DC measurements were performed at temperatures of 300, 200, 100 and 10 K, using a LakeShore CPX probe station and a HP4156 precision parameter analyzer.

Analysis and discussion

Figure 2 presents the experimental normalized drain current (I_{DS}/W) and the normalized gate current (I_{GS}/W), as a function of the gate voltage (V_{GS}) for $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ nTFETs, for $V_{DS} = 1.0$ V at temperatures ranging between 300 and 10 K. The on-state current for the $In_{0.7}Ga_{0.3}As$ device is higher than for the $In_{0.53}Ga_{0.47}As$ counterpart due to the higher BTBT current for the higher In content channel. This increase is caused by the smaller bandgap, better electrostatic coupling and also can be related to higher active doping concentration [26], which reduce the tunneling length.

Taking into account the effect of the temperature reduction, one can observe that, in contrast to a MOSFET where the mobility increases, all the current conduction mechanisms decrease with lower temperature, resulting in both lower I_{ON} and I_{OFF} currents in the TFETs. However, the I_{OFF} decreases relatively more than the I_{ON}. This behavior can be explained by the different temperature dependence of each current conduction mechanism of the TFET. The temperature dependence is represented by the equations (1)–(3), which are, respectively, the simplified current model of the, TAT and BTBT mechanism [27–29].

$$J_{SRH} \cong C1_{SRH} . e^{\left(-\frac{\frac{E_g}{2}+(E_d-E_i)}{k.T}\right)}, \quad (1)$$

$$J_{TAT} \cong C1_{TAT} . e^{\left(-\frac{\frac{E_g}{2}+(E_d-E_i)}{k.T}\right)}, \quad (2)$$

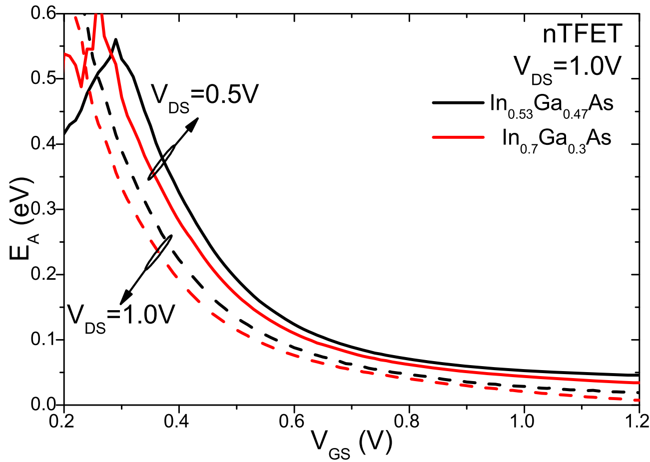

Figure 3. Extracted activation energy as a function of V_{GS}, for the $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ devices.

$$J_{\mathrm{BTBT}} \cong \cdot \frac{C1_{\mathrm{BTBT}}}{E_g} \cdot e^{\left(-C2_{\mathrm{BTBT}} \cdot \frac{E_g^{3/2}}{\xi}\right)}, \qquad (3)$$

where J is the current density, $C1_{\mathrm{sRH}}$, $C1_{\mathrm{TAT}}$ and $C1_{\mathrm{BTBT}}$ are pre-exponential constants for the simplification of the expressions, E_g is the bandgap, E_d is the defect energy level, E_i is the intrinsic energy level, k is the Boltzmann constant, ξ is the total electric field and $C2_{\mathrm{BTBT}}$ is an exponential constant for the J_{BTBT} simplification.

One can immediately notice that the SRH and TAT components, which are responsible for the I_{OFF}, are exponentially depending on T, resulting in a high variation with the temperature. In contrast, the BTBT current, which governs I_{ON}, has only an indirect influence of the temperature, which is caused by the bandgap increase at lower T. This results in a smaller relative variation of the BTBT components when compared with the TAT and SRH ones.

This smaller relative variation can also be observed in the activation energy (E_A), presented in figure 3, which represents the logarithm variation of the current as a function of the inverse temperature. One can notice that for lower V_{GS}, for which SRH and TAT mechanism are dominants, E_A is higher, indicating high temperature dependence. On the other hand, for high V_{GS}, region where BTBT is the dominant mechanism, E_A presents low values due to its low relative temperature dependence. When comparing both different devices ($In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$) it is noticeable that the $In_{0.7}Ga_{0.3}As$ device is less temperature dependent, i.e., presents higher BTBT component, caused by its lower tunneling length.

From figure 2 it is also possible to observe that for temperatures below 100 K the SRH and TAT components of the current are so reduced that the I_{OFF} starts to be limited by the gate current I_{GS}. The dominant conduction mechanism of I_{GS} for very thin gate dielectrics is the direct tunneling across the oxide bandgap (Fowler-Nordheim), therefore, its current density can be modeled by the equation (4) [30–32]. This conduction mechanism causes lower temperature dependence of I_{GS}, which is caused mainly by the bandgap variation, than in the SRH and TAT mechanisms, resulting in a limitation of the I_{OFF} by the I_{GS} at low temperatures.

$$J_G \cong \cdot \frac{C1_{\mathrm{F\text{-}N}}}{E_g} \cdot e^{\left(-C2_{\mathrm{F\text{-}N}} \cdot \frac{E_g^{3/2}}{\xi}\right)}, \qquad (4)$$

where J_G is the gate current density, $C1_{\mathrm{F\text{-}N}}$ and $C2_{\mathrm{F\text{-}N}}$ are the pre-exponential and exponential constants, respectively, for the simplification of the expressions.

Figure 4 presents the normalized gm/W as a function of the temperature for both studied devices. The devices in figure 4(a) are biased at a drain voltage (V_{DS}) of 0.5 V, and in figure 4(b) at $V_{DS} = 1.0$ V. Both graphs also show data for two different gate biases, $V_{GS} = 0.5$ V and $V_{GS} = 1.0$ V. From this figure one observes that the transconductance in the

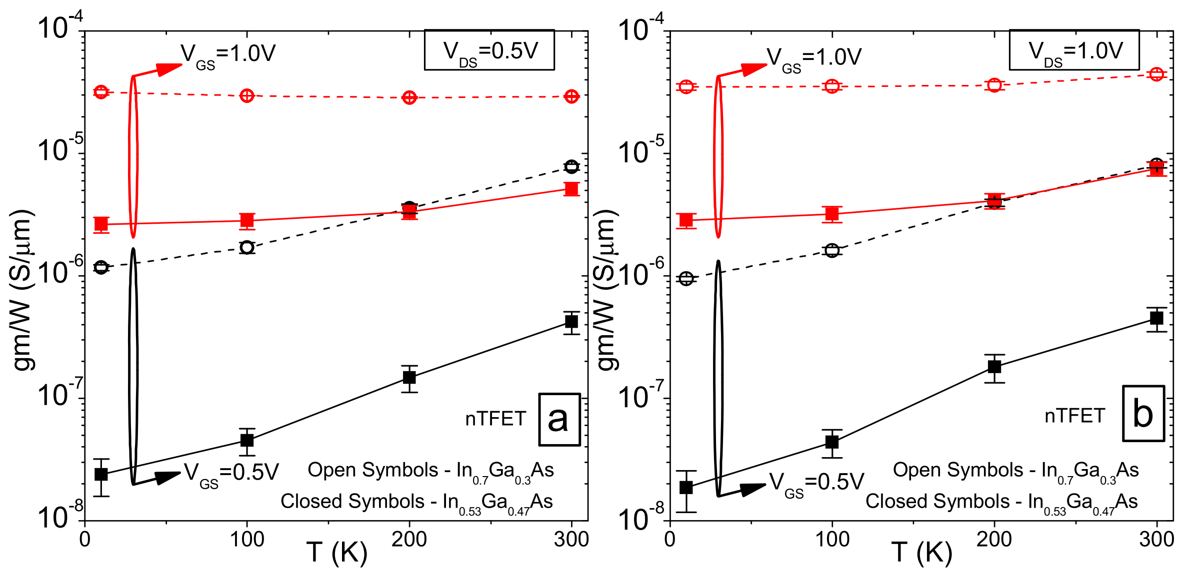

Figure 4. Experimental gm as a function of the temperature for the $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ devices, with $V_{DS} = 0.5$ V (a) and $V_{DS} = 1.0$ V (b).

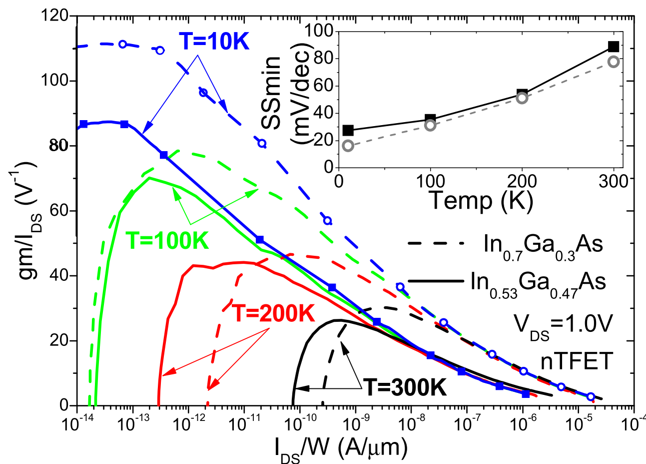

Figure 5. Experimental normalized gm/I_{DS} as a function of I_{DS}, for the $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ devices at temperatures ranging between 10 and 300 K. SS as a function of the temperature is shown in the inset graph.

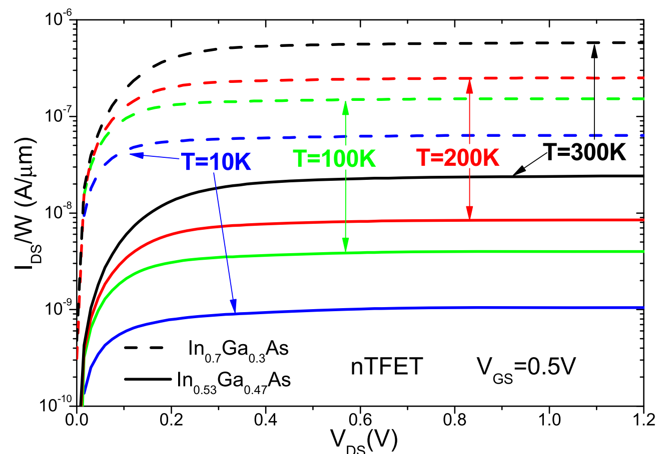

Figure 6. Experimental normalized I_{DS} as a function of V_{DS}, for the $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ devices at temperatures ranging between 10 and 300 K.

$In_{0.7}Ga_{0.3}As$ device is always higher than for the $In_{0.53}Ga_{0.47}As$ channel due to its lower bandgap.

For most experimental conditions in figure 4, gm decreases with lower T. However, for $V_{GS} = 1.0$ V and $V_{DS} = 0.5$ V the gm in the $In_{0.7}Ga_{0.3}As$ device tends to increase slightly at low temperatures. This could be related to the high series resistance (long channel device—5 μm), which decreases at low temperatures. The $In_{0.7}Ga_{0.3}As$ nTFET at this bias condition has a very high current), which means that the BTBT tunnel event is very efficient, and so it is likely that the channel series resistance starts to become observable, such that the reduction of the series resistance can result in an I_{ON} improvement at low T.

When comparing the impact of temperature for the different splits, it is noticeable that the $In_{0.7}Ga_{0.3}As$ device is less influenced than the $In_{0.53}Ga_{0.47}As$ counterpart. This lower temperature influence, which can also be observed in the E_A curve (figure 3), is caused by the higher BTBT component in this device, owing to its lower bandgap. For higher V_{GS} in both splits, where BTBT is even stronger, the same effect is noticed, resulting in a smaller temperature dependence compared to lower V_{GS} values.

The transistor efficiency (gm/I_{DS}) as a function of normalized I_{DS} for $V_{DS} = 1.0$ V, at temperatures ranging from 300 K down to 10 K, is presented in figure 5. For low I_{DS} values gm/I_{DS} is inversely proportional to the SS, which is presented in figure 5—inset. In this region, where gm/I_{DS} exhibits its highest values, the $In_{0.7}Ga_{0.3}As$ nTFET is better performing than the $In_{0.53}Ga_{0.47}As$ one, due to the smaller SRH and TAT influence, which enhances the SS.

Considering high I_{DS} values, the gm/I_{DS} is more dependent on the gm. In this region, as the gm is higher for the $In_{0.7}Ga_{0.3}As$ than for the $In_{0.53}Ga_{0.47}As$ channel, it also corresponds with higher gm/I_{DS}. In addition to the predominance at high currents of the BTBT, which is very weakly temperature dependent, both gm and I_{DS} decrease at low temperature in the same way, resulting in a very small variation of the gm/I_{DS} with temperature.

For $V_{GS} = 0.5$ V the high temperature dependence can also be observed in the I_{DS} as a function of V_{DS} (figure 6), and as the $In_{0.53}Ga_{0.47}As$ device has a higher bandgap, it is even more influenced by temperature. The plateau of this curve, i.e., the output conductance (figure 6), is also an important figure of merit in analog performance.

Figure 7 shows that for high V_{GS} values ($V_{GS} = 1.0$) an increase of g_D is observed, which is caused by the V_{DS} dependence of the effective energy window of overlap at the source–channel junction [33]. Energy window of tunneling is the energy window where the tunneling occurs, which is limited by the valence band of the source, the conduction band of the channel and the drain, and also the fermi levels of them. For high V_{DS} (figure 7(b)), this effective energy window is wider than for low V_{DS} (figure 7(a)), resulting in less V_{DS} dependence and reaching a saturation like region.

To better understand the effect of the temperature on the g_D, numerical simulations were performed using Sentaurus Device simulator [34]. The simulations were performed for the uniform $In_{0.53}Ga_{0.47}As$ channel device, considering the Dopant-dependent SRH, Schenk non-local TAT, non-local BTBT, and bandgap narrowing models, which parameters where obtained in [35]. Figure 8 compares the simulated and experimental I_{DS} as a function of V_{GS} for the $In_{0.53}Ga_{0.47}As$ nTFET, showing a good match between the experimental and the simulations. Among others, the output conductance has been obtained (figure 9), where the same tendency as the experimental result (g_D reduction for low temperatures) was observed.

Figure 10(a) presents the simulated energy band diagram (E_C, E_V) of a tilted cross section, which crosses the regions with highest BTBT generation (figures 10(b) and (c)), for three V_{DS} values, at room temperature and at 100 K. From this figure one can derive that due to the slight increase of the bandgap at lower T, the tunneling length increase. This behavior is more clearly shown in the zoom in of this graph, shown in the inset of figure 10.

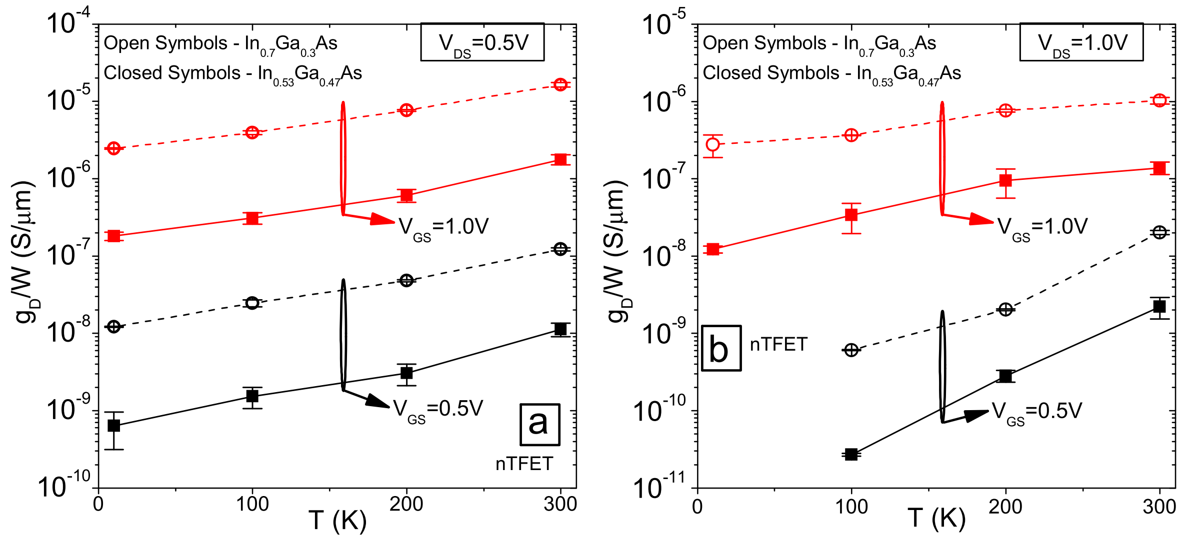

Figure 7. Experimental g_D as a function of the temperature for the $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ devices, with $V_{DS} = 0.5$ V (a) and $V_{DS} = 1.0$ V (b).

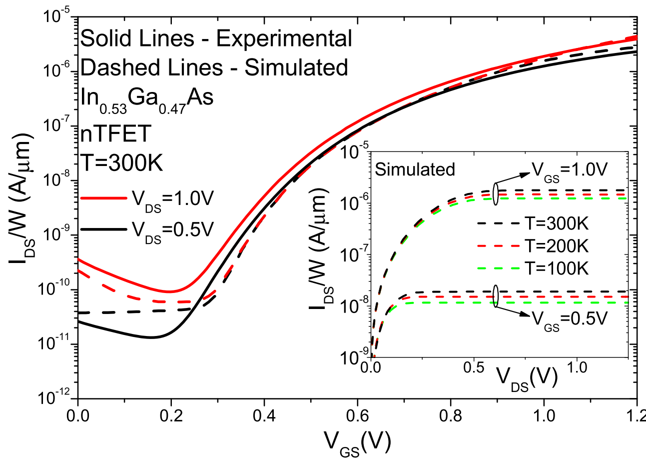

Figure 8. Experimental and simulated normalized I_{DS} as a function of V_{GS}, for the $In_{0.53}Ga_{0.47}As$ device. Simulated normalized I_{DS} as a function of V_{DS}, for the $In_{0.53}Ga_{0.47}As$ device at different temperatures.

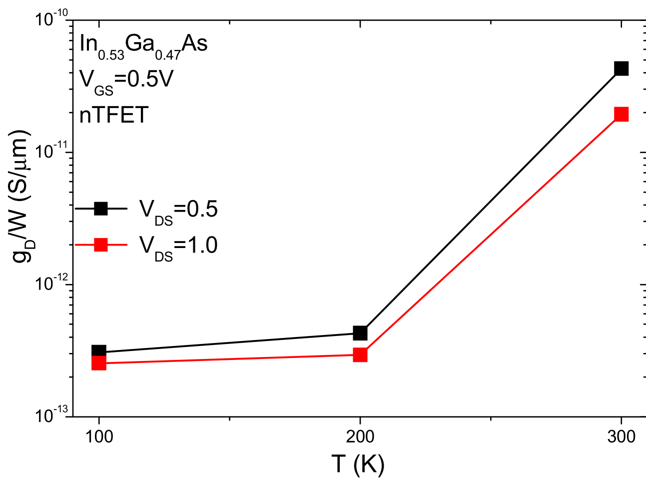

Figure 9. Simulated g_D as a function of the temperature for the $In_{0.53}Ga_{0.47}As$ device.

Figure 10(d) shows the BTBT generation rate at source/channel junction. One can observe from this figure that as a consequence of the small tunneling length increase at low temperature, the BTBT generation rate is reduced, which in turns results in a reduction of the BTBT current.

From figure 10(d) it is also possible to observe a reduction of the V_{DS} influence on the BTBT generation rate and, consequently, the BTBT current, at low temperatures, resulting in an improvement (reduction) of g_D, as can be found in figure 9.

An important figure of merit for the analog characteristics of transistors is the intrinsic voltage gain, obtained by equation (5). Figure 11 presents the experimental A_V as a function of the temperature for both $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ devices, with V_{DS} biased at 0.5 V (figure 11(a)) and 1.0 V (figure 11(b)). It is possible to observe that for low V_{GS} the $In_{0.7}Ga_{0.3}As$ presents higher A_V than the $In_{0.53}Ga_{0.47}As$ one due to the higher influence of BTBT caused by the lower bandgap. However, for high V_{GS} at low V_{DS} this $In_{0.7}Ga_{0.3}As$ device seems to suffer more from the series resistance, due to its higher current, resulting in a lower *gm* and A_V and also more influenced by the temperature.

$$A_V = 20 \cdot \log\left(\left|\frac{gm}{g_D}\right|\right). \quad (5)$$

The A_v analysis shows that there is a competition of factors between the *gm* degradation and g_D improvement (decrease) at low temperatures. For $V_{GS} = 1.0$ V, as gm experiences less relative influence of the temperature, the influence of the temperature on g_D is the predominant factor in A_V, resulting in its increase for low temperatures.

For low V_{GS} and at $V_{DS} = 0.5$ V, this competition of factors results in an A_V almost independent on temperature, because in this bias regime the gm is more affected by the temperature due to the lower influence of BTBT. For higher

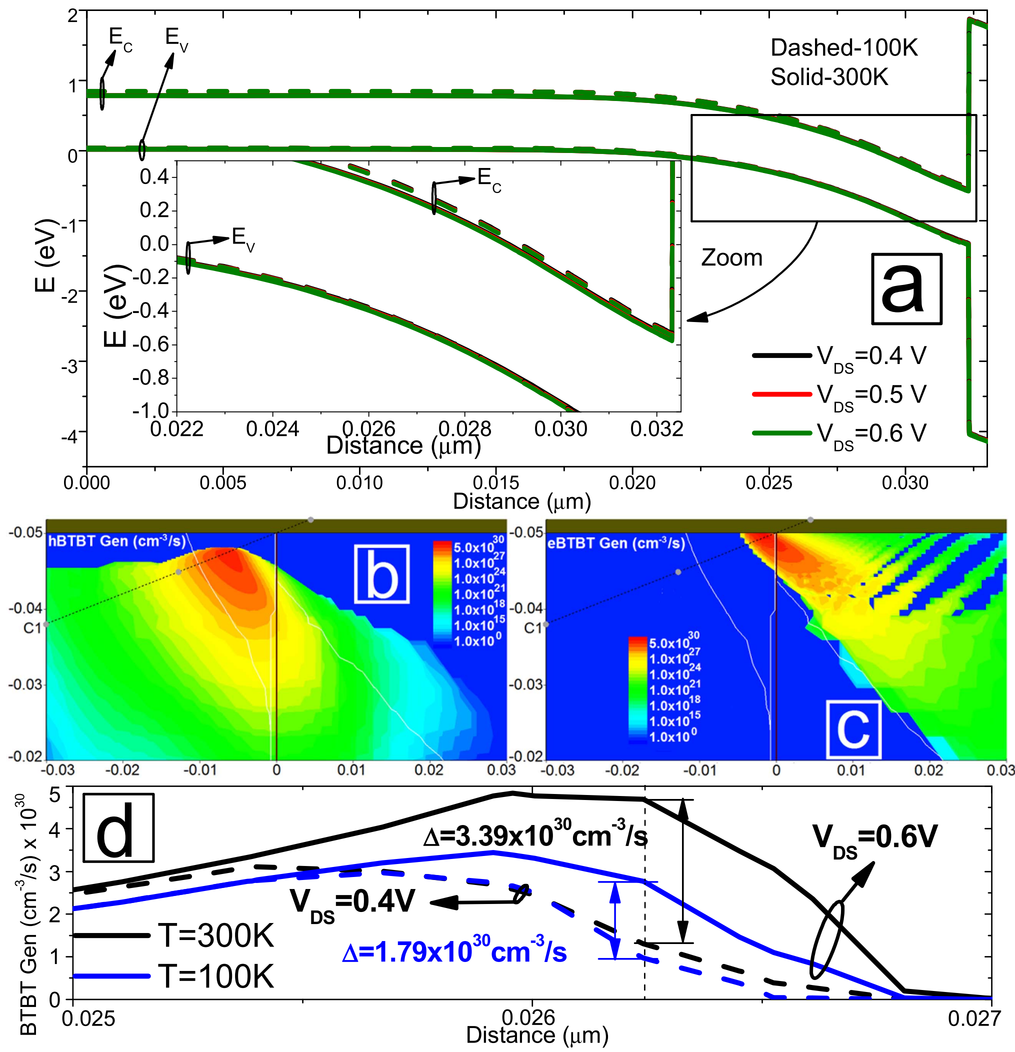

Figure 10. Simulated conduction energy and valence energy as a function of the distance of a tilted cross section (a), which cut crosses the maximum values of electron and holes BTBT generation rate (b) and (c). BTBT generation rate as a function of the cut distance for V_{DS} = 0.4 and 0.6 V (d).

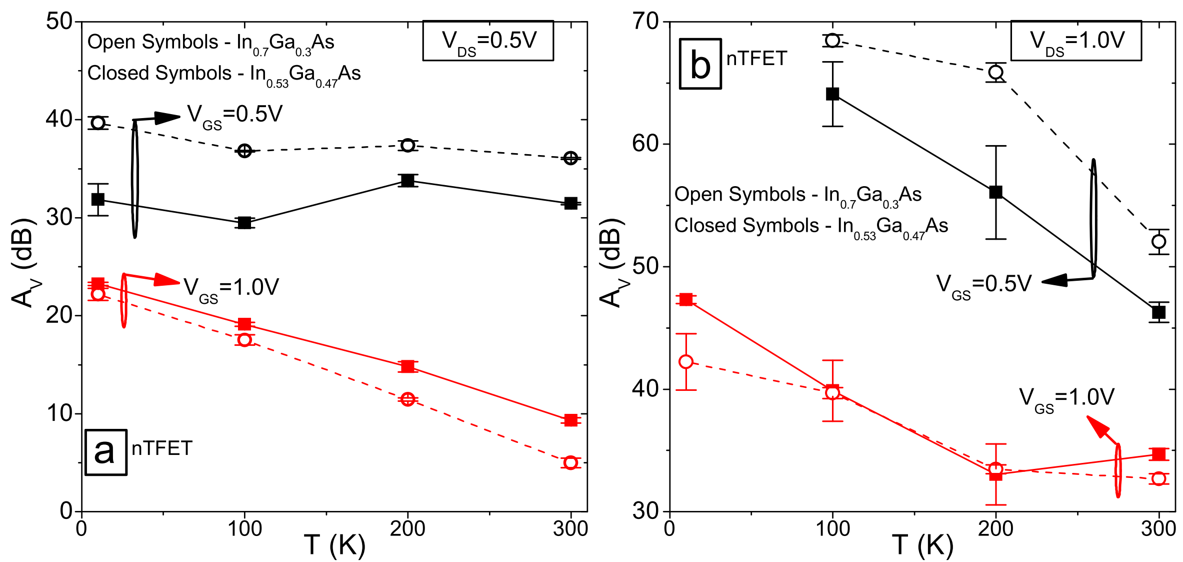

Figure 11. Experimental A_V as a function of the temperature for the $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ devices, with V_{DS} = 0.5 V (a) and V_{DS} = 1.0 V (b).

V_{DS}, as the g_D is very low, a very high A_V can be observed, however, the temperature influence is even higher.

Conclusion

This work presents an experimental study, complemented by numerical simulations, of the analog parameters behavior of spin-on-glass Zn-diffused $In_xGa_{1-x}As$ nTFETs down to 10 K. For In-70% the bandgap is lower, resulting in an increase of drain current and transconductance due to the BTBT dominance. However, it also presents a higher g_D than for the $In_{0.53}Ga_{0.47}As$ channel. This behavior generates a competition between the influence of gm and g_D, resulting in higher A_V for $In_{0.7}Ga_{0.3}As$ for low V_{GS} bias and in a similar A_V for both devices at high V_{GS} values.

In this device technology, at temperatures lower than 100 K the reduction of SRH and TAT is so pronounced that the gate current dominates I_{OFF}, resulting in marginal temperature dependence below 100 K of I_{OFF}. The reduction of the temperature causes a degradation of gm, however, it presents a higher BTBT component, which is less temperature dependent. The temperature influence on g_D was observed experimentally and also in the simulations and it is related to the reduction of the drain dependence of the BTBT generation rate. The temperature influence is more pronounced in g_D than in gm, resulting in an increase of A_V at low temperatures. For lower drain and gate bias (0.5 V) the A_V presents less temperature sensitivity for both devices analyzed, which could be a good option for some applications.

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References

[1] Reddick W M and Amaratunga G 1995 Silicon surface tunnel transistor *Appl. Phys. Lett.* **64** 494–6

[2] Kim M, Wakabayashi Y, Nakane R, Yokoyama M, Takenaka M and Takagi S 2014 High Ion/Ioff Ge-source ultrathin body strained-SOI Tunnel FETs *IEEE IEDM Technical Digest* pp 331–4

[3] Krishnamohan T, Kim D, Raghunathan S and Saraswat K 2008 Double-gate strained-Ge heterostructure Tunneling FET (TFET) with record high dive currents and <60 mV/dec subthreshold slope *IEEE IEDM Technical Digest* pp 1–3

[4] Choi W Y, Park B G, Lee J D and Liu T J K 2007 Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less Than 60 mV/dec *IEEE Electron Device Lett.* **28** 743–5

[5] Lu H and Seabaugh A 2014 Tunnel field-effect transistors: state-of-the-art *IEEE J. Electron Device Soc.* **2** 44–9

[6] Verhulst A S, Vandenberghe W G, Maex K and Groeseneken G 2008 Boosting the on-current of a n-channel nanowire tunnel field-effect transistor by source material optimization *J. Appl. Phys.* **104** 064514

[7] Leonelli D, Vandooren A, Rooyackers R, De Gendt S, Heyns M M and Groeseneken G 2011 Drive current enhancement in p-tunnel FETs by optimization of the process conditions *Solid-State Electron.* **65–66** 28–32

[8] Vandooren A, Leonelli D, Rooyackers R, Hikavyy A, Devriendt K, Demand M, Loo R, Groeseneken G and Huyghebaert C 2013 Analysis of trap-assisted tunneling in vertical Si homo-junction and SiGe hetero-junction Tunnel-FETs *Solid-State Electron.* **83** 50–5

[9] Schmidt M, Schäfer A, Minamisawa R, Buca D, Trellenkamp S, Hartmann J M, Zhao Q T and Mantl S 2014 Line and point tunneling in scaled Si/SiGe heterostructure TFETs *IEEE Electron Device Lett.* **35** 699–701

[10] Verreck D, Verhulst A, Van de Put M, Sorée B, Collaert N, Mocuta A, Thean A and Groeseneken G 2016 Uniform strain in heterostructure tunnel field-effect transistors *IEEE Electron Device Lett.* **37** 337–40

[11] Takagi S, Kim M, Noguchi M, Nishi K and Takenaka M 2015 Tunneling FET device technologies using III–V and Ge materials *Symp. on Energy Efficient Electronic Systems (E3S)* pp 1–2

[12] Agopian P G D, Martino M D V, dos Santos S D, Neves F S, Martino J A, Vandooren A, Rooyackers R, Simoen E, Thean A and Claeys C 2015 Analog performance on vertical nanowire-TFET with different source compositions *IEEE Trans. Electron Devices* **62** 16–22

[13] Martino M D V, Neves F S, Agopian P G D, Martino J A, Vandooren A, Rooyackers R, Simoen E, Thean A and Claeys C 2015 Analog performance of vertical nanowire TFETs as a function of temperature and transport mechanism *Solid-State Electron.* **112** 51–5

[14] Mallik A and Chattopadhyay A 2012 Tunnel Field-Effect Transistors for analog/mixed-signal system-on-chip applications *IEEE Trans. Electron Devices* **59** 888–94

[15] Agopian P G D, dos Santos S D, Neves F S, Martino J A, Vandooren A, Rooyackers R, Simoen E and Claeys C 2013 NW-TFET analog performance for different Ge source compositions *Proc. IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conf. (S3S)*

[16] Agopian P G D, Martino J A, Rooyackers R, Vandooren A, Simoen E and Claeys C 2013 Experimental comparison between trigate p-TFET and p-FinFET analog performance as a function of temperature *IEEE Trans. Electron Devices* **60** 2493–7

[17] Agopian P G D, Martino J A, Rooyackers R, Vandooren A, Simoen E and Claeys C 2015 Intrinsic voltage gain of Line-TFETs and comparison with other TFET and MOSFET architectures *Proc. EuroSOI-ULIS* pp 13–5

[18] Bordallo C, Sivieri V, Martino J A, Agopian P G D, Rooyackers R, Vandooren A, Simoen E, Thean A and Claeys C 2016 Impact of the NW-TFET diameter on the efficiency and the intrinsic voltage gain from a conduction regime perspective *IEEE Trans. Electron Devices* **63** 2930–5

[19] Zhao Q-T *et al* 2015 Strained Si and SiGe nanowire tunnel FETs for logic and analog applications *IEEE J. Electron Device Soc.* **3** 103–14

[20] Sedighi B, Hu X, Liu H, Nahas J and Niemier M 2015 Analog circuit design using tunnel-FETs *IEEE Trans. Circuits Syst. I* **62** 39–48

[21] Agopian P G D, Martino J A, Vandooren A, Rooyackers R, Simoen E, Thean A and Claeys C 2015 Comparison between vertical silicon NW-TFET and NW-MOSFET from analog point of view *Proc. EuroSOI-ULIS*

[22] Liu L, Mohata D and Datta S 2012 Scaling length theory of double-gate interband tunnel field-effect transistors *IEEE Trans. Electron Devices* **59** 902–8

[23] Moselund K, Björk M, Schmid H, Ghoneim H, Karg S, Lörtscher E, Riess W and Riel H 2011 Silicon nanowire tunnel FETs: low-temperature operation and influence of high-*k* gate dielectric *IEEE Trans. Electron Devices* **58** 2911–6

[24] Noguchi M, Kim S H, Yokoyama M, Ichikawa O, Osada T, Hata M, Takenaka M and Takagi S 2015 High Ion/Ioff and low subthreshold slope planar-type InGaAs tunnel field effect transistors with Zn-diffused source junctions *J. Appl. Phys.* **118** 045712

[25] Alian A *et al* 2015 Record performance InGaAs homo-junction TFET with superior SS reliability over MOSFET *IEEE IEDM Technical Digest.* pp 823–6

[26] Yamamoto Y and Kanbe H 1980 Zn diffusion in $In_xGa_{1-x}As$ with $ZnAs_2$ source *Japan. J. Appl. Phys.* **19** 121–8

[27] Hall R N 1952 Electron-hole recombination in Germanium *Phys. Rev.* **87** 387

[28] Chynoweth A G, Feldmann W L and Logan R A 1961 Excess tunnel current in silicon Esaki junctions *Phys. Rev.* **121** 684–94

[29] Hurkx G A M, Klaassen D B M and Knuvers M P G 1992 A new recombination model for device simulation including tunneling *IEEE Trans. Electron Devices* **39** 331–8

[30] Agopian P G D, Martino J A, Simoen E and Claeys C 2007 Study of linear kink effect in PD SOI nMOSFETs *Microeletron. J.* **38** 114–9

[31] Chao K and Chen M 1995 Fowler-nordheim limited band-to-band tunelling (FNBB) for p-MOSFET gate current in a floating bulk condition *Solid State Electron.* **38** 135–7

[32] Lenzlinger M and Snow E 1969 Fowler-Nordheim Tunneling into thermally grown SiO2 *J. Appl. Phys.* **40** 278–83

[33] Verhulst A, Leonelli D, Rooyackers R and Groeseneken G 2011 Drain voltage dependent analytical model of tunnel field-effect transistors *J. Appl. Phys.* **110** 024510

[34] Synopsys, Sentaurus Device L-2016.03

[35] Smets Q *et al* 2014 InGaAs tunnel diodes for calibration of semi-classical and quantum mechanical band-to-band tunneling models *J. Appl. Phys.* **115** 184503