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# Study of line-TFET analog performance comparing with other TFET and MOSFET architectures

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ABSTRACT

In this work the Line-TFET performance is compared with MOSFET and Point-TFET devices, with different architectures (FinFET and GAA:Gate-All-Around) at both room and high temperatures. This analysis is based on the experimental basic analog parameters such as transconductance (gm), output conductance ($g_D$) and intrinsic voltage gain ($A_V$). Although the Line-TFETs present worse $A_V$ than the point-TFETs, when they are compared with MOSFET technology, the line-TFET shows a much better intrinsic voltage gain than both MOSFET architectures (FinFET and GAA). Besides the $A_V$, the highest on-state current was obtained for Line-TFETs when compared with other two TFET architectures, which leads to a good compromise for analog application.

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## 1. Introduction

Tunnel-FETs have been proposed by the international community as an alternative for MOSFETs, when focusing on extremely small technology nodes, due to their high speed switching capability [1] that allows to improve the energy efficiency of switches. However, as the low on-current is a problem of homo-junction TFETs, several works report research on different materials and different geometries aiming to reach a smaller subthreshold swing and an on-current improvement [2,3].

A planar Line-TFET is an alternative structure that increases the electric field at the source-pocket junction and consequently improves the on-current and reduces the subthreshold swing when compared with the point-TFET silicon devices [4–6].

Although the main focus of the tunnel-FET is the digital switch, some recent work has also pointed out the great potential of these devices for analog applications [7–10].

In this work the planar heterojunction Line-nTFET is experimentally analyzed through the basic analog parameters, focusing mainly on intrinsic voltage gain. A comparison of the intrinsic voltage gain of Line-TFETs with devices with different architectures like FinFET (MOSFET and TFETs) [7] and Gate-all-around (MOSFET and TFET) [11] is also performed, for temperatures ranging from room up to 150 °C. For vertical GAA-TFETs, different source compositions (Si and $Si_{0.73}Ge_{0.27}$) will be also considered.

## 2. Device characteristics

The studied Line-nTFETs are Si/SiGe heterojunction devices fabricated on silicon-on-insulator wafers at imec/Belgium. The p-type $Si_{0.55}Ge_{0.45}$ source extends under the gate and a thin intrinsic silicon pocket layer (~5 nm) is on top. The source and the drain regions are separated by a nominally undoped Si channel.

The gate stack is composed by a 1 nm interfacial $SiO_2$ layer followed by 1.8 nm of $HfO_2$, 2 nm of TiN and p-doped amorphous silicon. The channel width (W) ranges from 110 nm to 200 nm and two different gate lengths (L) (1 μm and 130 nm) were evaluated. Fig. 1 presents a schematic structure of a Line-TFET and more details on this structure/fabrication can be found in [6].

## 3. Analysis and discussion

Since the source of Line-TFETs extends under the gate region, this architecture promotes tunneling in the same electric field direction, which is more efficient than the conventional point-tunneling. Besides, the position of the tunneling source/channel

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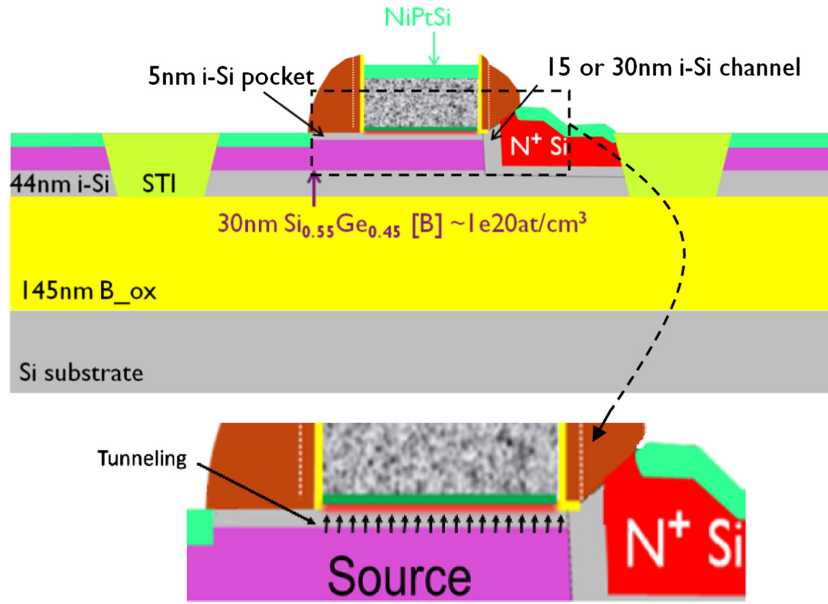


**Fig. 1.** Line-TFET structure.

junction makes the total tunneling proportional to the $L \times W$ dimensions.

Fig. 2 presents the transfer characteristic normalized by the channel width of a single Line-TFET for different drain bias (A) and for point-TFETs with different source composition (B) as a function of gate voltage. From Fig. 2, it is possible to observe that Line-TFETs (2A) reaches a higher on-state current than point-TFETs (2B), considering the same channel width. This ON-current improvement, promoted by the Line-TFET structure, is a result of the alignment of the electric field with the tunneling direction that in turns, results in a strong energy band bending, increasing the band-to-band current. It is also possible to observe from the Line-TFET transfer characteristics (Fig. 2A) that the smaller the drain bias ($V_{DS}$), the steeper the drain current ($I_{DS}$) in the sub-threshold region due to the off current reduction. The SS improvement becomes even more pronounced with increasing gate length and consequently the tunneling area as reported in [6].

Besides the high on state current, when the output characteristic is evaluated (Fig. 3), the line-TFET also presents a good plateau in the saturation like region, showing to be a promising device for

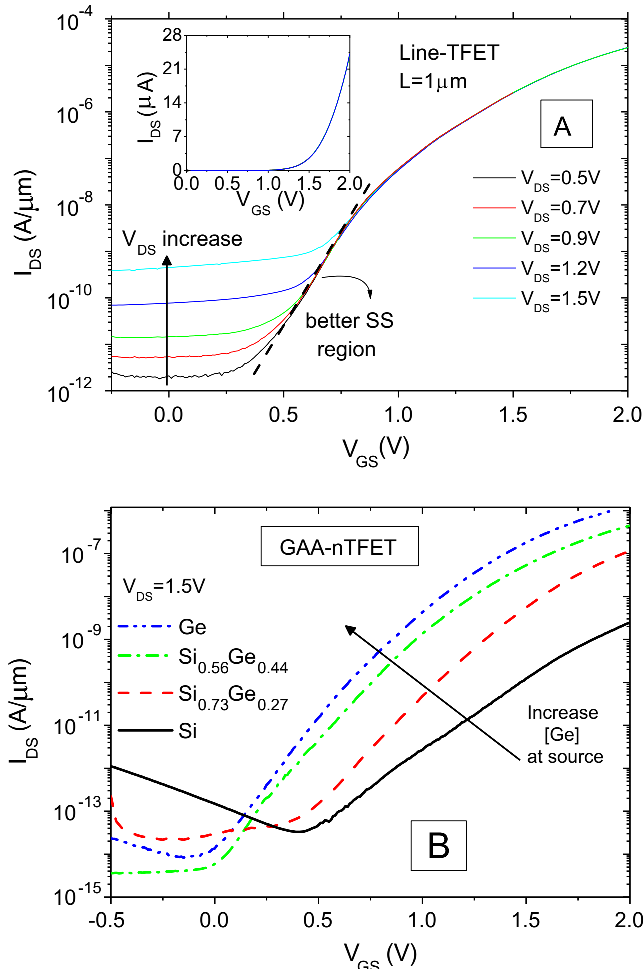


**Fig. 2.** Experimental normalized transfer curves of a Line-TFET for different drain bias (A) and of a point-TFET for different source compositions [12] (B).

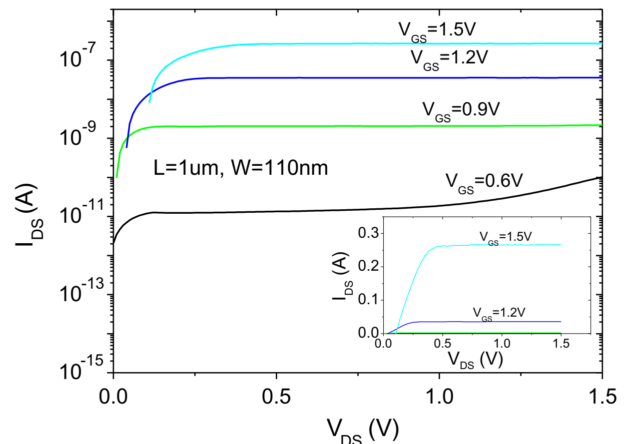


**Fig. 3.** Experimental output characteristic of a Line-TFET for different gate bias.

analog applications, as was already reported for point-TFETs [7,8]. However, at low gate bias, it is clear that the saturation like region does not present a plateau, i.e., the output characteristic is degraded and becomes inappropriate for this kind of application. Since the drain current level changes several orders of magnitude with the gate bias increase, the drain current was also plotted in a linear scale (inset), in order to better observe the plateau region, confirming the aforementioned.

Considering that the intrinsic voltage gain ($A_V$) is one of the most important figures of merit for analog applications and it can be calculated by the transconductance (gm) over output conductance ($g_D$) ratio, these parameters were evaluated for different bias, channel lengths and channel widths, aiming to optimize the Line-TFET $A_V$ performance.

The gm and $g_D$ analysis were performed for different channel lengths and different channel widths in order to select the best combination of the transistor dimensions to optimize the $A_V$ value as can be seen in Fig. 4.

From Fig. 4A, it is possible to notice that although gm increases with the gate bias due to the higher overlap between bands, similarly as occurs for point-TFETs, when the comparison between line and point TFETs focus on the gm dependence with channel length, the line-TFETs presents a direct dependence on L, while point devices usually are independent on it. The higher gm for longer channel length occurs due to the larger tunneling junction area underneath the gate as shown in Fig. 4 (source/Si pocket).

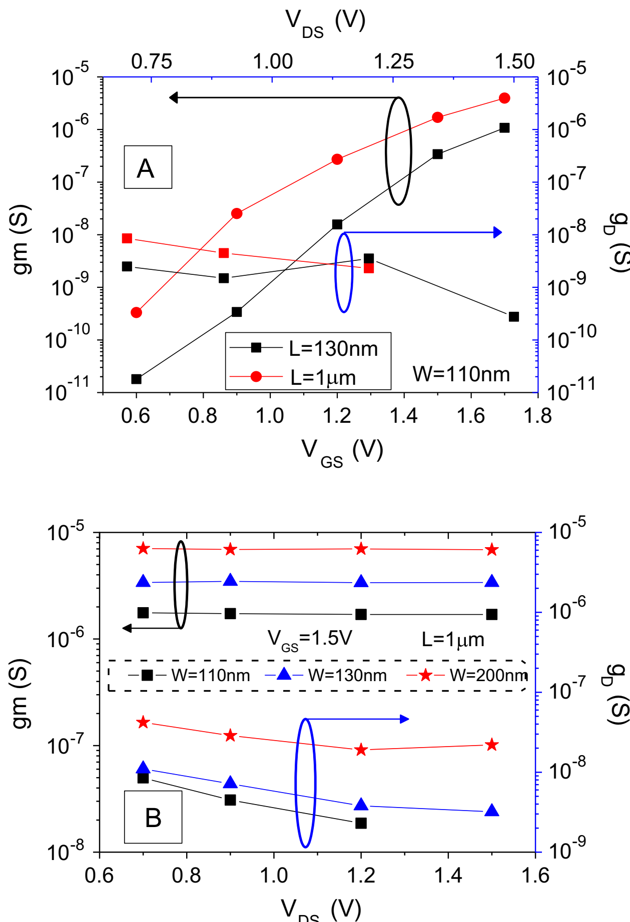


**Fig. 4.** Transconductance (Left/Bottom axis) and output conductance (Right/Top axis) for different channel lengths (A) and for different channel widths as a function of $V_{DS}$ (B).

However, evaluating the $g_D$ values, a smaller gate length dependence is observed. Besides this, as $V_{DS}$ increases, the TFET devices operate more in the "saturation like" region, resulting in a better (smaller) $g_D$.

The dependence of these two parameters ($g_D$ and gm) on channel width (W) were also evaluated for high $V_{GS}$ (1.5 V) as a function of drain bias (Fig. 4B). Although the drain bias does almost not affect the transconductance, it increases with the channel width, as expected, due to the junction area increase. Focusing on output conductance ($g_D$), it was observed that it depends on both the drain bias and the channel width, but in the opposite way. While the higher drain bias contributes to the $g_D$ improvement (the TFET operates more in the "saturation like" region), the drain current increases with channel width resulting in a $g_D$ degradation (increase).

Keeping in mind that the transconductance presented a significant improvement for longer channel device, while the variation on output conductance is not so important, the obtained intrinsic voltage gain ($A_V$) for longer devices was higher than the shorter one. Fig. 5 shows the experimental $A_V$ for long line-TFETs (L = 1 µm) with different channel widths operating at different drain bias. From Fig. 5 it is possible to observe that the output characteristic improvement associated with a $V_{DS}$ increase leads to an optimization of the bias operation point for the analog performance of all Line-TFETs. However, when the channel width (W) was evaluated, the response of a transistor with W of 130 nm, shows a reduction of two times on transconductance and a strong reduction on $g_D$ compared with their counterpart with W = 200 nm, that in turns, results in a best $A_V$ value for devices with W = 130 nm and L = 1 µm.

Since the line-TFET with W = 130 nm and L = 1 µm shows to be slightly better and the best bias condition was defined above for the line-TFET architecture and it was already performed for TFET-FinFET and GAA-FinFET architectures in [7,8], respectively, from now on, their analog performance is compared among these three different architectures. Besides this analysis, a comparison of this planar Line-TFET was also performed for different technologies (MOS and TFET).

The first comparison, shown in Fig. 6, is focused on gm and $g_D$ of these three different architectures. Comparing the TFETs fabricated in a planar (line) and FinFET structure (Fig. 6A) it is possible to see that both transconductance and output conductance obtained for planar devices are very high because the line TFETs becomes to be dominated by the earlier start of the Band-to-band tunneling phenomena. However, considering the vertical GAA structure

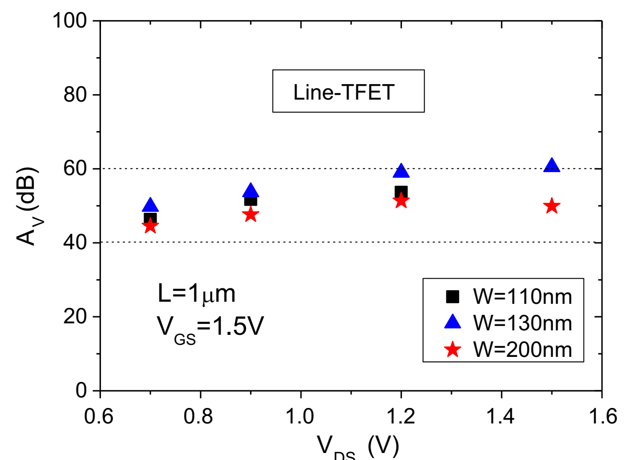


**Fig. 5.** Experimental $A_V$ for Line-TFETs for different $V_{DS}$ and channel widths at $V_{GS}$ = 1.5 V.

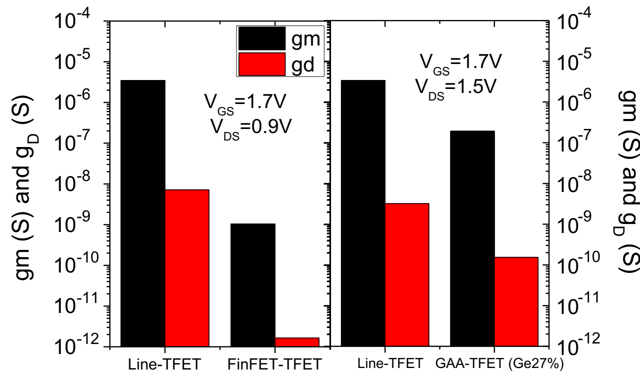


**Fig. 6.** Experimental comparison of gm and $g_D$ at optimum point for different architectures: Line-TFET × FinFET (A) and Line-TFET × GAA-TFET (B).

(Fig. 6B), only the transconductance stands out due to its improvement.

Making the analog evaluation for different temperatures (from room to 150 °C), the $A_V$ performance among the planar Line-TFET and transistors fabricated with the FinFET structure (tunnel-FET and MOSFET), shows a smaller $A_V$ for Line-TFETs than for the TFET with the FinFET structure (Fig. 7). It occurs because line-TFETs are more dependent of BTBT and as a consequence a higher $g_D$ was obtained.

However, when line-TFETs are compared with the conventional FinFETs (MOSFET technology), the $A_V$ of Line-TFETs is at least 30 dB higher for all temperatures because the BTBT tunneling current is less dependent of $V_{DS}$ than the drift current.

Considering the gate-all around transistors, like nanowire devices, it is well known that for smaller diameter, the coupling between gate and channel is higher, resulting in a predominance of BTBT rate along all the source/channel junction area [13]. As a consequence it can be obtained a better subthreshold swing behavior, higher gm and consequently higher transistor efficiency (gm/$I_{DS}$) at weak conduction regime as reported by [14], which increases the intrinsic voltage gain increases only in this operation region. However, transistors with higher diameter is more TAT dependent (less BTBT dependence), which degrades the weak inversion, but it is less drain voltage dependent, resulting in a better output conductance, Early voltage and consequently the intrinsic voltage gain at strong conduction as already reported in [7,8].

Focusing on the performance of intrinsic voltage gain in the strong conduction regime, the same analog comparison was performed, but now considering Line-TFETs and vertical GAA structures (Si-MOSFETs and TFETs with Si and $Si_{0.73}Ge_{0.27}$ sources) as can be seen in Fig. 8. Since the line-TFETs reaches a higher BTBT current while GAA structures are more TAT dependent, the GAA-TFETs present higher $A_V$ values than the Line TFETs, independent on the source composition.

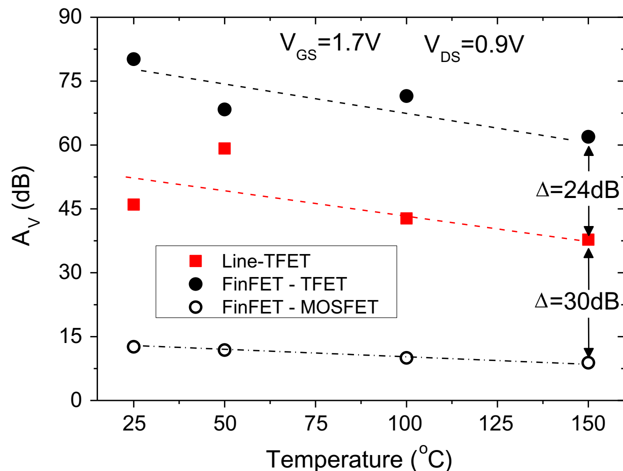


**Fig. 7.** Experimental comparison of $A_V$ as a function of temperature among Line-TFET, FinFET-TFET and FinFET MOSFET, for FinFET-TFET optimal bias point ($V_{GS}$ = 1.7 V and $V_{DS}$ = 0.9 V).

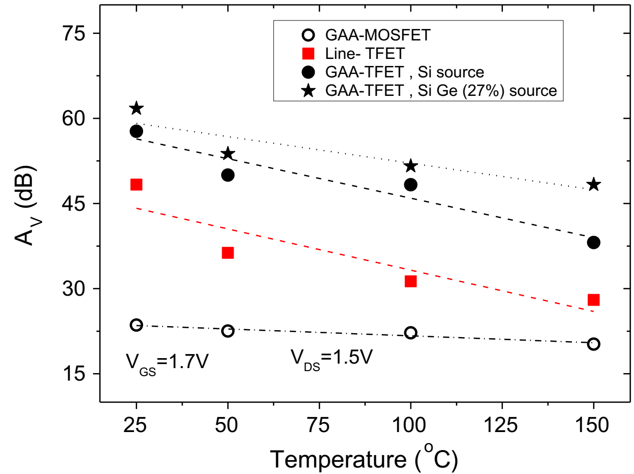


**Fig. 8.** Experimental comparison of $A_V$ as a function of temperature among Line-TFET, GAA-TFET (with different source compositions) and GAA-MOSFET, for GAA-TFET optimal bias point ($V_{GS}$ = 1.7 V and $V_{DS}$ = 1.5 V).

However when the Line-TFET is compared with a GAA MOSFET, the Line TFET seems to be better again.

Although Line-TFETs do not reach $A_V$ values as high as for GAA-TFETs and Fin-TFETs, when a high on-state current is required, the planar Line-TFET can be considered as an alternative, since it reaches on-state currents much higher than the other TFET structures studied in this paper.

## 4. Conclusion

This paper presents an analysis of the intrinsic voltage gain of Line-TFETs and makes a comparison with devices fabricated with vertical GAA and FinFET structures for both TFET and MOSFET technologies. The results show that this planar line-TFET architecture does not present the highest $A_V$ values when compared with the two other vertical TFET architectures (FinFET-TFET and GAA-TFET), however it reaches a very high on-state current, which till now was a road block for another TFET structures. Therefore it is possible to conclude that Line-TFETs can be a good alternative to replace MOSFETs since it reaches the highest on-state currents and a better intrinsic voltage gain than the advanced MOSFET architectures (at least 30 dB higher than FinFETs and 10 dB higher when compared with GAA-MOSFETs).

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