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Low-frequency noise investigation of n-channel 3D devices

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ABSTRACT

In this paper, the low-frequency (LF) noise in standard n-channel triple-gate Bulk FinFETs has been experimentally investigated with variation in the fin widths (W_{Fin}), channel lengths (L) and gate dielectric. The origin of the noise will be analyzed in order to understand the physical mechanisms involved in 3D device architectures. Although the device scaling brings the idea of noise reduction, we show the opposite behavior because already single electron trapping has a marked impact on the device operation. Significant variation in the noise spectral density has been observed, which is related to the random occurrence of excess Lorentzian components ($1/f^2$-like), associated with generation–recombination (GR) noise. In addition, the gate-voltage-dependent GR noise peaks have been studied, which are assigned to gate oxide traps.

1. Introduction

Bulk FinFETs are finding their commercial breakthrough for 22 nm technologies and below due to the superior control over the short-channel effects offered by the multiple-gate architecture [1]. Much attention is nowadays given to the fabrication of tri-gate FinFETs on bulk substrates but, till today there is still discussion on some technical issues associated with the substrate choice (bulk or SOI) to face the challenges beyond the 10 nm generation [2]. However, all kinds of multigate transistors and nanowire devices are also investigated for advanced technology node applications such as analog circuits, dynamic threshold operation [3], one-transistor (1T) capacitorless memory devices [4,5] working like gateless [6] or like biristor [7] devices and cylindrical vertical FETs for non-volatile memories [8].

In the last decade it became clear that low-frequency (LF) noise is not only an important figure of merit for both analog and mixed-signal applications, but that LF noise analysis is a very powerful and sensitive tool to reveal and quantify the presence of defects both in the dielectric layer, in the channel region and at their interfaces [9–13] which is directly impacting the quality of electronic devices.

Generally, large variations in noise levels from device to device are observed. The LF noise origin has been related to either number [14] or mobility fluctuations [15], while the surface roughness of the fin can have a pronounced impact on the noise. Previous noise studies on bulk triple-gate FinFETs have revealed a combination of $1/f$-like noise and GR noise to be present in linear operation [3,16], and showing that the flicker noise usually is dominated by the number fluctuations or gate-oxide trapping mechanism. GR noise centers both in the silicon fin and in the gate oxide contribute Lorentzians to the noise spectrum [14].

Low-frequency noise characterization is also applied to advanced memory devices in order to obtain more information on the defects affecting their performance. The study of generation–recombination (GR) centers in Bulk FinFETs is very important for analyzing the data retention [15]. Operating the devices in the dynamic threshold mode, which is beneficial for analog applications, has no consequences for the noise behavior [16].

2. Experimental

The process splits have been fabricated on 300 mm Czochralski Si wafers, employing a Fin height H_{Fin} of about 65 nm and 5 parallel fins. The investigated standard n-channel Bulk FinFETs with extensions have an undoped channel and the gate dielectric consists for some devices of 5 nm SiO_2, while all the others have been processed with 2.5 nm SiON capped with 5 nm Plasma-Enhanced Atomic Layer Deposited (PE-ALD) TiN and 100 nm poly-silicon. The gate oxide thickness is not scaled too aggressively to reduce the gate leakage current and its potential impact on retention in

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1T memory applications. Well implants and a ground plane doping have been implemented in order to reduce the leakage currents between fins and the silicon substrate. The standard process flow up to metal-1 has been optimized for logic applications. More processing details can be found in [17].

We analyzed devices with a channel length (L) of 70 nm and different fin widths W_{Fin} (10, 20, 40 and 65 nm) and also devices with W_{Fin} = 20 nm and L of 45, 70, 90 and 1000 nm. The noise measurements were performed at 25 °C on wafer in linear operation at a drain bias V_D of 50 mV with the substrate contact grounded and the gate voltage (V_G) stepped from weak to stronger inversion. The noise system relies on BTA hardware under control of ProPlusSolution software.

3. Results and discussion

The drain current and transconductance versus gate voltage are shown in Fig. 1 for Bulk FinFET transistors with different fin width (W_{Fin}) and gate length (L). As expected, one can clearly see that the maximum transconductance and drain current increase with fin width and the opposite behavior with the increasing length of the channel because the current is directly proportional to W (where $W \cong W_{Fin} + 2\,H_{Fin}$) and is inversely proportional to L [3].

A typical behavior of the drain current noise spectral density (Sid) versus drain current (I_D) in FinFETs devices is represented in Fig. 2 for a measurement frequency (f) of 25 Hz, whereby Sid follows for low drain currents a quadratic law with the drain current. There are also clear GR humps in the Sid vs. I_D curves, indicating the presence of GR centers in the gate dielectric, as reported elsewhere in more detail [14].

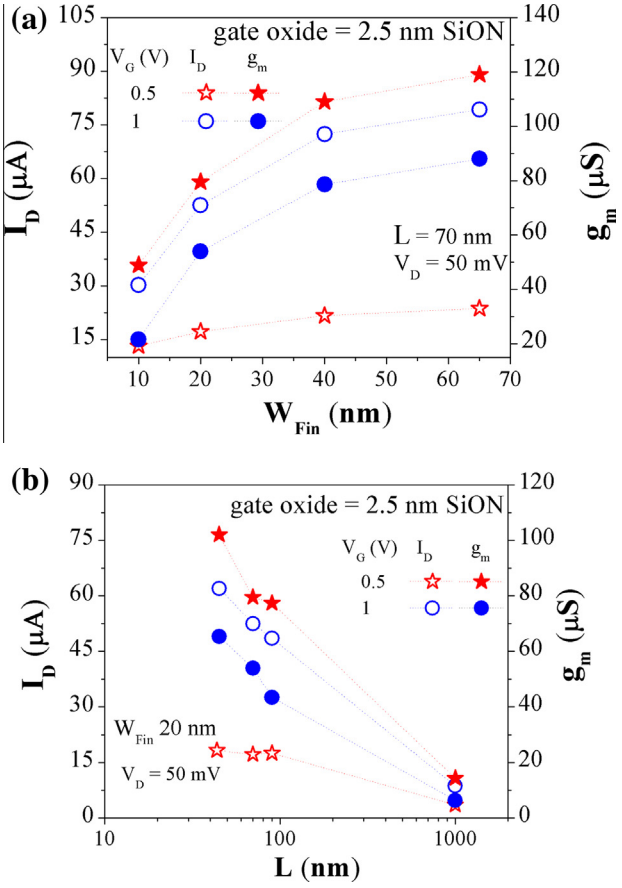

Fig. 1. Drain current (I_D) and Transconductance (g_m) for 3D devices (Bulk FinFETs) with different fin width W_{Fin} (a) and channel length L (b).

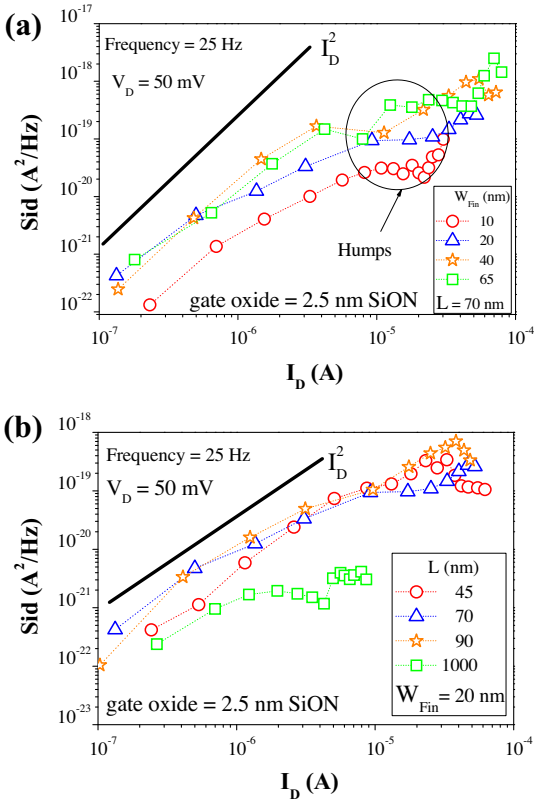

Fig. 2. Noise spectral density (Sid) versus drain current (I_D) at f = 25 Hz for Bulk FinFETs with different fin width W_{Fin} (a) and channel lengths (b).

The superposition of $1/f$ noise and at higher frequencies a Lorentzian due to GR noise is shown in Fig. 3. GR noise is characterized by a plateau and at higher frequencies a roll off with $1/f^2$ [11].

The normalized $1/f$ noise spectral density (Sid/I_D^2) at 25 Hz is shown in Fig. 4 together with $(g_m/I_D)^2$ curves. A similar behavior of the two curves is an indication for number fluctuations. This corresponds with a plateau in weak inversion and a roll-off at higher I_D [18].

The input-referred noise spectral density (Sid/g_m^2) is represented in Fig. 5. The constant value at low V_G confirms the trapping origin of the $1/f$ noise. In this case, there is a plateau level around the threshold voltage (V_T), from which an oxide trap density can be derived [14].

By analyzing the curves of Sid as a function of W_{Fin} for several devices, an increase of LF noise with the increase of W_{Fin} is observed. Device miniaturization, leading to a reduction of the number of carriers available for transport, gives rise to a greater sensitivity to inevitable device variations. It can be confirmed by analyzing Eq. (1) [19–21], where q is the elementary charge, α_H is the Hooge parameter (10^{-3} a 10^{-6}), f is the frequency and C_{ox} is the gate oxide capacitance.

$$\frac{Sid}{I_D^2} = \frac{q.\alpha_H}{f.W.L.C_{ox}(V_G - V_T)} \tag{1}$$

On the one hand, it is possible to observe an increase of LF noise magnitude with the increase of L in the curves of Sid as a function of L when comparing devices with L = 1000 nm with the other lengths. Some difference in strong inversion can be observed (L of 45, 70 and 90 nm) which can be attributed to the correlated mobility fluctuations [21,22].

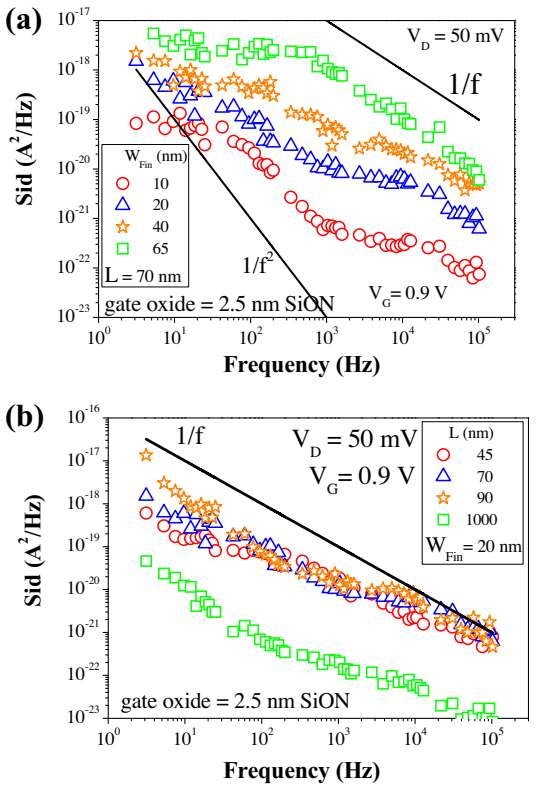

Fig. 3. Noise spectral density (Sid) versus frequency at $V_G = 0.9$ V for Bulk FinFETs with different fin width W_{Fin} (a) and channel lengths (b).

The corresponding current power spectral density (Sid) for devices with different gate oxide thickness and materials is presented in Fig. 6. One can observe that the GR noise is more pronounced at higher gate voltage V_G, indicating that the responsible trap centers are residing in the gate dielectric and not in the silicon depletion region [11].

The noise behavior reported in Ref. [16] clearly shows that LF noise is more pronounced in the saturation region (at higher drain voltage V_D). All devices show practically the same low-frequency noise magnitude indicating that they have a similar behavior with respect to the gate dielectric quality. In this case the noise is weakly affected only by the thickness of the two materials: conventional SiO_2 and SiON [13,23].

The devices processed with 5 nm SiO_2 as a gate dielectric are used for memory application. These devices have lower gate leakage current and are more resistive at higher gate voltage. One of the important metrics for memory operation is the retention time of the stored hole charge in case of n-channel transistors. The narrow devices have fully depleted fins and no holes can be stored in the 1-state there, so that the charges are stored in the ground plane near the drain region [24] by recombining with generated electrons or by tunneling through the gate oxide. The 0-state can be compromised by hole generation by thermally or field-assisted mechanisms.

The fact that the charges are stored outside the fin, away from the Si/SiO_2 interfaces indicates that gate oxide traps will not contribute significantly to the charge retention, while, on the contrary, bulk defects can have a strong impact. This implies that no correlation is expected with the $1/f$ noise magnitude, while GR Lorentzians due to fin defects are a fingerprint of excess charge generation.

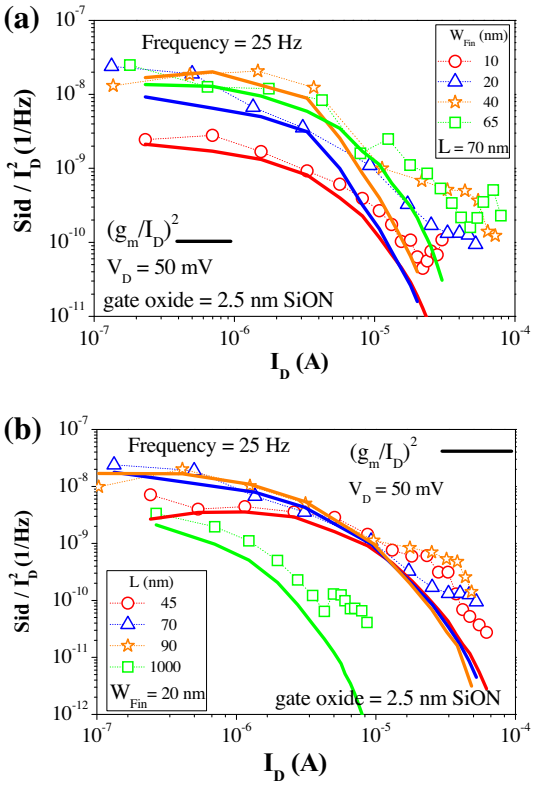

Fig. 4. Normalized noise spectral density (Sid/I_D^2) versus drain current (I_D) at $f = 25$ Hz for Bulk FinFETs with different fin width W_{Fin} (a) and channel lengths (b).

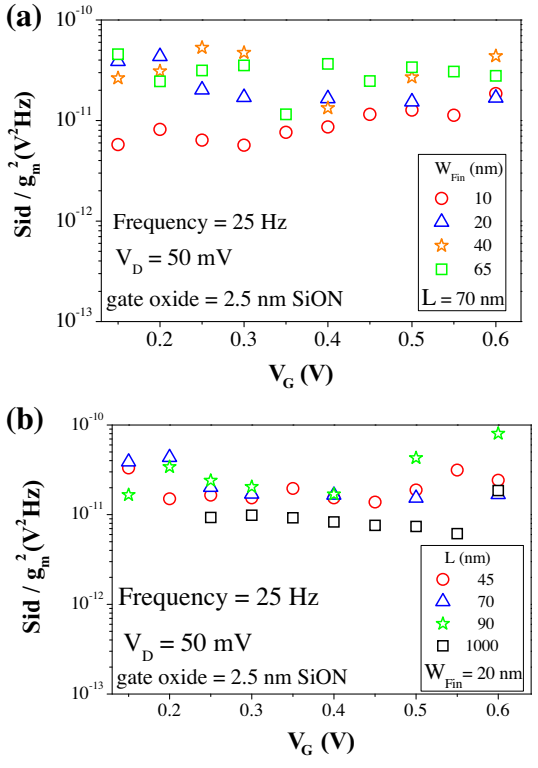

Fig. 5. Input-referred voltage noise spectral density (Sid/g_m^2) versus gate voltage (V_G) at $f = 25$ Hz for Bulk FinFETs with different fin width W_{Fin} (a) and channel lengths (b).

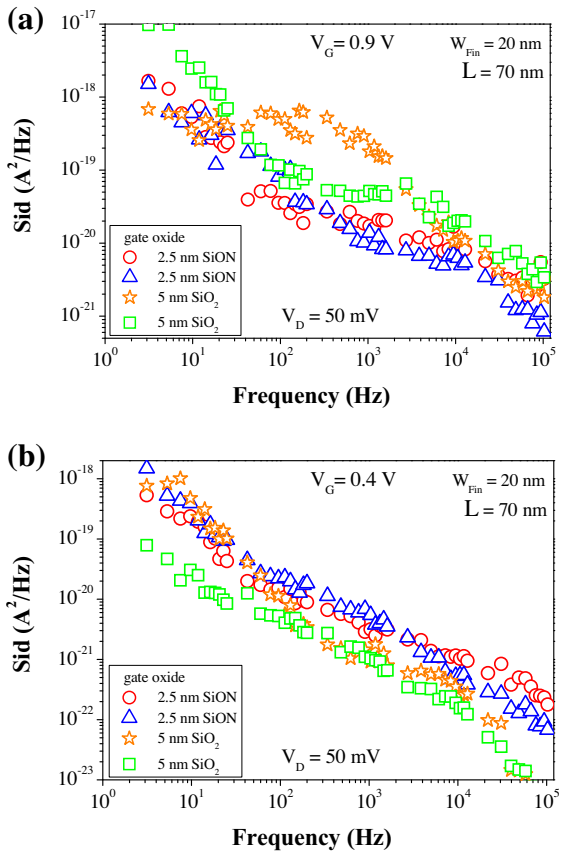

Fig. 6. Noise spectral density (Sid) versus frequency at V_G = 0.9 V (a) and V_G = 0.4 V (b) for Bulk FinFETs with different gate oxide material.

4. Conclusions

This work presented an experimental study of the low frequency noise in 3D devices with different fin widths W_{Fin}, channel lengths and gate dielectrics. The measurements have identified both 1/*f* and GR noise contributions. The 1/*f*-noise is caused by trapping and detrapping of carriers by defects in the gate oxide. In fact, the presence of GR centers in the gate oxide, derived from the excess Lorentzian noise is in further support of this interpretation.

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