VLSI Design, 2002 VOL. 15 (1), pp. 469–476

Taylor & Francis
Taylor & Francis Group

A CMOS/SOI Single-input PWM Discriminator for Low-voltage Body-implanted Applications*

JADER A. DE LIMA[a,†], SIDNEI F. SILVA[a], ADRIANO S. CORDEIRO[a] and MICHEL VERLEYSEN[b,‡]

[a]*Electrical Engineering Department, Universidade Estadual Paulista, Av. Ariberto Pereira de Cunha, 333, 12516-410 Guaratinguetá-SP, Brazil;*
[b]*Microelectronics Laboratory, Université Catholique de Louvain, B-1348 Louvain-la-Neuve, Belgium*

(Received 15 January 2001; Revised 20 April 2001)

A CMOS/SOI circuit to decode Pulse-Width Modulation (PWM) signals is presented as part of a body-implanted neurostimulator for visual prosthesis. Since encoded data is the sole input to the circuit, the decoding technique is based on a novel double-integration concept and does not require low-pass filtering. Non-overlapping control phases are internally derived from the incoming pulses and a fast-settling comparator ensures good discrimination accuracy in the megahertz range. The circuit was integrated on a 2 μm single-metal thin-film CMOS/SOI fabrication process and has an effective area of 2 mm^2. Measured resolution of encoding parameter α is better than 10% at 6 MHz and $V_{DD} = 3.3$ V. Idle-mode consumption is 340 μW. Pulses of frequencies up to 15 MHz and $\alpha = 10\%$ can be discriminated for 2.3 V $\leq V_{DD} \leq$ 3.3 V. Such an excellent immunity to V_{DD} deviations meets a design specification with respect to inherent coupling losses on transmitting data and power by means of a transcutaneous link.

Keywords: PWM decoder; SOI design; Low-voltage comparators; Implanted circuits; Visual prosthesis

INTRODUCTION

With the perspective of providing quasi-ideal three-terminal transistors, the CMOS Silicon-on-Insulator (SOI) technology has increasingly become more attractive as compared to its bulk counterpart on designing integrated circuits with superior performance on temperature and radiation hardness, power consumption, latch-up hazards and others [1,2]. The compactness of SOI circuits is increased due to the absence of separated wells for N- and P-channel devices. In addition, transistor dimensions are shrunk and stray capacitances considerably reduced by the presence of buried oxide, further pushing the frequency limit of Silicon technology. Very-low leakage currents make CMOS/SOI suitable for low-voltage, low-power (LVLP) applications such as battery-powered and human-implanted devices.

A SOI circuit to discriminate Pulse-Width Modulation (PWM)-encoded data has been designed as part of a neuro-stimulator for a visual prosthesis project [3]. Commonly, PWM encoding and decoding techniques for data transmission are well known and easily accomplished. Discrimination is simplified when a clocking signal, locked-up to the main high-frequency encoding clock, is made available at the local receiver, as usually happens in network communication. In such cases, chip complexity or low-power consumption does not necessarily represent a major design constraint, however. Data can also be decoded by using the PWM signal to control the charge of an integrator with a reference applied to its input and taking the dc component of the resulting truncated ramp [4]. Nevertheless, low-pass filtering would demand very large on-chip RC values, prohibitive to body-implanted applications.

This paper introduces a four-step bit-discrimination technique that handles the requisite of a unique input to the PWM decoder. Owing to inherent coupling losses in the transcutaneous link, it should also accomplish good immunity to variations on power supply and input-data level. Furthermore, the proposed circuit should be

*Based on a "Low-Power Silicon-on-Insulator PWM Discriminator for Biomedical applications" which appeared in IEEE ISCAS 2000, Geneva, Switzerland. © 2000 IEEE

†Corresponding author. E-mail: delima@feg.unesp.br
‡E-mail: verleysen@dice.ucl.ac.be

ISSN 1065-514X print/ISSN 1563-5171 online © 2002 Taylor & Francis Ltd
DOI: 10.1080/1065514021000012075

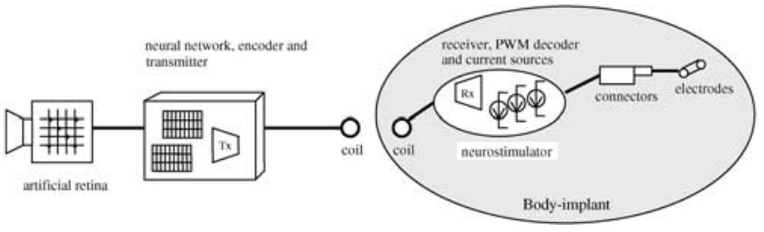

FIGURE 1 Visual prosthesis system.

compatible to low-voltage supplies and operate in the megahertz range while keeping power consumption at acceptable levels.

The organization of this paper is as follows. In the second section, the goals and achievements of the neurostimulator are discussed. In the third section, a classification of CMOS/SOI structures and basic SOI MOSFET modeling are briefly reviewed. The fourth section describes the PWM decoding technique and proposed circuit. Design procedures and simulation data are discussed in the fifth section. Experimental results are presented in the sixth section. Discussion and concluding remarks are summarized in the seventh section.

VISUAL PROSTHESIS

An electronic device intended to be used as a visual prosthesis for blind people has been developed [3]. Some blind patients, like those who suffer from *Retinitis Pigmentosa*, still have their optic nerve intact. The possibility to electrically stimulate such a nerve, and therefore, generate *phosphenes* (visual sensations) is, thus, investigated. Electrical stimulation is achieved through a cuff electrode wrapped around the optic nerve. The electrode is formed by several contacts connected to an electronic device generating current pulses. It has been demonstrated that cuff electrodes with several contacts may be used to selectively activate fibers or groups of fibers in a nerve [5]. In the current project, this principle is applied to the human optic nerve [6].

An overview of the electronic devices developed is given in Fig. 1. At the left of the chain, an image is captured by a digital camera. The artificial eye corresponds to a two-dimensional array of pixels containing photo-detectors and processing units mimicking the neural networks of the retina with real-time, parallel massive computation capabilities. This image is transformed into a digital sequence by means of image processing techniques and realized by an external digital processor. The digital sequence is then transmitted to an internal processor, part of the body-implant, through a RF transcutaneous link. Two flat coils, fixed to each side of the skin, act as transmitting and receiving loop antennas. A receiver, a single-input PWM decoder and controlled current-sources complete the body-implanted neurostimulator. RF transmission of both data and power [7] is based on a technology developed for cochlear implants. The digital sequence embeds the parameters used by the neurostimulator to generate current pulses to the four electrode contacts.

Since human experimentation takes place, it is worth noticing that safety and reliability constraints prevail over any technical consideration in the development of such a device. For this reason, the choice of the type of data being transmitted through the transcutaneous link aimed to simplify the intra-corporal part as much as possible, even at the cost of an increased complexity in the external processor. The proposed technique consists in transmitting discretized values of the current amplitude into each contact of the four electrodes, at every time-step as shown in Fig. 2 [8]. In accordance with the planned physiological experimentation, time-step has been fixed to 20 μs, and current amplitude ranges from -6 to 6 mA, by relative steps of less than 10%. If one adds the necessary commands and control bits, corrector bits, etc., the required bandwidth is approximately 3 Mbit/s.

Power transmission through the link not only simplifies the design of the implanted processor but it is also compulsory since consumption demands are too high to consider a battery implant, as in some pacemakers. The implanted-device consumption, including the power injected through the electrode contacts, is estimated to 200 mW. Finally, a back channel (from the implanted part to the external circuit) should also be provided in order to transfer control information as well as measurements of the current amplitude across the electrode contacts and their impedance, and others.

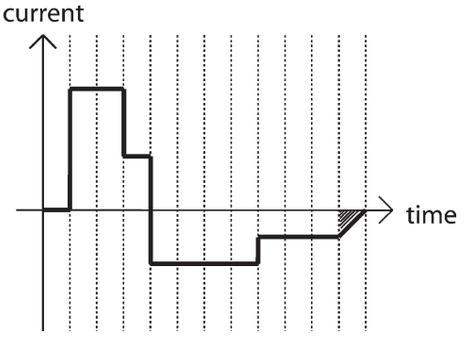

FIGURE 2 Typical staircase current waveform; the hatched pulse results from automatic charge recovery.

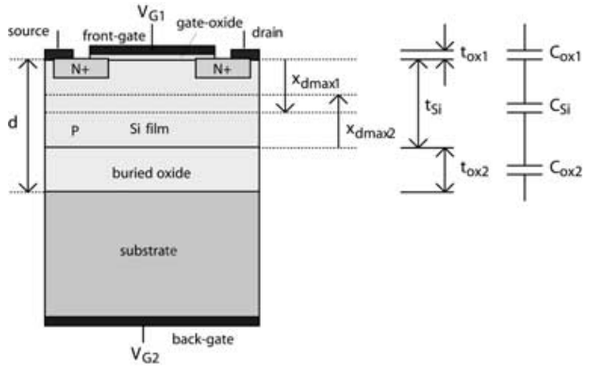

FIGURE 3 Cross-section of a SOI transistor.

Inevitably, such power and data-rate requirements lead to contradictory specifications. As a compromise, FSK modulation on 6 MHz data has been specified, together with a class-D modulator. This paper focuses on the design and realization of a PWM demodulator that satisfies the above specifications. A SOI circuit has been designed for power-consumption reasons.

SOI MOSFET DESIGN PARAMETERS

The cross-section of a N-channel SOI MOSFET is depicted in Fig. 3, where the thickness of different layers and intrinsic capacitances are identified. Beneath the Si-film that lodges active devices, a buried-oxide layer, grown before any transistor processing starts, provides electrical isolation to prevent from most parasitic effects experienced in conventional bulk transistors as they find their origin in the interaction between devices and substrate. A thick Si-substrate merely provides mechanical support to the whole structure and plays no role in the transistor electrical characteristic. The mechanisms of channel formation and carrier transportation of a SOI transistor are similar to those of a standard MOSFET [9]. The main difference, however, is that the former is dually controlled by front- and back-gate bias. Both gates induce depletion regions with widths x_{dmax1} and x_{dmax2} (indices 1 and 2 stand for the front- and back-gate interface, respectively), leading to a classification of SOI transistors: (a) *partially-depleted* (PD), where $d > x_{dmax1} + x_{dmax2}$, and (b) *fully-depleted* (FD), when the Si-film is totally depleted by front-gate bias, so that $d < x_{dmax1} + x_{dmax2}$.

Thin-film SOI transistors feature a Si-film thickness smaller than $x_{dmax1} + x_{dmax2}$ and are fully-depleted at threshold, regardless of back-gate biasing, although either a thin accumulation- or depletion-layer at the back-gate interface can be present. FD transistors exhibit the most attractive properties such as lower electric fields, higher mobility and small-signal transconductance, reduced stray capacitances, lower body-effect coefficient, better short-channel behavior and a quasi-ideal subthreshold slope [1].

TABLE I Basic modeling of a FD SOI MOSFFET

Saturation current I_{Dsat} [A]	$I_{Dsat} \cong \frac{\beta}{2n}(V_{G1} - V_{TH})^2$
Body-effect coefficient $\gamma = \partial V_{TH}/V_{G2}$ [−]	$\gamma = -\frac{C_{Si}C_{ox2}}{C_{ox1}(C_{Si}+C_{ox2})} = -(n-1)$
Transconductance $g_m = \partial I_{Dsat}/V_{G1}$ [A/V]	$g_m = \sqrt{\frac{2\beta I_{Dsat}}{n}}$
Subthreshold slope S [V]	$S = \frac{kT}{q} n \ln(10)$
Transistor gain-factor β [A/V^2]	$\beta = (W/L)\mu C_{ox1}$

The operation mode of a FD transistor (enhancement or accumulation) depends on fabrication parameters, mainly the type of gate-material used. Owing to the inherent difficulty to block Boron diffusion into the gate-oxide, identical doping-impurity (Phosphorus) in the poly-Si gate-material is normally used to implement both types of transistors. As a result, N- and P-channel transistors operate, respectively, on enhancement- (EM) and accumulation-mode (AM), the latter having the same doping polarity for source, drain and body regions.

Adopting standard MOSFET symbology, the basic modeling and small-signal parameters for a grounded-source FD SOI MOSFET with a depleted back-gate interface are reviewed in Table I [1]. As it can be noted, conventional bulk-transistor equations can be applied to model FD SOI devices, with the exception of the body-effect coefficient γ, which is now dimensionless and constant, as it remains first-order independent of the Si-film doping concentration and the channel-to-substrate voltage, improving thus the device large-signal linearity. The threshold-voltage dependence on back-gate bias V_{G2} is linear, unlikely in bulk transistors. Design techniques developed for conventional CMOS circuits can thus be straightforwardly employed to the synthesis of CMOS/SOI circuits built up of thin-film FD transistors.

PWM DECODER DESCRIPTION

Figure 4 shows the decoder single input, a sequence of pulses D_{in} with a fixed frequency $f_{in} = 1/T_{in}$. Encoded by PWM, the incoming information is expressed in terms of the parameter α, whose value is referenced to a duty-cycle of 50%. A coded "0" corresponds to a pulse shorter than

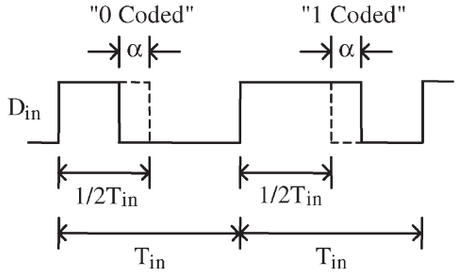

FIGURE 4 Incoming PWM encoded data.

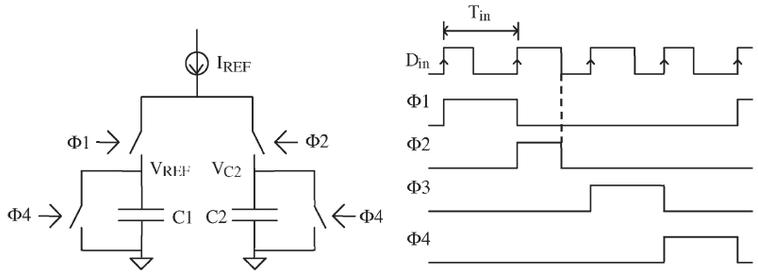

FIGURE 5 Double-integration concept ($C_1 = 2C_2$) and non-overlapping control phases.

$1/2T_{in}$ and is represented by $\alpha < 0$. Conversely, a logic "1" implies in a pulse longer than $1/2T_{in}$ and $\alpha > 0$. As no clock or synchronizing signal is made available, the arbitration condition corresponding to a 50%-duty cycle pulse ($\alpha = 0$) has to be internally generated. Therefore, the discriminator resolution depends on the accuracy of establishing such a condition.

The proposed double-integration discrimination technique is shown in Fig. 5, where lossless capacitors C_1 and C_2 are charged by a current source I_{REF} through ideal switches. These capacitors are grounded from one side and do not suffer from parasitic coupling to substrate. Full bit-discrimination demands four cycles: *precharge* (Φ_1), *sampling* (Φ_2), *comparison* (Φ_3) and *reset* (Φ_4). All non-overlapping phases are asserted during a period T_{in}, with exception of Φ_2 that coincides with incoming pulse D_{in} and has, therefore, duration of $(1/2T_{in}) \pm \alpha$. The discrimination is carried out as follows. Upon precharging ($\Phi_1 =$ "1"), capacitor C_1 reaches a reference voltage V_{REF} after period T_{in}. On sampling ($\Phi_2 =$ "1"), capacitor C_2 is charged as long as D_{in} remains at a high level, developing a voltage V_{C2}. By setting $C_1 = 2C_2$, V_{REF} ideally corresponds to the arbitration condition $\alpha = 0$. By neglecting the clock-feedthrough effect on stored charges, a comparison ($\Phi_3 =$ "1") between sampled-and-held voltages V_{REF} and V_{C2} assigns the digital value to the encoded parameter α. Upon resetting ($\Phi_4 =$ "1"), the comparator output is latched and capacitors discharged.

The decoder block-diagram is shown in Fig. 6. It comprises of a schmitt-triggered edge-detector (ST/ED), a phase-generator (PG) and four integrator–comparator (INT/CMP) blocks. The input-clock to PG is derived in ST/ED upon detecting the positive transitions of incoming bit-stream. Since no external resetting signal is present, hazardous phase-generation on powering-up is avoided by turning unstable spurious states in the finite-state machine of PG. As four phases are required to accomplish the discrimination of one bit, the same number of integrator–comparator sets is needed. A continuous and sequential decoding of D_{in} is ensured by rotating the control phases in INT/CMP blocks as indicated, so that phases [Φ_1, Φ_2, Φ_3, Φ_4], as generated by the PG block, are connected as [Φ_1, Φ_2, Φ_3, Φ_4] to INT/CMP$_1$, [Φ_2, Φ_3, Φ_4, Φ_1] to INT/CMP$_2$, [Φ_3, Φ_4, Φ_1, Φ_2] to INT/CMP$_3$ and [Φ_4, Φ_1, Φ_2, Φ_3] to INT/CMP$_4$. For instance, when precharging occurs in INT/CMP$_1$, sampling, comparison and resetting are simultaneously performed in INT/CMP$_2$, INT/CMP$_3$ and INT/CMP$_4$, respectively. Decoded information is then sequentially output at OUT$_1$, OUT$_2$, OUT$_3$ and OUT$_4$.

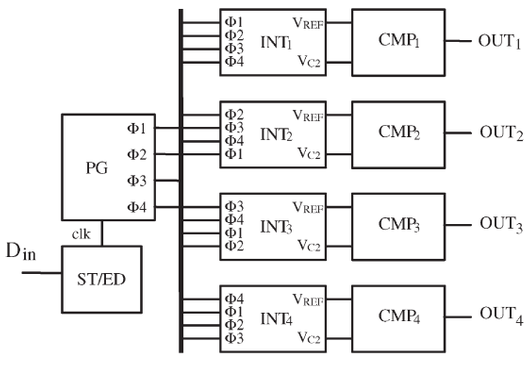

FIGURE 6 Decoder block diagram.

Fast-settling Comparator

The accuracy and frequency range of the proposed decoding technique depend essentially on the comparator characteristics such as resolution and propagation delay. The basic schematic of a simple low-voltage, fast-settling comparator is presented in Fig. 7. It consists of a preamplifier made up of a differential pair loaded by diode-connected transistors (M_1–M_{14}), a current subtractor based on wide-swing current-mirrors (M_{15}–M_{18}) [10] and a latch stage (M_{19}–M_{22}), which by means of positive feedback improves the recovery at nodes X and Y when $\Phi_3 =$ "1", speeding up comparison and providing full-scale digital output-swing. Bias voltages V_{CP} and V_{CN} are properly chosen to minimize the current-mirror voltage compliance to $2\,V_{DSAT}$.

The comparison is carried out as follows. Capacitance C_X is initially discharged by $\Phi_3 =$ "0" and node Y preset as capacitance C_Y is charged to V_{DD}. Upon perfect device matching, a condition $V_{REF} > V_{C2}$ at the beginning of the comparison cycle implies $I_B > I_A$ and $I_D = I_C = I_B - I_A > 0$ is imposed by the current subtractor so that C_X begins to be charged. As C_Y discharges through M_{19}, device M_{21} turns on and reinforces the charge of C_X, knocking down the voltage at node Y as positive feedback

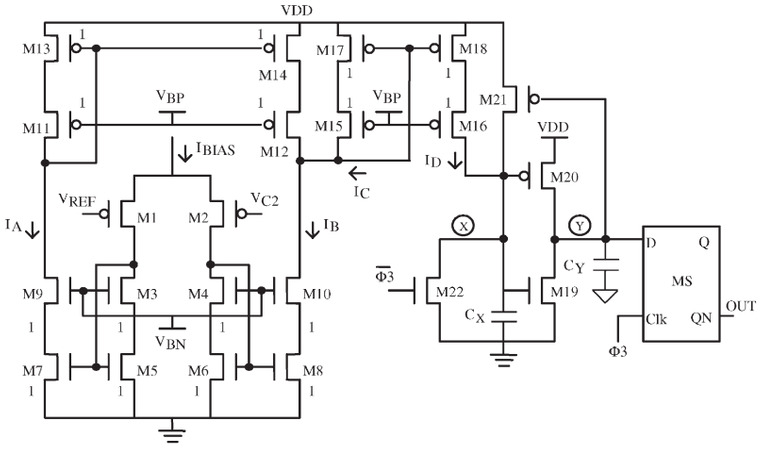

FIGURE 7 Simplified schematic of low-voltage comparator.

develops. On the other hand, $V_{REF} < V_{C2}$ yields $I_B < I_A$ and $I_D = I_C = 0$. In this case, C_X remains uncharged and node Y preset. Since the output node is isolated from the input by current mirrors, no kickback effect at the comparator input occurs as full output-swing is attained. Clocked by Φ_3, a second master-slave latch holds the comparison result over the four subsequent phases.

The comparator bias current I_{BIAS} is derived from an on-chip reference-current source whose basic schematic is shown in Fig. 8. Transistors M_{22} and M_{23} work on weak inversion, so that $I_R = (1/R)U_T \ln A$ [11] where U_T is the thermal voltage and A corresponds to the ratio W_{22}/W_{23}, for a fixed channel-length L. Devices M_{24}–M_{28} operate on strong inversion to improve current mirroring [11] and generate $I_{BIAS} = BI_R$, where B is the weighting factor.

As small values of α can be regarded as a small-signal overdriving, an insight into the comparator worst-case propagation delay and its dependence on design parameters can be obtained by individually analyzing the small-signal time-constants of amplifying stages. In such analyses, transistors are assumed on strong inversion and saturation region.

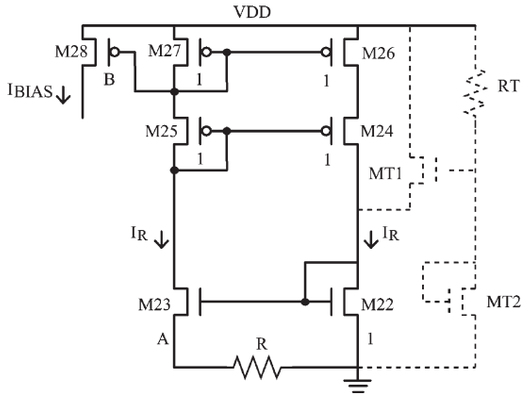

FIGURE 8 On-chip reference-current source.

Considering $r_{o3} \cong r_{o5}$ and $g_{m3}r_{o5} \gg 1$, which normally occurs, the small-signal voltage gain of the preamplifier is given by

$$A_{V1} \cong \frac{g_{m1}}{g_{m5}} = \sqrt{\frac{(W/L)_1}{(W/L)_5}} \tag{1}$$

with dominant-pole and unit-gain frequencies $\omega_c = g_{m5}/C_A$ and $\omega_t = g_{m1}/C_A$, respectively, where C_A is the stage load-capacitance. The preamplifier transient response is then imposed by $\tau_1 = 1/\omega_c = C_A/g_{m5}$ and can be improved by reducing C_A and/or increasing g_{m5}. Small sizes W and L assigned to transistors M_3–M_4 and M_9–M_{10} minimize the capacitance C_A. Raising g_{m5} speeds up settling node X at the expense of lower voltage gain, however, so that a design trade-off between A_{V1} and g_{m5} should be achieved.

When a linear positive-feedback takes place, the regeneration time-constant of the latch can be estimated by the equivalent small-signal circuit of Fig. 9. Applying Kirchhoff's laws, one has

$$v_x - v_y = (g_{m19} + g_{m20})R_Y v_x - g_{m21}R_X v_y - R_X C_X \frac{dv_x}{dt} + R_Y C_Y \frac{dv_y}{dt} \tag{2}$$

where R_X and R_Y represent the load resistances. In order to get an exploitable outcome, simplifying assumptions are adopted, such as $C_X \cong C_Y$ and $R_X \cong R_Y$. Additionally, if $g_{m21} = g_{m19} + g_{m20}$ is imposed by design and denoting $\Delta v = v_x - v_y$, it results

$$\Delta V = \tau_2 \frac{d\Delta v}{dt} \tag{3}$$

where $\tau_2 = C_X/g_{m3}$ is the latch time-constant. Assuming that C_X and C_Y are mainly formed by channel capacitance $C_{ch} = WLC_{ox}$, it comes out that τ_2 is proportional to $L^2/[\mu(V_{GS} - V_{TH})]$ and can be regarded as relatively constant for a given technology. Therefore, by imposing

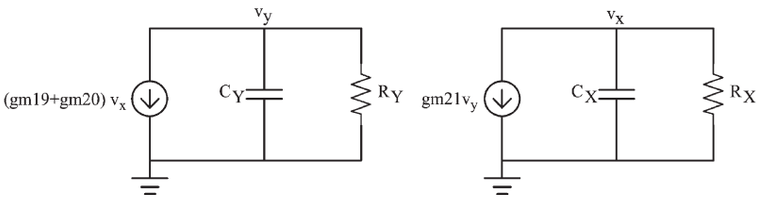

FIGURE 9 Equivalent small-signal circuit of latch.

minimum channel length to M_{19}–M_{21}, the propagation delay of the regenerative latch is reduced.

CIRCUIT DESIGN AND SIMULATION

In order to meet design specifications, the circuit has to decode data at $f_{in} = 6\,\text{MHz}$ for $|\alpha| \leq 8.33\,\text{ns}$, or $|\alpha_{\%}| \leq 10\%$. A single 3.3 V-power supply is initially adopted, although the design approach can be extended to lower supply voltages. The PWM decoder was sized according to parameters of a low-voltage 2 μm CMOS/SOI fabrication process. Typical large-geometry parameters are $V_{THN} = 0.4\,\text{V}$, $V_{THP} = -0.4\,\text{V}$, $T_{ox} = 30\,\text{nm}$, $\mu_n = 467\,\text{cm}^2/\text{V s}$ and $\mu_p = 142\,\text{cm}^2/\text{V s}$.

Since the accuracy of discrimination relies on excellent matching between capacitors ($C_1/C_2 = 2$) in the integrator, stray capacitances associated with comparator input-transistors and routing should be carefully considered. Adopted values are $C_1 = 4.1056\,\text{pF}$ and $C_2 = 2.0528\,\text{pF}$. As V_{C2} reaches its peak for $\alpha_{\%} = 0$, the I_{REF} value is estimated $@V_{C2max} = 3.3\,\text{V}$ and corresponds to 40 μA. As C_1 and C_2 are only charged by I_{REF} during Φ_1 and Φ_2, respectively, a same current source I_{REF} is time-shared between two INT/CMP blocks in order to reduce power consumption and mismatching. On-chip reference current is 0.75 μA, from which the tail-current of the comparator $I_{BIAS} = 5\,\mu\text{A}$ is mirrored. Transistor sizing is listed in Table II. The comparator input common-mode range (CMR) corresponds to $0.73\,\text{V} \leq \text{CMR} \leq 2.72\,\text{V}$.

Simulation was carried out with ELDO whose built-in models implement the equations described in [12], with a set of parameters optimized to fit the IV characteristic of transistors fabricated with the process to be used. Upon ideal matching, Table III lists the range of decodable values of $\alpha_{\%}$ as function of temperature. At worst-case temperature of 40°C, an incoming D_{in} with encoding parameter within interval $3.18\% \leq |\alpha_{\%}| \leq 47.1\%$ can be correctly discriminated. For such values of $\alpha_{\%}$ it results $0.92\,\text{V} \leq V_{C2} \leq 2.61\,\text{V}$, so that the sampled voltage across C_2 is kept inside the comparator CMR.

TABLE II Drawn sizing of comparator transistors

	M_{1-2}	M_{3-18}	M_{19}	M_{20}	M_{21}	M_{22}
W (μm)	30.0	8.0	12.0	6.0	15.0	12.0
L (μm)	3.0	4.0	2.0	2.0	2.0	2.0

Figure 10 displays the output waveforms at nodes OUT_1–OUT_4 from circuit simulation, having as input an encoded bit-stream [0,1,1,0,0,0,0,1,0,1,0…] at $f_{in} = 6\,\text{MHz}$, $\alpha_{\%} = 10\%$ and $T = 40°\text{C}$. Indices 1–4 indicate the corresponding control phases as input to $INT/COMP_1$. An interpretation of some results follows. Assuming all outputs initially at "0", bit "1" at time-step 2_a is sampled by $INT/COMP_1$ and discriminated as OUT_1 at the beginning of step 4_a. Similarly, Bit "1" at step 3_a is sampled by $INT/COMP_2$ and discriminated as OUT_2 at the start of step 1_b and thus successively.

EXPERIMENTAL RESULTS

In accordance with Fig. 6, the PWM decoder was integrated on a 2 μm single-poly, single-metal thin-film CMOS/SOI fabrication process at Microelectronics Laboratory, Catholic University of Louvain, Louvain-la-Neuve. N- and P-channel transistors are fully-depleted devices with depleted back-gate interface, operating in enhancement and accumulation modes, respectively. The circuit effective-area is approximately $2\,\text{mm}^2$ and its microphotograph is displayed in Fig. 11. Typically, minimum recognizable parameter $\alpha_{\%}$ was below 10% at 6 MHz and $V_{DD} = 3.3\,\text{V}$. As attested by process characterization, significant transistor mismatching limits the comparator resolution to nearly 7 mV and degrades the α resolution, therefore.

Experimental waveforms of incoming and decoded data at 6 MHz and 3.3 V are shown in Fig. 12a,b, for a sequence of pulses generated with a constant encoding parameter $\alpha_{\%} = -10\%$ and $\alpha_{\%} = +7\%$, respectively. On the absence of incoming data, idle consumption is 340 μW. Figure 13 shows the highest operating frequency as function of power supply. Encoded pulses with frequencies up to 15 MHz and $\alpha_{\%} = 10\%$ can be discriminated for V_{DD} spanning from 2.3–3.3 V. Such a result represents a satisfactory immunity to supply-voltage perturbations,

TABLE III Limit values of parameter $\alpha_{\%}$ as determined by temperature

T (°C)	$\alpha_{min\%}$ (%)	$\alpha_{max\%}$ (%)	$V_{C2\,min}$ (V)	$V_{C2\,max}$ (V)
15	3.13	52.1	0.76	2.70
25	3.16	49.9	0.87	2.66
40	3.18	47.1	0.92	2.61

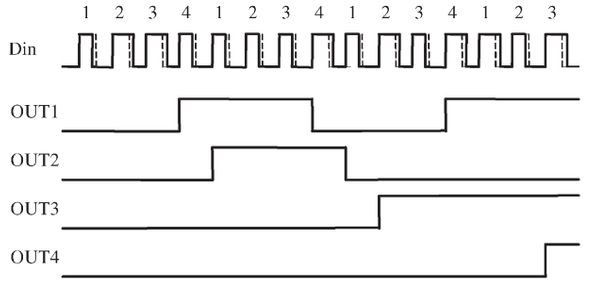

FIGURE 10 Simulated output waveforms for different encoding parameter ($\alpha > 0$ and $\alpha < 0$).

as demanded for body-implanted applications powered by a transcutaneous link.

CONCLUSION

A CMOS/SOI PWM discriminator intended for low-voltage biomedical applications, as part of a body-implanted neurostimulator in a visual prosthesis, was designed. Based on a double-integration concept, the novel decoding technique does not require low-pass filtering and meets a design restriction of having the incoming bit-stream as the sole signal to the decoder. Consequently, the arbitration condition equivalent to encoding parameter $\alpha = 0$ is internally generated. The proposed technique is accomplished in four subsequent cycles. Furthermore, it provides good accuracy of discrimination while keeping circuit complexity and power consumption at acceptable levels. For a 2 μm single-poly, single-metal CMOS/SOI fabrication process, the chip size is around 2 mm^2.

The minimum recognizable encoding parameter α was typically below 10% at nominal operating-frequency and supply-voltage of 6 MHz and 3.3 V, respectively. On the absence of incoming data, idle power consumption is 340 μW. The experimental resolution of the comparator corresponds to 7 mV and is limited by component mismatching. The decoder is capable to reach operating

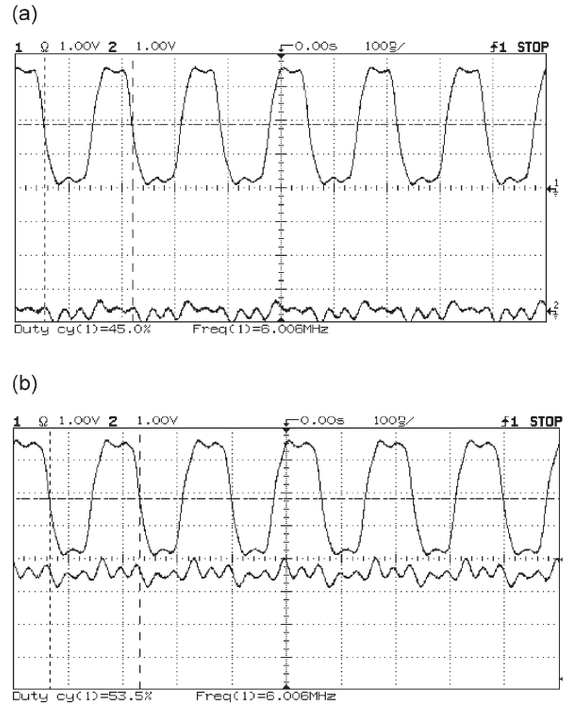

FIGURE 12 Discriminator response to $\alpha = -10\%$ @$f = 6$ MHz (a) and $\alpha = +7\%$ @$f = 6$ MHz (b).

frequencies as high as 15 MHz for a 10%-encoding parameter. An excellent immunity to power-supply variations is verified since information can be discriminated for V_{DD} ranging from 2.3–3.3 V. Although a nominal 3.3 V-supply was initially specified, the presented circuit can be re-sized to accommodate lower values of V_{DD}.

Acknowledgements

The authors would like to express their thankfulness to Brazilian Foundation FAPESP for financial assistance (grants 97/09613-0 and 98/04295-3) and continuous support on integrated circuits research, to the Belgian FNRS (National Fund for Scientific Research) for

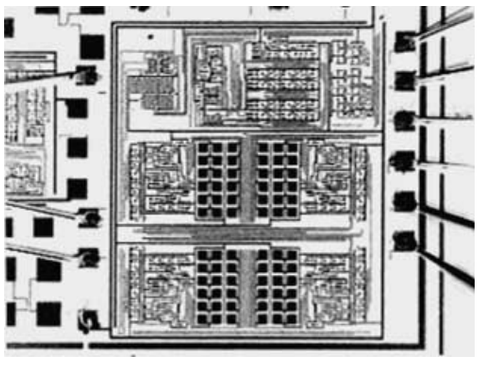

FIGURE 11 Die microphotograph.

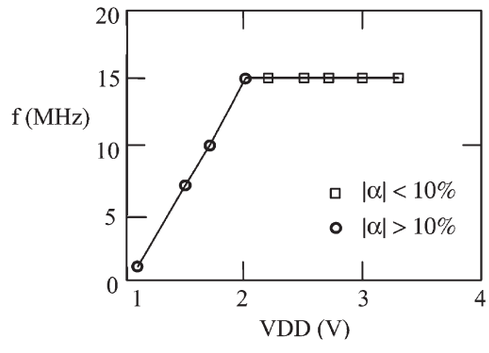

FIGURE 13 Maximum operation frequency against supply voltage.

financial assistance on the UNESP-UCL collaboration, and to the Mivip Esprit project LTR22527, funded by the European Commission. Michel Verleysen is a research fellow of the Belgian FNRS.

References

[1] Colinge, J.P. (1997), Chapter 5, Silicon-on-Insulator Technology: Materials to VLSI, 2nd ed, (Kluwer Academic Publishers, Dordrecht).
[2] Bernstein, K. and Rohrer, N. (1999) SOI Circuit Design Concepts (Kluwer Academic Publishers, Dordrecht).
[3] Microsystems Based Visual Prosthesis (MIVIP), ESPRIT4, Project Reference: 22527.
[4] Couch, II, L. (1994) Modern Communication Systems (Prentice-Hall, Englewood Cliff, NJ).
[5] Veraart, C., Grill, W. and Mortimer, J.T. (1993) "Selective control of muscle activation with a multipolar nerve cuff electrode", *IEEE Transactions on Biomedical Engineering* **40**, 640–653.
[6] Veraart, C., Delbeke, J., Wanet-Defalque, M.-C., Vanlierde, A., Michaux, G., Parrini, S., Glineur, O., Verleysen, M., Trullemans, C. and Mortimer, J.T. "Selective Stimulation of the Human Optic Nerve", *4th Conference of the International Functional Electrical Stimulation Society*, Aug. 1999, Sendai, Japan, 57–59.
[7] Huang, Q. and Oberle, M. (1998) "A 0.5-mW passive telemetry IC for biomedical applications", *IEEE Journal of Solid State Circuits* **33**, 937–946.
[8] Doguet, P., Mevel, H., Verleysen, M., Troosters, M. and Trullemans, C. "An Integrated Circuit for the Electrical Stimulation of the Optic Nerve", *IFESS'2000, 5th Conference of the International Functional Electrical Stimulation Society*, 18–20 June 2000, Aalborg, Denmark, 309–312.
[9] Tsividis, Y.P. (1998) Operation and Modeling of the MOS Transistor (McGraw-Hill, New York).
[10] Johns, D. and Martin, K. (1997) Analog Integrated Circuit Design (Wiley, New York).
[11] Vittoz, E. (1993) In: Franca, J. and Tsividis, Y., eds, Design of VLSI Circuits for Telecommunication and Signal Processing (Prentice-Hall, Englewood Cliff, NJ).
[12] Enz, C., Krummenacher, F. and Vittoz, E. (1995) "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications", Analog Integrated Circuits and Signal Processing (Kluwer Academic Publishers, Dordrecht) **Vol. 8**, pp. 83–114.

Jader A. De Lima obtained both BS (1977) and MS (1980) degrees in EE from Universidade de Sao Paulo, Brazil, and his Ph.D. (1984) degree in EE from Universidade Estadual de Campinas, Brazil. Research Assistant at the University of Edinburgh, UK, from 1986 to 1989. He jointed then Motorola (EDO), in Geneva, Switzerland and FASELEC/Philips in Zurich, Switzerland. He was also design leader at Thomson Consumer Electronic Components, in Grenoble, France. Currently, he is an Associate Professor at Universidade Estadual Paulista, Brazil. His research interests are micropower analogue design, continuous-time filters and biomedical instrumentation.

Sidnei F. Silva received his BS degree in Electrical Engineering from Universidade Estadual Paulista, Brazil, in 1998. As a student, he carried out several designs on analog micropower. Currently, he is working as an industrial process engineer.

Adriano S. Cordeiro is currently a graduation student in Electrical Engineering at Universidade Estadual Paulista, Brazil. He has undertaken some works on integrated circuit designing and already co-authored a few papers. His major interests are low-voltage analog design and biomedical instrumentation.

Michel Verleysen received the M.Sc. and Ph.D. degrees from the Université Catholique de Louvain (Belgium), in 1987 and 1992 respectively. In 1992, he was Invited Professor at the EPFL, Lausanne, Switzerland). His research interests include artificial neural networks, data mining, VLSI implementations of learning systems, and biomedical electronic devices. He is a member of the IEEE, co-editor-in-chief of the Neural Processing Letters journal, and chairman of the European Symposium on Artificial Neural Networks. He is member of the editorial board of many neural networks and VLSI related journal, and of the scientific committee of many conferences on artificial neural networks.