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Pros and cons of symmetrical dual-*k* spacer technology in hybrid FinFETs

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ABSTRACT

The symmetrical dual-*k* spacer technology in hybrid FinFETs has been widely explored for better electrostatic control of the fin-based devices in nanoscale region. Since, high-*k* tangible spacer materials are broadly became a matter of study due to their better immunity to the short channel effects (SCEs) in nano devices. However, the only cause that restricts the circuit designers from using high-*k* spacer is the unreasonable increasing fringing capacitances. This work quantitatively analyzed the benefits and drawbacks of considering two different dielectric spacer materials symmetrically in either sides of the channel for the hybrid device. From the demonstrated results, the inclusion of high-*k* spacer predicts an effective reduction in off-state leakage along with an improvement in drive current. However, these devices have paid the cost in terms of a high total gate-to-gate capacitance (C_{gg}) that consequently results poor cutoff frequency (f_T) and delay.

1. Introduction

The invention of 3-D FinFET technology in the semiconductor era has been considerably enabled the advancement of electronics industry and have been of immense interest for sub-20 nm applications [1,2]. The fin based devices are excellent in suppressing the short channel effects (SCEs) and have superior control over the carriers in the channel [3–7]. This improvement in technology facilitates a longer battery lifetime and energy efficient electronics in both operating regions *i.e.*, high performance (HP) and low power (LP). According to the reported articles and International Technology Roadmap for Semiconductors (ITRS) prediction, the 3-Dimensional topology is here to expedite the profitable industries likely to 5-nm technology node [8,9]. The only modifications in lower nodes is either in physical architecture like nanowires and nanotubes or incorporation of new materials in the channel such as Ge, GaAs, SiGe, etc. keeping the CMOS compatibility [10–12]. Today's market is more consensus about the HP consumer applications and may continue for subsequent years. The HP applications primary goal is to achieve high current drivability with higher packing density instead of bothering regarding the static leakage current [11,13]. So, to achieve the HP computing applications, a new transistor *i.e.*, hybrid FinFET was first proposed by *Zhang et al.* [14]. Henceforth further modification and continuous research on hybrid devices was carried by *Fahad et al.* [15,9] and *Pradhan et al.* [11,16,17]. Hybrid FinFETs merge several technologies in a single SOI platform namely 3-D FinFET and 2-D UTB MOSFET. However, to analyze further impact of spacer technology in the hybrid FinFETs, this work incorporates two different spacer materials symmetrically in the underlap region of either side of the channel for the hybrid

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device. Previously, the underlap FinFETs have showed immense control over SCEs [18,19]. But the major issues, which are faced by underlap FinFETs are the precise control of doping profile and an increased amount of underlap resistance. These issues are well tackled by Refs. [18–20] with an inclusion of high-*k* dielectric spacers at the underlap region. Similarly, *Pal et al.* [21,7] have examined that superior control on the channel and meaningful improvements are achievable in terms of I_{on} and I_{off} by contemplating dual-k spacers over the underlap regions. The above mentioned works are carried out contemplating the high-*k* spacer materials in the conventional 3-D FinFET structures. In this work, we have estimated the benefits as well as drawbacks of symmetrical inclusion of dual-*k* spacer in either side of the channel for the hybrid devices over conventional FinFETs. The lengths of both spacers (inner high-*k*, L_{hk}, and outer low-*k*, L_{lk}) are optimized for better circuit applications. The performances considered for this investigation are drive current (I_{on}), off state leakage current (I_{off}), effective drain current (I_{DEFF}), subthreshold slope (*SS*), transconductance (g_m), total gate capacitance (C_{gg}), output conductance (g_d), cutoff frequency (f_T), and gain (A_V).

The organization of the paper is as follows: Section 2 describes the architecture of hybrid FinFETs. Section 3 presents the simulation setup that discusses the methods and models considered for simulating the devices. In Section 4, the investigation is done for optimizing the length of dual-*k* spacer and the benefits and drawbacks of the high-*k* spacer inclusion. Finally, the concluding observations are pointed in Section 5.

2. Hybrid FinFET architecture with symmetrical dual-k spacer technology

The 3-D bird view of conventional SOI FinFET and hybrid FinFET with dual-*k* spacer technology architectures chosen for this work are presented in Fig. 1 (a) and (b) accordingly. Fig. 1(c) demonstrates the vertical and horizontal 2-D perspective views of both the devices. The SOI FinFET [6] offers significant control over SCEs and electrostatic parameters with a vertical thin channel and also have lesser fabrication complexity as compared to the bulk FinFET [22]. The major issues in SOI FinFET are self-heating effects because of the thick buried oxide and the cost factor. However, the self-heating effect is well-taken care by *Fiegna et al.* [23] and the cost factor is mitigated by the less complicated process steps. The 3-D FinFET and 2-D UTB technology are combined together to design the advanced hybrid topology. It predicts many advantages like maximum area efficiency, high packing density, and high drive current as studied in Refs. [14,9]. The key objective in this work is to establish symmetrical underlap regions at both sides of the channel towards source/drain and pattern the regions with two different dielectric spacer materials (Si_3N_4, $k = 7.5$ and HfO_2, $k = 22$). Then the benefits and drawbacks in performances of the designed device are compared with conventional FinFET [6]. The spacer lengths of Si_3N_4 is termed as L_{lk} and HfO_2 as L_{hk} and the ratio of L_{lk}:L_{hk} is varied to get an optimum ratio. The physical and electrical parameters are calibrated according to the ITRS specifications [8,6]. The SiO_2 with physical thickness of 0.9 nm is considered as gate oxide.

The channel is lightly doped to prevent the device from random dopant fluctuation (RDF) effect. Table 1 shows the physical dimensions for designing both the devices. Several technologies are merged in this work *i.e.*, 3-D FinFET + 2-D UTB + spacer

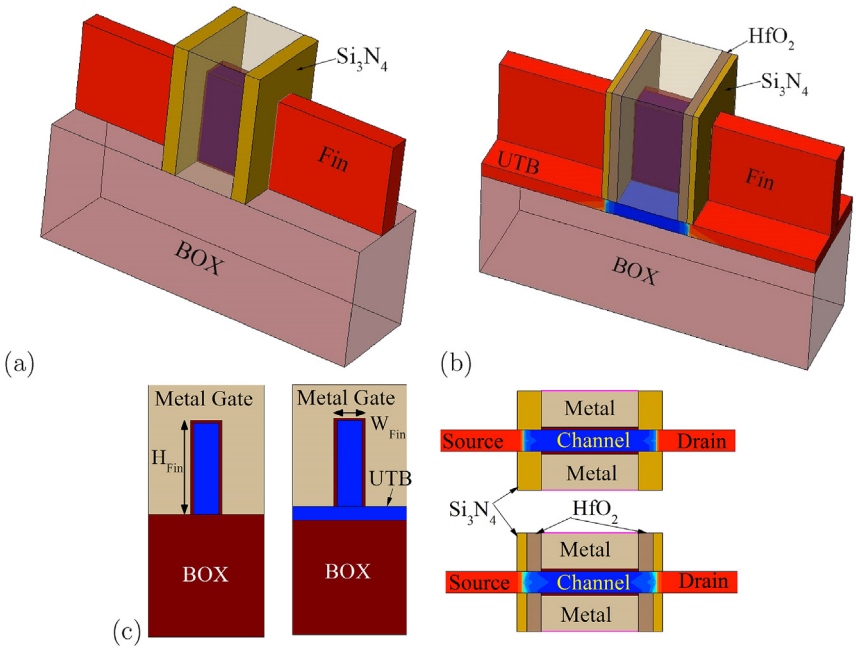

Fig. 1. (a) Typical trigate FinFET (D1) (b) Symmetrical dual-*k* spacer hybrid FinFET (D2, D3, D4, D5) (C) 2-D cut view of both devices.

Table 1
[a]Device design parameters.

Parameters	Nomenclature (nm)	Conventional FinFET	Symmetrical Dual-*k* hybrid FinFET
W_{Fin}	Fin Width	7 nm	7 nm
H_{Fin}	Fin Height	30 nm	H_{Fin}-UTB = 25 nm
L_g	Gate length	20 nm	20 nm
UTB	Ultra thin body thickness	–	5 nm
L_{lk}:L_{hk}	Length of low-*k*:Length of high-*k*	5:0 (D1)	1:4 (D2), 2:3 (D3), 3:2 (D4), 4:1 (D5)
t_{ox}	physical gate oxide thickness	0.9 nm	0.9 nm
L_T	Total device length	110 nm	110 nm
W_T	Total device width	32.2 nm	32.2 nm
BOX	Buried oxide thickness	40 nm	40 nm

[a] 2013 Overall roadmap technology characteristics (ORTC) ITRS parameters for 14 nm technology node FinFET.

engineering (two different dielectrics as inner high-*k* near to channel and outer low-*k* near to S/D in the underlap region). And a list of benefits and drawbacks for the adopted technology over conventional FinFET are systematically presented.

3. Simulation techniques

Comprehensive 3-D simulations are being carried out by Sentaurus TCAD [24] to evaluate the prospective benefits and drawbacks of the hybrid device over traditional one. The numerical process and device simulations allow crucial insights on the nature of semiconductor devices that can lead to new perceptions [24]. However, the simulation needs to be properly calibrated before designing any device. Hence, the validity of the simulator has been established according to our previous work [16]. The mobility model that accounts of doping, transverse field, and velocity saturation dependency along with the drift-diffusion (DD) model are considered in the simulation. The quantum confinement effect in fin and UTB which is determined from the density gradient based quantization model is also activated in the simulation. The Lombardi high-*k* model is considered to dealt with the high-*k* related mobility degradation effects [11,12]. To avoid the poly-Si gate depletion effects, the metal gate technology is used in this work. For better comparison among the devices, the threshold voltage (V_{th}) is kept at an approximate value for all device cases by carefully tuning the gate metal work function.

4. Performance evaluation

Fig. 2(a) shows the variation of electrostatic potential in the spacer and channel region (on state, V_{DS} = 0.7 V) for the conventional and the proposed hybrid FinFETs with increasing high-*k* spacer length (L_{hk}). It is noticed that the potential lines diverge from their path and give extra peaks at the two spacer interface near the drain side in case of hybrid FinFET.

As the inner high-*k* spacer length increases, the potential lines are well confined with an increase amount in the channel region and interface of the two spacers, which conclusively enhances the on-current (I_{on}) of the device. Similarly from Fig. 2(b), a significant improvement in SS (roughly 3.14%) can be observed in case of hybrid FinFET. D2 device gives the optimum SS value *i.e.*, 63.52 mV/decade, which is nearer to the ideal value (60 mV/decade) and the degradation occurs with decrease in L_{hk}.

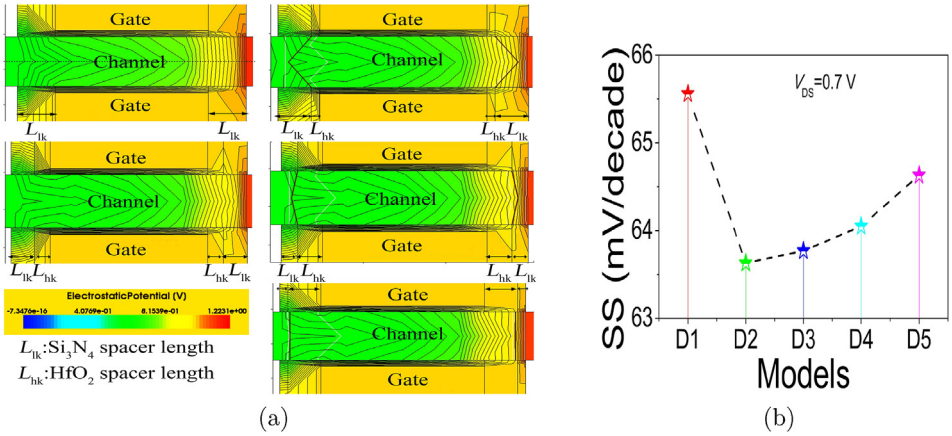

Fig. 2. Variation of electrostatic potential inside the channel and interface of the two spacers for conventional and hybrid FinFET for different L_{lk}:L_{hk} ratios at V_{DS} = 0.7 V.

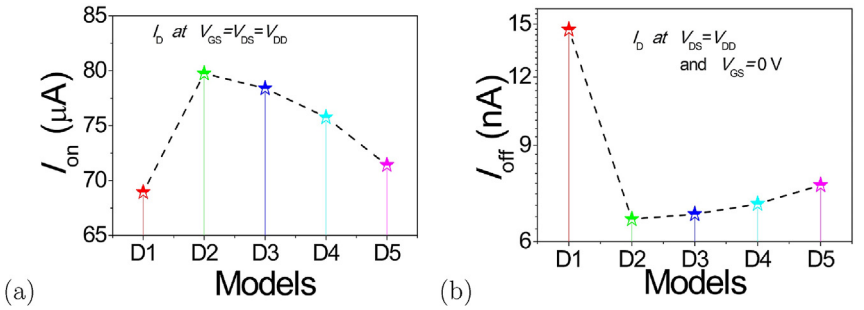

Fig. 3. Comparison among various architectures (a) I_{on} (b) I_{off}.

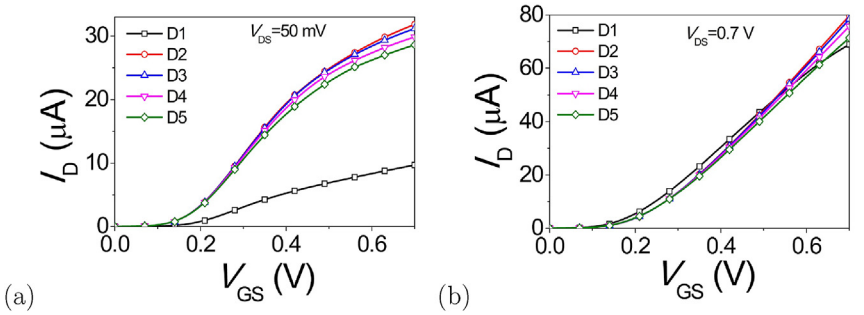

Fig. 4. Non-normalized I_D–V_{GS} performance analysis between conventional SOI FinFET and hybrid FinFETs at different L_{lk}:L_{hk} ratios for (a) V_{DS} = 50 mV (b) V_{DS} = 0.7 V.

An identical analogy can be made for I_{on} and I_{off} of our proposed device, which are presented in Fig. 3(a) and (b). The non-normalized on-current is compared between conventional FinFET and different topologies of hybrid channel FinFET in Fig. 3(a). The drive current of any device plays an important role in HP consumer applications. Hence, it is crucial to perceive the response of inner high-k spacer length (L_{hk}) on I_{off} and I_{on}. A sharp increase in I_{on} is identified with increase in L_{hk} up to an optimum value of 4 nm. The D2 (L_{lk}:L_{hk} = 1:4) architecture exhibits highest enhancement in I_{on} (around **1.23x**) from the conventional one *i.e.*, D1. This increase in I_{on} is partially because of the UTB (hybrid channel) and due to the inclusion of larger L_{hk}, which further modulates the carrier concentration in underlap region. Comparative analysis of I_{off} for different architectures is given in Fig. 3(b). The hybrid FinFETs with L_{lk}:L_{hk} = 1:4 shows an almost 60% of reduction in off-state leakage current as compared to conventional one.

Fig. 4(a) and (b) compare the transfer characteristic among conventional and hybrid FinFETs at different L_{lk}:L_{hk} ratios for both low and high V_{DS}. It can be observed that the inclusion of dual-*k* spacer over the underlap regions of the proposed hybrid FinFETs can able to deliver 66.66% higher non-normalized drive current with the same chip area as compared to conventional FinFET. Each nanometer increase in L_{hk} spacer of the hybrid FinFET leads to a increase in I_{on}. This enhancement in I_{on} with L_{hk} is because of the gate fringe induced barrier lowering (GFIBL) in the underlap region [18].

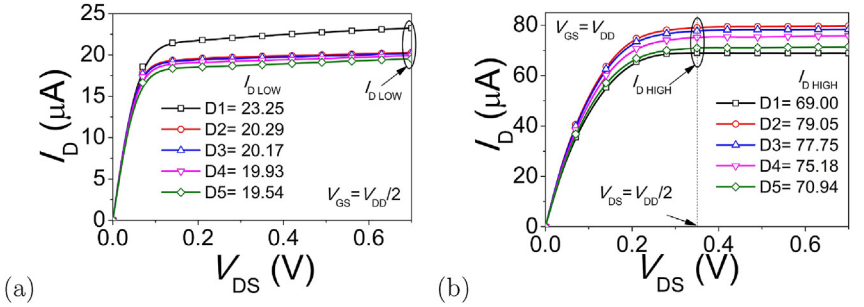

Fig. 5. Non-normalized I_D – V_{DS} performance comparison among conventional SOI FinFET and hybrid FinFETs at different L_{lk}:L_{hk} ratios for (a) V_{GS} = V_{DD}/2 (b) V_{DS} = V_{DD}.

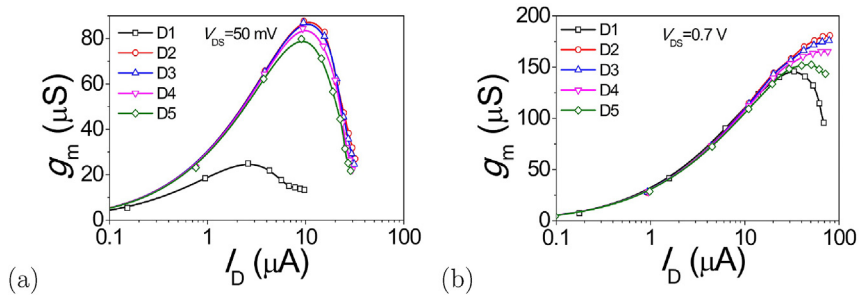

Fig. 6. g_m–I_D performance analysis between conventional SOI FinFET and hybrid FinFETs at different L_{lk}:L_{hk} ratios for (a) V_{DS} = 50 mV (b) V_{DS} = 0.7 V.

The I_D–V_{DS} of the hybrid FinFETs with spacer technology are compared to the conventional FinFET at $V_{GS} = V_{DD}/2$ and V_{GS}=V_{DD} as shown in Fig. 5(a) and (b) respectively. I_{DLOW} ($V_{GS} = V_{DD}/2, V_{DS} = V_{DD}$) and I_{DHIGH} ($V_{GS} = V_{DD}, V_{DS} = V_{DD}/2$) are calculated to evaluate the effective drain current ($I_{DEFF} = (I_{DLOW} + I_{DHIGH})/2$), which estimates the effective drain current drawn during switching. It is more realistic and way less optimistic than I_{DSat} assessment. By observing the inset values of I_{DLOW} and I_{DHIGH} from Fig. 5, it is clear that the device having high L_{hk} provide more I_{DEFF}. The D2 device (L_{lk}:L_{hk} = 1:4) delivers I_{DEFF} = (20.29 + 79.05)/2 μA = 49.67 μA, which is optimum from any other cases and is nearly 7.6% higher than the conventional FinFET (D1).

Fig. 6(a) and (b) show the plot of g_m for a conventional FinFET and different topologies of hybrid FinFETs with varying L_{lk}:L_{hk} ratio at high (V_{DS} = 0.7 V) and low (V_{DS} = 50 mV). To analyze the immense improvement in g_m ($\partial I_D/\partial V_{GS}$) with an increase in L_{lk}:L_{hk} spacer ratio, we have evaluated and studied the $I_D - g_m$ curve. According to the literature, access resistance problem is more serious in conventional trigate FinFETs. However, some solutions are available like increasing the H_{Fin} out of the gate region [25]. The parasitic resistance problem can be avoided by using a UTB in FinFET technology, *i.e.*, hybrid FinFETs with higher L_{hk} spacer length, which further increases the drain current. This is also validated from Figs. 4–6, both the parameters *i.e.*, on-current, I_{DEFF}, and g_m are increasing with the increase in L_{hk} in hybrid FinFETs. This is primarily due to the fringing field induced inversion charge modulation inside the underlap region. The charge-based model of g_m for undoped multigate MOSFETs are represented as [26]:

$$g_m = \partial I_D/\partial V_{GS} = \left(\mu W \Big/ L_{eff}\right)(Q_S - Q_D) \tag{1}$$

where Q_D and Q_S represent the gate-to-drain and gate-to-source charges, μ is the electron mobility, W, and L_{eff} are the width and effective channel length of the device. From Eq. (1), the g_m is directly related to the source/drain charge difference ($Q_S - Q_D$) and μ. In subthreshold region (low V_{DS} and V_{GS}), the Q_S of the hybrid FinFETs increases moderately because of the immense gate control and in the mean time Q_D remains almost constant as the gate induced fringing field is negligible. Hence, Q_S–Q_D increases rapidly resulting a high subthreshold g_m (Fig. 6(a)). Similarly, with an increase in L_{hk}, the reverse gate-to-drain field plays a significant role, which further reduces the Q_D. As a result, g_m increases with increase in L_{hk} in subthreshold region and shows maximum for D2 device case (L_{lk}:L_{hk}=1:4). But, in superthreshold region (high V_{DS}), the μ term is very high and dominates g_m. Again, increasing L_{hk} in superthreshold region, the Q_D escalates with a unchanged Q_S that reduces Q_S–Q_D term of Eq. (1). However, due to the improved mobility for high L_{hk} devices, there is a minor increment in g_m can be noticed at superthreshold region (Fig. 6(b)).

Fig. 7 (a) illustrates the output conductance (g_d) for conventional and hybrid FinFETs at V_{GS} = 0.7 V. The g_d can be expressed as [26].

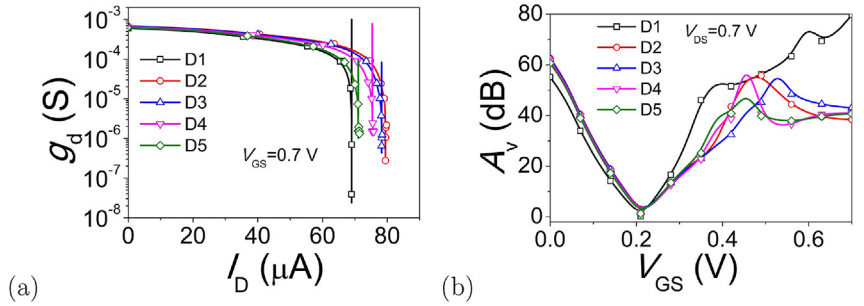

Fig. 7. Analog parameters analyzed among hybrid FinFETs with different L_{lk}:L_{hk} ratios and conventional FinFET (a) Output conductance (g_d) at V_{GS} = 0.7 V (b) gain (g_m/g_d).

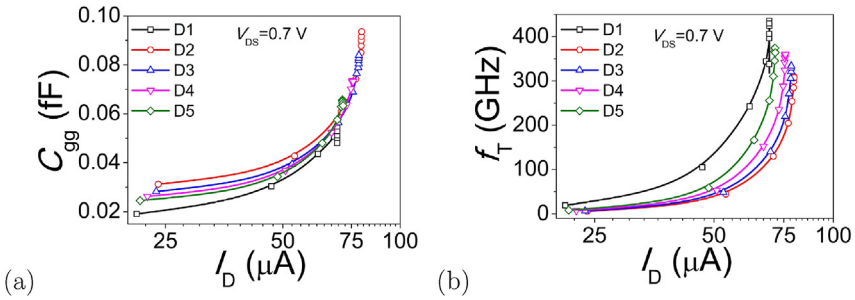

Fig. 8. Comparison of (a) $C_{gg} - I_D$ (b) $f_T - I_D$, among hybrid FinFETs with different L_{lk}:L_{hk} ratios and conventional FinFET at $V_{DS} = 0.7$ V.

$$g_d = \partial I_D / \partial V_{DS} = \left(\mu W \Big/ L_{eff}\right) Q_D \tag{2}$$

The interpretation of above variables are well explained under Eq. (1). From Eq. (2), g_d increases proportionately with Q_D. In earlier analogy under Fig. 6(b), we have perceived that Q_D plays a significant role in superthreshold region (high V_{DS}) and become the dominating factor for high L_{hk} devices. So, it is observed from Fig. 7(a) that with increase in L_{hk}, the gate induced fringing field increases, which further enhances the Q_D and increases the g_d in superthreshold region. However, there is a reverse effect in subthreshold region *i.e.*, g_d decreases with increase in L_{hk} as Q_D remains constant at subthreshold region. For analog performances, the gain ($A_V = g_m/g_d$) of the device is an important figure of merits (FOMs) that is analyzed in Fig. 7(b). From Fig. 7(b), in subthreshold region, A_V is dominated by g_m as a result, A_V increases with increase in L_{hk} that is due to higher g_m as discussed in Fig. 6. And just a reverse phenomena is noticed in the superthreshold region. This is because of the g_d factor as argued in Fig. 7(a).

The variation of total gate capacitance (C_{gg}), and cutoff frequency ($f_T = g_m/(2\pi C_{gg})$) with respect to I_D for conventional FinFET and different architectures of hybrid FinFETs are shown in Fig. 8(a) and (b) respectively. It is seen that C_{gg} increases with the increase in I_D, and the increment is higher for larger L_{hk} hybrid FinFETs because of the advancement in the gate side wall developed fringing field lines. So, C_{gg} increases whereas g_m is almost constant for hybrid devices in the superthreshold region as shown in Fig. 6(b). Hence, the increase in C_{gg} dominates the f_T for the proposed devices consequently a decline in f_T is observed in case of hybrid devices as demonstrated in Fig. 8(b).

5. Conclusion

This paper illustrates the benefits and drawbacks of hybrid FinFETs (UTB + FinFET + Spacer engineering) with compare to conventional FinFETs for subsequent technology nodes. The impact of dual-*k* spacers (inner high-*k* (HfO_2) and outer low-*k* (Si_3N_4)) in improving the performances of the hybrid devices have been analyzed. The proposed device with an optimal high-*k* spacer length (L_{hk}) can be efficiently reduce the *SS* and I_{off} with an improved I_{on}. The D2 topology *i.e.*, hybrid FinFET with L_{lk}:L_{hk} = 1:4 exhibits superior electrostatic integrity in both I_{on} and I_{off}, which in turn enhance the overall device performance. Nonetheless, D2 architecture shows a **1.23x** improvement in I_{on}, and around 60% reduction in I_{off} as compared to SOI FinFET that is required for high speed, and low power consumption applications. We have also demonstrated the influence of L_{lk}:L_{hk} ratios on various analog/RF FOMs like g_m, A_V, and f_T in both subthreshold and superthreshold region of operations. From the presented outcomes, it is concluded that the hybrid FinFETs with higher L_{lk}:L_{hk} ratios are outperformed as compared to conventional FinFET with regard to I_{off}, I_{on} and g_m. However, the primary drawbacks of these structures are the higher C_{gg} that further pay the cost as a poor f_T.

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