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Denise Maria de Andrade

MICROFABRICATION AND CHARACTERIZATION OF VERTICAL ORGANIC FIELD-EFFECT TRANSISTORS BASED ON ROLLED-UP DRAIN ELECTRODE

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MICROFABRICATION AND CHARACTERIZATION OF VERTICAL ORGANIC FIELD-EFFECT TRANSISTORS BASED ON ROLLED-UP DRAIN ELECTRODE

Dissertation submitted to the Graduate Program in Science and Technology of Materials (POSMAT) from Sao Paulo State University (UNESP) in partial fulfillment of the requirements for the Master's degree in Science and Technology of Materials. Supervisor: Prof. Dr. Carlos Cesar Bof Bufon.

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To my parents, Paulo and Elise,

for always supporting me.

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"With men you're expected to do well and get the support, but for females, you have to sacrifice something in a different way from men... I think it's very important for other woman to see that I have had success." — May-Britt Moser, Psychologist and Neuroscientist

RESUMO

Nas últimas décadas têm sido observada uma crescente tendência de estudo e desenvolvimento de transistores de efeito de campo orgânicos, os OFETs (acrônimo em inglês para *organic field-effect transistors*), para aplicações nas mais diversas áreas. Dispositivos eletrônicos orgânicos surgiram como um fenômeno tecnológico por conta de suas propriedades inerentes, tais como flexibilidade e deformabilidade, além do grande potencial da compatibilidade com materiais biológicos. Contudo, apresentam elevadas tensões de operação em comparação a dispositivos inorgânicos. Este problema foi contornado por meio de uma mudança na arquitetura: um arranjo vertical de todas as camadas que compõem o dispositivo, o que leva a formação do canal de condução ao longo da espessura da camada ativa do transistor. Este dispositivo foi denominado como transistor de efeito de campo orgânico com arquitetura vertical ou VOFET (acrônimo em inglês para *vertical organic field-effect transistors*). Apesar de isto garantir baixo consumo de energia, ainda existem alguns aspectos limitantes, como por exemplo o efeito de blindagem do eletrodo da fonte e a deposição de filmes metálicos sobre camadas orgânicas ultra-finas. Recentemente, o conceito de VOFETs foi ampliado pelo desenvolvimento de uma nova plataforma que utiliza nanomembranas enroladas para formar o eletrodo de dreno desses transistores, os VOFETs baseados em nanomembranas enroladas ou r-VOFETs (acrônimo em inglês para *rolled-up nanomembrane based VOFET*). Esta proposta permite a fabricação de transistores com canais de condução ultrafinos e emprega um eletrodo de fonte com perfurações retangulares definidas por meio de litografia óptica e deposição de filmes finos. Com isso em mente, neste trabalho, propõem-se novas estratégias para aprimorar o desempenho da plataforma do r-VOFET e investigar mais a fundo o seu princípio de operação. Foram obtidos resultados consistentes com trabalhos anteriores, os dipositivos apresentaram baixas tensões de operação (<-5 V) e melhora na faixa da razão *on/off* (~10^4-10^5). Em contraste com o mecanismo

de operação sugerido, nenhuma evidência de uma dependência linear entre o número de bordas do eletrodo de fonte e a corrente de saída (o denominado "efeito de bordas") foi observada. Constatou-se que a permeabilidade ao campo elétrico do *gate* do eletrodo de fonte (medido pelo "Fator de Preenchimento", *FF*) desempenha a maior influência sobre a modulação da corrente. Portanto, com o intuito de explorar a promissora combinação de canal de condução ultracurto e a facilidade de interação entre estímulos externos e a camada ativa do dispositivo, investigou-se a possibilidade de aplicação da plataforma r-VOFET como fototransistor. Os resultados obtidos foram impressionantes, tal como alta fotosensibilidade (~10^4) e rápido tempo de resposta (~8,2 s), demonstrando grande potencial para tecnologias de sensoriamento.

Palavras-chave: transistor, litografia óptica, semicondutor orgânico, nanomembrana enrolada, fototransistor.

ABSTRACT

The past decade has seen a growing trend toward the investigation and development of organic field-effect transistors (OFETs) for several applications. Organic electronics have emerged as a phenomenon because of their inherent features such as flexibility and stretchability, in addition to the great potential to interface with biological systems. However, one of the main obstacles is the high operating voltages compared to inorganic counterparts. Such a problem was addressed by a change in the architecture design, a vertical stacking of the device layers and the formation of the conducting channel along the transistor's active layer thickness. This device was named VOFET (vertical organic field-effect transistor). Although the approach guarantees lower power consumption, this architecture still has some limiting factors, including the source electrode screening effect and metal deposition on top of ultra-thin organic layers. Recently, a novel architecture that involves the preparation of drain electrode by rolling-up metallic nanomembranes has expanded the VOFET concept. The rolled-up nanomembrane-based VOFET (r-VOFET) allows the incorporation of ultra-thin organic semiconductor layers and employs a patterned source electrode defined by photolithography and thin-film deposition. Accordingly, in this work, we proposed new strategies to improve the performance and investigate the operating principle of the r-VOFET platform. Our findings are consistent with previous studies, our devices exhibited low operating voltages (<-5 V) and enhanced *on/off* ratio (~10^4-10^5). In contrast to the operating mechanism suggested, there was no evidence of a linear dependence between the number of source-electrode edges and the output current (the so-called "edge-driven mechanism"). We discovered that the source electrode permeability to the gate electric field (measured by the "Fill Factor" value, *FF*) plays a major role in current modulation. Finally, to explore the promising combination of ultra-short conducting channel and facilitated external stimuli with the device's active layer, we conducted a study about the

application of the r-VOFET platform as a phototransistor. We observed impressive results, such as high photosensitivity (~10^5) and fast response time (~8.2 s), thus demonstrating great potential for sensing technologies.

Keywords: transistor, photolithography, organic semiconductor, rolled-up nanomembrane, phototransistor.

LIST OF ABBREVIATIONS AND SYMBOLS

2D – Two-dimensional

3D – Tridimensional

A – Area

A - Ampere

AFM – Atomic Force Microscopy

ALD – Atomic layer deposition

Al_2O_3 – Aluminum oxide

Au – Gold

C – Carbon atom

CdSe – Cadmium selenide

CF_4 – Tetrafluoromethane

C_{ins} – Capacitance per area

CL – Contact Limited

CLS – Confocal laser scanning

cm – Centimeter

Cr – Chromium

CuPc – Copper-phthalocyanine

C_{60} – Fullerene

D – Drain electrode

DNTT – Dinaphtho[2,3-b:2′,3,-f]thieno[3,2 -b]thiophene

DPA – 2,6-diphenyl anthracene

E – Electric field

E_g – Forbidden energy gap

EL – Electroluminescence

*e*V – Electron volt

$E_\perp$ – Electric field perpendicular to the interface

FET – Field-effect transistor

FF – Fill Factor

G – Gate electrode

GaAs – Gallium arsenide

g_D – Conductance

g_m – Transconductance

Ge – Germanium

GeO_x – Germanium oxide

HF – Hydrogen fluoride

HMDS – Hexamethyldisilazane

HOMO – Highest occupied molecular orbital

H_2O – Water

H_2O_2 – Hydrogen peroxide

I_{DS} – Electric current between S and D electrodes

I_{ON} – Transistor output current at on state

I_{OFF} – Transistor output current at off state

J – Current density

k – Boltzmann constant

L – Transistor conducting channel length

L_P – Source-electrode perforation length

L_S – Source-electrode stripe length

LED – Light-emitting diode

LUMO – Lowest unoccupied molecular orbital

NM – Nanomembrane

n_{SE} – Number of source edges

n_P – Number of source perforations

NW – Nanowire

N_0 – Density of states

N_2 – Nitrogen gas

OFET – Organic Field-Effect Transistor

OH^- – Hydroxyl groups

OLED – Organic light-emitting devices

OPBT – Organic permeable base transistor

OPT – Organic phototransistor

OSC – Organic semiconductor

OSIT – Organic static induction transistor

OTFT – Organic Thin-Film Transistor

P – Photosensitivity

PCDTPT – Poly[1,2,5]thiadiazolo[3,4-c]pyridine-4,7-diyl(4,4-dihexadecyl-4H-clopenta[2,1-b:3,4-b0]dithiophene-2,6-diyl)[1,2,5]thiadiazolo[3,4-c]pyridine-7,4-diyl(4,4-dihexadecyl-4H-cyclopenta[2,1-b:3,4-b0]dithiophene-2,6-diyl)

$PC_{61}BM$ – [6,6]-phenylC_{61} butyric acid methyl ester

PDVT-8 – poly[2,5-bis(alkyl)pyrrolo[3,4-c]-pyrrole-1,4(2H,5H)-dione-alt-5,5′-di(thiophen-2-yl)-2,2′-(E)-2-(2-(thiophen-2-yl)vinyl)-thiophene]

PE – Patterned electrode

PE-VOFET – Patterned-electrode vertical organic field-effect transistor

PLED – OLEDs incorporating conjugated polymers

PMMA – Poly(methyl methacrylate)

P(NDI2OD-T2) – poly{[N,N′-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5'-(2,29-bithiophene)}

PS – Polystyrene

q – Elementary charge

Q – Charge

QD – Quantum dots

R – Photoresponsivity

r-VOFET – Rolled-up nanomembrane-based vertical organic field-effect transistor

S – Source electrode

S – Sub-threshold swing

SAM – Self-assembled monolayer

SB-VOFET – Schottky barrier vertical organic field-effect transistor

SCLC – Space-charge limited current

SEM – Scanning Electron Microscopy

Si – Silicon

SiO_2 – Silicon oxide

T – Temperature

Ti – Titanium

t_{int} – Integration time

TMA – Trimethylaluminum

TMDs – Transition metal dichalcogenides

UV – Ultraviolet

V – Voltage bias

V_D – Drain voltage bias

V_{DS} – Voltage applied between S and D electrodes

V_G – Gate voltage bias

V_{GS} – Voltage applied between S and G electrodes

VLSI – Very Large Scale Integration

VOFET – Vertical Organic Field-Effect Transistor

V_{th} – Threshold voltage

W – Watt

W – Transistor conducting channel width

W_F – Work function

ZnS – Zinc Sulfate

Ω – Ohm

φ_b – Energetic potential barrier

Φ_B – Carrier injection barrier

μ – Charge-carrier mobility

μ_{lin} – Linear-regime mobility

μ_{sat} – Saturation-regime mobility

μ_{FET} – Field-effect mobility

μ_n – Electron mobility

ε – Vacuum permittivity

ε_0 – Relative permittivity

ε_r – Dielectric constant or relative permittivity

τ – Time constant

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1. INTRODUCTION

The use of field-effect transistors (FETs) in electronic circuits has become more and more popular since their pioneering proposition by Julius Edgar Lilienfeld in 1930 [1]. The FET's simple architecture was an advantage itself, with the requirement of only one type of semiconductor that does not need to be doped, unlike bipolar transistors. Accordingly, FETs are three-terminal devices, in which an electric field controls the electrical behavior causing signal amplification and switching functions. The principle of FET operation is based on the current established between two of the terminals, *viz*. source (S) and drain (D), whereas the third terminal, gate (G), controls the device current amplitude by the applied bias [2–4].

During the 1980s, organic materials such as polymers and semiconductor molecules began to be processed in the form of thin films [5–7]. A few years later, the fabrication of organic/inorganic hybrid electronic components became possible, providing the properties and high versatility of organic materials to electronics [3]. Within this frame, organic field-effect transistors (OFETs) emerged as a key enabling technology wherein features such as flexibility, lightweight, and low production cost are possible [8,9]. Compared to conventional FETs, the performance of organic semiconductors (OSCs) is inferior to that of inorganic semiconductors. However, OFETs are promising due to their easy fabrication – the device's layers can be deposited and patterned at room temperature involving a combination of low-cost solution-processing and direct-write printing –, which affords their great potential for the field of flexible and large-area electronics [3,4].

In the last years, considerable literature has grown up around the performance of OFETs. This progress has been achieved using high-mobility OSCs [10–14] and materials with high dielectric constant (κ, kappa) [15–19], and it is also related to addressing the architecture design and processing methods. However, a key issue of the planar architecture is attributed to

the high operating voltages and low output current compared to inorganic counterparts. This problem is associated with the complexity to achieve nanometric lateral structuring, consequently the relatively large conducting channels impact greatly the OFET performance. A simple and effective solution was the vertical architecture (VOFETs), which involves a vertical stacking of the device layers and the formation of the conducting channel along the OSC thin film thickness. Since traditional deposition methods allow reliable and precise control over thin film thickness, several VOFETs with ultra-short channels have been reported lately [20–25].

There are, however, identifiable shortcomings with metal deposition over organic thin films such as morphology modification and channel length shortening that can occur due to metal diffusion [26–28]. With that in mind, in 2020, we proposed the rolled-up nanomembrane-based VOFET (r-VOFET), a platform that implements the enormous technological potential of the vertical architecture with the outstanding approach of hybrid metal/OSC/metal contact employing nanomembranes as electrodes [21]. The deterministic self-rolling nanomembrane ensures a soft and reliable electrical contact between metal and organic thin film with a thickness of a few nanometers, hence the r-VOFET has the shortest conducting channel reported in the literature.

Overall, we have summarized in Figure 1, the key developments for the OFET platform to give a comprehensive big picture of the important role occupied by the vertical architecture in addressing some issues of the traditional planar architecture, and therefore, expanding the potential applications for organic transistors. We start from the first FET device in the 1930s to the more recent concept, the r-VOFET, which is the main topic of this work.

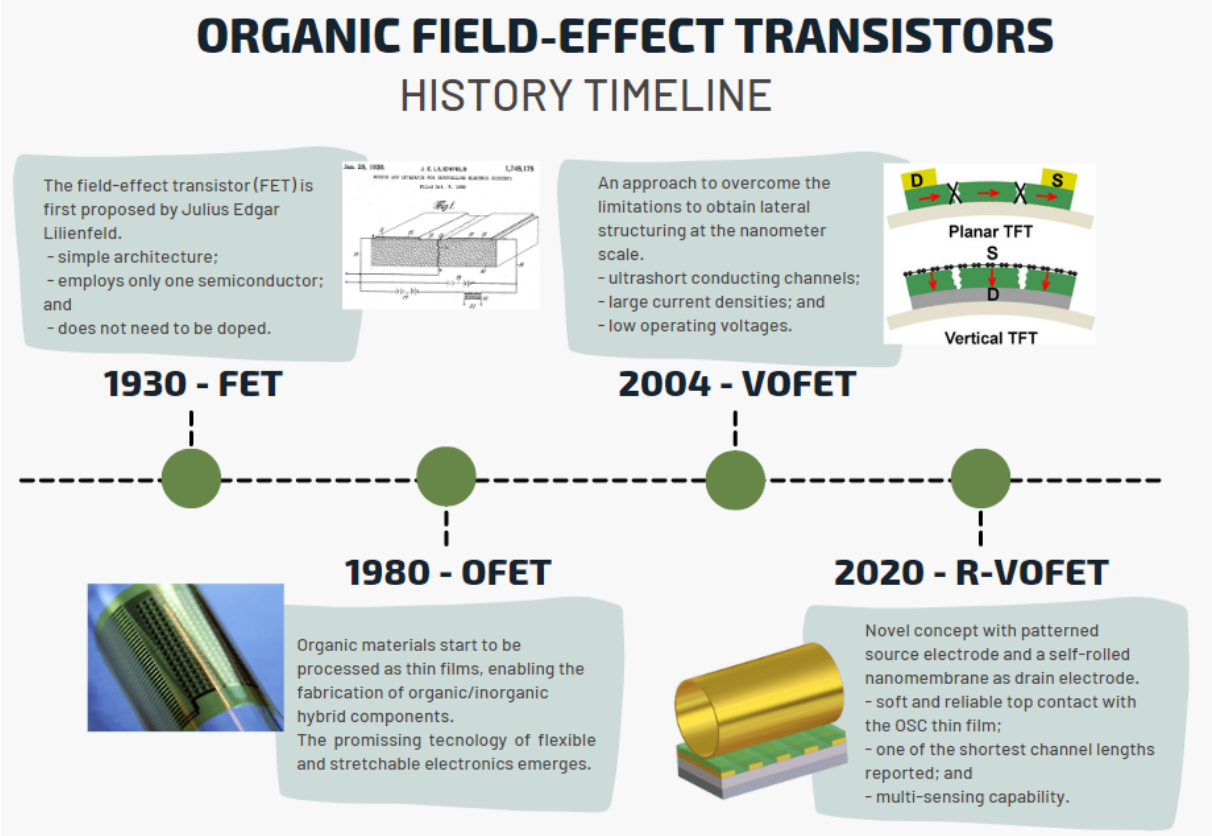


Figure 1. Timeline showing key developments for the OFET platform. Adapted from ref.: [1,22,29,30].

Despite the r-VOFET's remarkable findings, it still suffers from inferior performance when compared to high-performance transistors (*viz.* relatively low *on/off* ratio, high gate-leakage current, and significant hysteresis). Therefore, in this work, we aimed to expand on the results of our previous study by improving the r-VOFET platform's performance and reproducibility through engineering approaches. We also highlight that processing the devices entirely employing photolithography-assisted patterning effectively allowed a more careful control over the patterned structures to study closely the effects caused by changes in the electrode geometry and choice of materials. Specifically, we intended to:

- To obtain improved r-VOFETs employing microfabrication techniques and to define the rectangular-perforated source electrode employing photolithography-assisted patterning;

- To optimize the fabrication process, thereby enhancing performance by architecture modifications and allowing a more reliable extraction of important device parameters and to study the operating mechanism;
- To systematically study the edge-driven operating taking both n_{SE} and the Fill Factor value (*FF*) into account, so it would be possible to assess more information about the source electrode;
- To estimate r-VOFET performance parameters and compare with transistors in the literature (*i.e.*, saturation, threshold voltage, I_{ON}/I_{OFF} ratio, gate leakage); and
- To investigate the r-VOFET platform's potential when applied as a phototransistor.

2. THEORY AND BACKGROUND

Low-power and low-voltage operation are fundamental features for devices to be compatible with modern electronics. On account of this statement, the VOFET concept has emerged as a powerful platform to outperform its traditional counterparts [4,31,32]. As illustrated in Figure 2, in contrast to planar architectures that show conducting channel lengths (L) up to hundreds of micrometers, the nanoscaled channel lengths of VOFETs offer a possible way towards overcoming the inherent OSC's low mobility and facilitate high current densities with low power consumption. Additionally, the simple vertical architecture allows the use of low-cost and less complex fabrication processes, thus offering great potential for large-area and high-performance organic electronics.

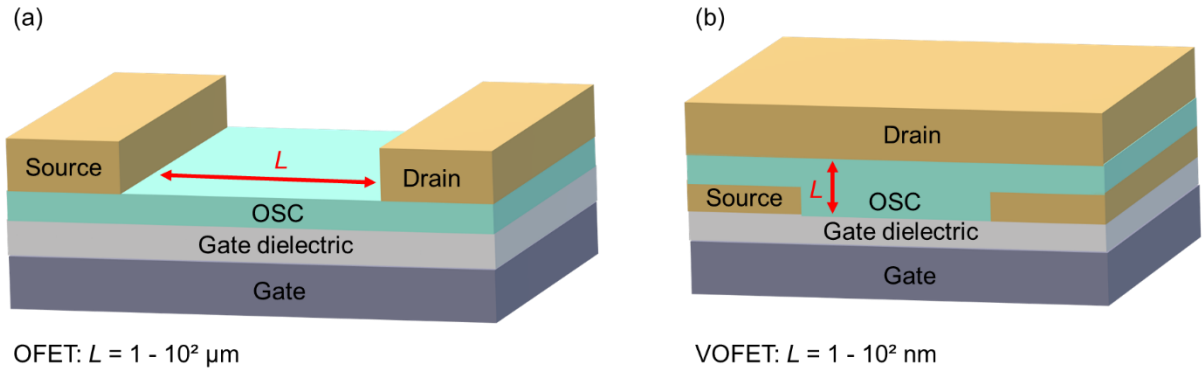


Figure 2. Schematic illustrations comparing the device layer arrangement and conducting channel length (L) of the planar OFET (a) and the VOFET (b) architectures.

On the question of flexible electronics, organic devices attract considerable interest due to their mechanical properties and processing conditions that allow them to be fabricated on flexible substrates such as polymers. Another advantage of the VOFET platform is that in-plane cracks in the OSC layer formed during repeated bending cycles show little to no effect on the formation of the vertical conducting channel along the OSC layer thickness. Therefore,

the out-of-plane current flow ensures that device operation is preserved and overcomes the critical bending limitation observed for planar OFETs and inorganic transistors [29,33].

Furthermore, in the ascending field of organic electronics, the VOFET has a pivotal role in allowing the combination of low-cost processing and batch fabrication with a simple architecture design and fundamental features essential for a wide range of technologies. Thus, novel-engineering strategies to improve device performance and the exploration of new strategies for comprehensive control of the operation are of crucial importance to realizing novel high-performance devices. Hence, for further contextualization about the topic, this chapter is divided into the following sections: Section 2.1 introduces the basic background of organic semiconductors, molecular orbital theory, and charge transport mechanisms; Section 2.2, we discuss the theory and operation of the OFET platform; Section 2.3 describes the VOFET platform architecture, types, and operating mechanism; and finally, Section 2.4 comprises about phototransistors, a potential application for VOFETs.

2.1. ORGANIC SEMICONDUCTORS

Organic semiconductors (OSC) have been extensively studied because of their unique electronic properties combined with the chemical and mechanical benefits observed for organic compounds. Additionally, due to their ability to be fabricated with low-temperature processing techniques onto flexible substrates, which facilitates low-cost and more versatile fabrication methods, OSCs are attractive candidates for applications in devices such as solar cells [34–36], field-effect transistors (OFETs) [37,38], stretchable electronics [39], and lasers [40].

Organic materials are composed mostly of carbon (C) and hydrogen (H) atoms, with a few heteroatoms such as sulfur (S), oxygen (O), and nitrogen (N). For a long time, they had been considered to have low electrical conductivity [3]. However, the discovery of

semiconducting behavior in organic compounds created a new and fascinating field of research. Since the first report on organic electroluminescence (EL) cells by Bernanose *et al*. in 1953 [6], and by Pope and coworkers in 1963 [7], OSC attracted tremendous attention and encouraged rapid growth of this field of research [3].

Currently, great attention has been directed toward the technology of organic light-emitting devices (OLEDs). Initially, the single-crystal-based OLEDs were thick and required excessive-high operating voltages (above 400 V) [7]. In 1989, Tang and Van Slyke developed more efficient EL devices, LEDs based on amorphous organic thin films showing operating voltages lower than 10 V [5]. In 1990, Burroughes *et al.* reported the first approach of OLEDs incorporating conjugated polymers (PLEDs) [41]. They demonstrated easily processed devices with robust structures and reasonably efficient operation. Overall, many new technologies were proposed such as new materials and device architectures, establishing a prosperous growing field [3,42].

It is possible to classify organic semiconductors into two major classes: molecular and polymeric materials. Molecular organic semiconductors are small molecules, in general, with a non-repeating structure, whereas polymeric organic semiconductors consist of linked chains of repeating small subunits (monomers). Crystalline films and layers of small molecules can be deposited under vacuum, while not requiring high-temperature or high-purity processing methods [3]. On the other hand, polymers are often solution processed because they are more soluble than small molecules in common solvents, which allows the use of simple and low-cost deposition techniques, such as spin-coating and large-scale industrial coating [3,43].

The semiconducting nature of commonly studied polymers and small molecules is usually associated with a backbone of conjugated bonds – *i.e.*, unsaturated structures showing alternating single and double bonds [3,43,44]. The conjugated structure is essential for charge

conduction due to lower energy levels related to π-bonds [3,43]. A few examples of the two classes of organic semiconductors can be found in Figure 3.

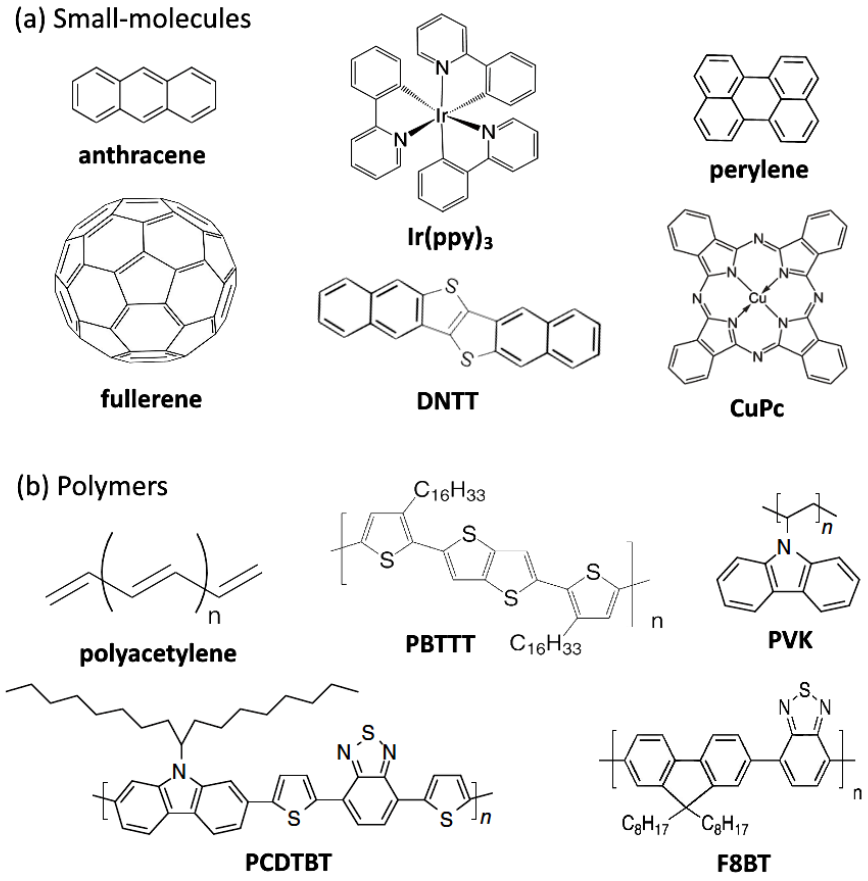


Figure 3. Examples of chemical structures of π-conjugated molecules for the two classes of organic semiconductors: (a) small molecules and (b) polymers. Adapted from ref.: [3,43].

A neutral C atom has six electrons: two electrons in a 1s orbital, two electrons in a 2s orbital, and two in 2p orbitals (as shown in the schematic representation of valence atomic orbitals in Figure 4a). When a binding atom approaches this neutral C, the 2s and 2p orbitals combine forming new hybrid orbitals $2sp^2$ (in the case of a conjugated system). Therefore, a single-bond configuration is formed of only one conventional σ-bond, which is formed by the sp^2 hybrid orbitals and has fully paired electrons in their bonding states (σ) and empty antibonding (σ*) states. This leads to strong, stable, and highly directional carbon chains. On the other hand, the double-bond configuration is formed by one σ and two π-bonds. The

remaining half-filled p_z orbitals are responsible for forming the π-bonds (Figure 4b). In this case, $2p_z$ orbitals are hybridized resulting in weaker π or π* orbitals, allowing that charge transfer can occur through the delocalized π/π*-states of the conjugated system. The weaker splitting of π and π*-orbitals has more favorable (lower) energy levels than the σ-σ* transition of the C–C bond as shown in the diagram of energy levels in Figure 4c [3,43].

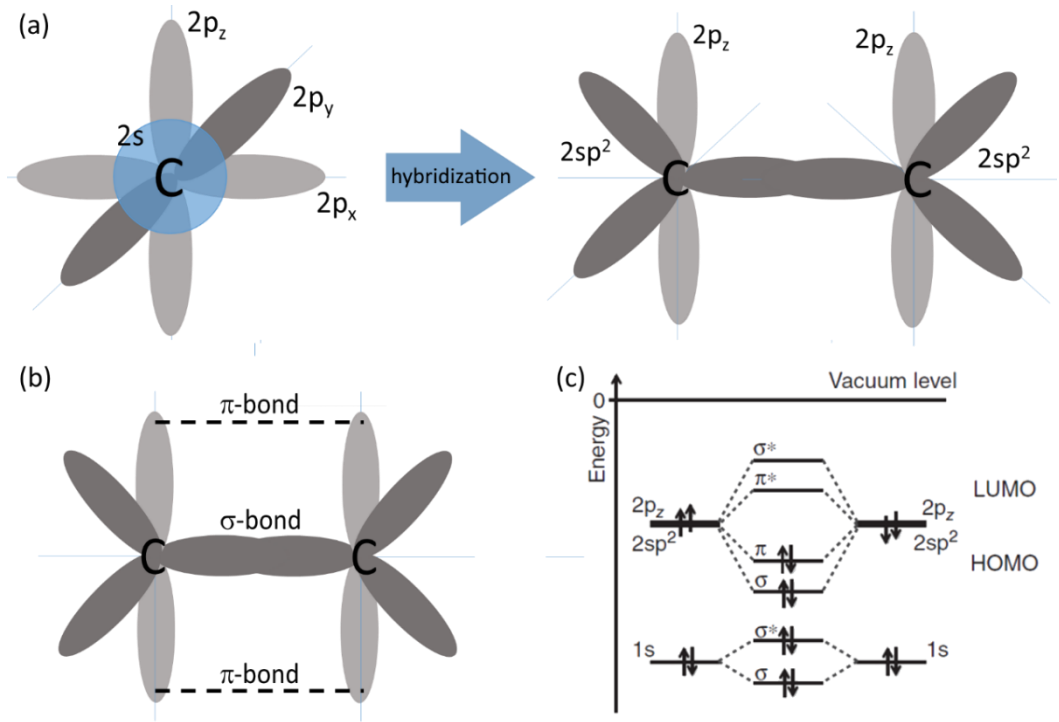


Figure 4. Schematic representation of hybridization and bonding of a carbon atom. (a) Valence atomic orbital of a neutral C atom and its hybridization in sp^2 molecular orbitals after the combination with another binding atom. (b) Representation of a double bonding structure. (c) Simple diagram illustrating the energy levels of the formation of σ and π bonds from atomic orbitals, and molecular orbitals such as HOMO and LUMO as well. Only orbitals involved in the carbon-carbon interaction are shown. Adapted from ref.: [3].

In a molecule, the multiple atoms and their atomic orbitals interact resulting in molecular orbitals. The lower-energy and the higher-energy orbital are called the highest occupied molecular orbital (HOMO) level and the lowest unoccupied molecular orbital (LUMO) level, respectively [3]. In a conjugated system, the two unpaired $2p_z$ electrons will tend to occupy the two spin-allowed π states, leaving the unoccupied π* states above a forbidden energy gap E_g (this energy separates HOMO and LUMO levels). Therefore, when the injection

of electrons occurs, electrons will go into the empty orbital at the LUMO energy. Similarly, the injection of holes corresponds to taking electrons out of the HOMO energy and subsequently placing them in the electrode. Whether electron or hole injection can occur depending on the OSC molecular orbital levels, similar to the inorganic semiconductor band gap energy [3,44].

Typical properties of OSCs are absorption and emission of light in the visible spectral range, and a degree of conductivity that is suitable for classical semiconducting devices (LEDs, FETs, and solar cells). However, this semiconducting behavior differs completely from the one observed in inorganic materials [3]. Inorganic semiconductors have narrow band gaps (0.67 eV for germanium, 1.1 eV for silicon, and 1.4 eV for GaAs), intrinsic conductivities ranging around 10^{-8} to 10^{-2} $\Omega^{-1}cm^{-1}$, and at room temperature, free charges can be created by thermal excitation from a valence band to a conduction band. Also, the dielectric constant (k or ε_r), which is the macroscopic equivalent to the atomic or molecular polarization, has values as large as $\varepsilon_r = 11$ [3,45]. On the other hand, organic semiconductors are formed by weak van der Waals interactions between molecules, exhibiting a wide bandgap around 1.5-3 eV (limited by HOMO and LUMO levels) [46], and a distinct charge transport mechanism [3,47]. Their conductivity is extrinsic and charge carriers must be injected from electrodes or generated by photoexcitation. Furthermore, OSC exhibits low dielectric constants (≈ 3), thus interactions between free charge carriers are substantial and cannot be ignored [3].

The transport mechanisms in OSCs are usually explained by a cross-over between band and hopping transport of charge carriers. In the band transport, at low temperatures (close to 0 K), an electron in a LUMO donor site will move to an empty LUMO accepting site (the same happens with holes at the HOMO level). This charge transfer occurs at constant mobility due to a sequence of collisions (*i.e.*, scattering at structural defects since organic molecules typically exhibit no long-range order). In addition, with increasing temperature, vibrations of the lattice will increase charge carrier scattering. However, as long as the scattering process is

only a weak perturbation, including all intra- and intermolecular vibrations, charge transport can still be described in terms of a band model [3,48].

In the context where the band concept cannot describe the transport (*i.e.*, high temperatures), the charge flow mechanism is attributed to intra-molecular charge diffusion and inter-molecular charge hopping. In hopping transport, a charge carrier is localized at individual sites and transport takes place via charges jumping from site to site [49,50]. The probability of each hop depends on the site energy, the hopping distance, the temperature, and the electronic disorder since each inter-molecular hop requires significant reorganization energy with a polarization effect [3,48–51].

2.2. THEORY AND OPERATION OF ORGANIC FIELD-EFFECT TRANSISTORS

OFET is a three-terminal device that uses a third electrode (gate) to control the electrical current through an OSC layer localized between the other two electrodes (source and drain). As a regular electronic device, OFETs have features such as controlling conductance and output current amplification (10^6 - 10^8) [3,47,48,52,53]. It is also possible to study the OSC properties such as charge-carrier mobility and transport characteristics [44,48,52].

Two common OFET architectures are shown in Figure 5, they are called (a) bottom and (b) top contact configurations. In the bottom contact configuration, the source/drain electrodes are in direct contact with the insulator, while in the top contact configuration, the source/drain electrodes are stacked over the OSC. In normal practice, bottom-gated architectures are more commonly used because this configuration avoids metal and gate dielectric deposition steps over the organic layer [54].

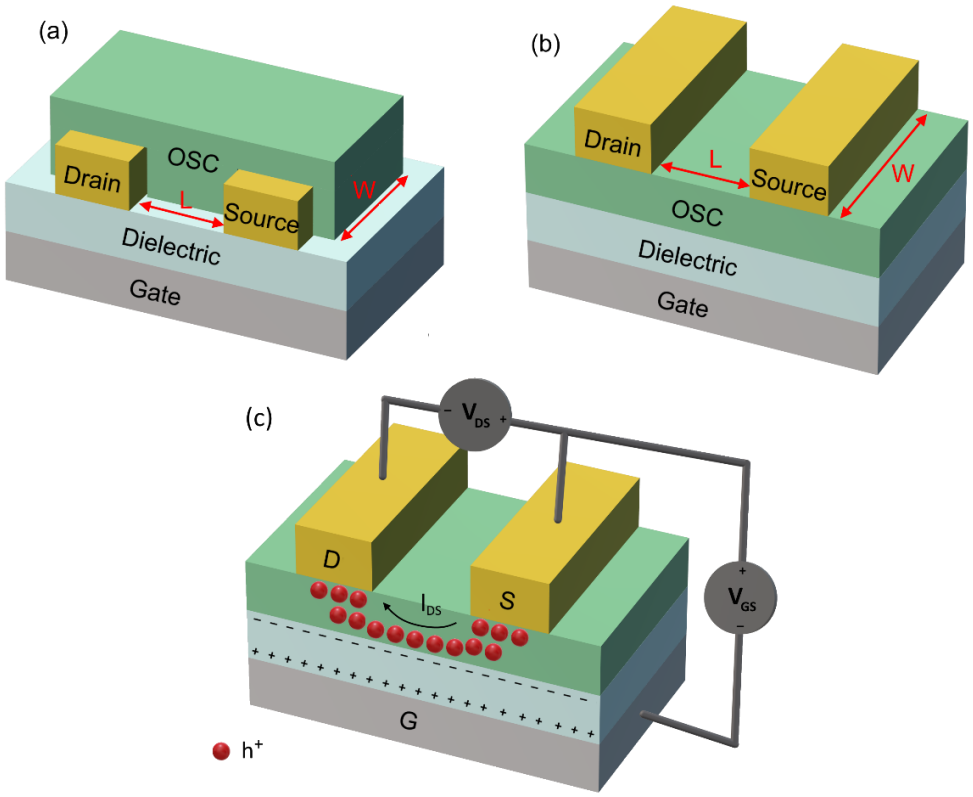


Figure 5. Schematic illustrations of OFET architecture and operation. (a) OFET with a bottom contact configuration and (b) a top contact configuration. *W* and *L* are the conducting channel dimensions of the transistor (width and length respectively). (c) The OFET operation is illustrated by the formation of a conducting channel in the vicinity of the OSC/dielectric interface under bias application. The OSC considered here is p-type, hence holes (h^+) are the majority charge carriers.

As illustrated in Figure 5c, the device operation depends on the application of two potentials at the same time: at the gate electrode (V_{GS}) and at the drain electrode (V_{DS}), with the source electrode held at ground. When V_{GS} is applied, the device behavior is a lot similar to a planar capacitor: a high charge density is created next to the dielectric interface. Thus, it generates an accumulation of opposite carriers in the OSC layer adjacent to the dielectric layer, which changes the channel conductance. Consequently, when V_{DS} is applied, charge carriers are easily injected into the conducting channel and are pulled in the direction of the drain electrode, where the drain current (I_{DS}) is measured. Thereby, I_{DS} modulation occurs depending on the magnitude of the gate electric field applied [2,4,54].

Figure 6a shows the output characteristics curves measured for a close-to-ideal OFET. The output curves study the evolution of I_{DS} *vs.* V_{DS}, where each curve is measured at a fixed V_{GS} value. This measurement allows identifying two regimes of operation: linear and saturation regimes. An explanation for this is the distribution of charge carrier accumulation along the OFET conducting channel [2,54]. To help understand it, Figures 6b-d illustrate the charge carrier density distribution for each case.

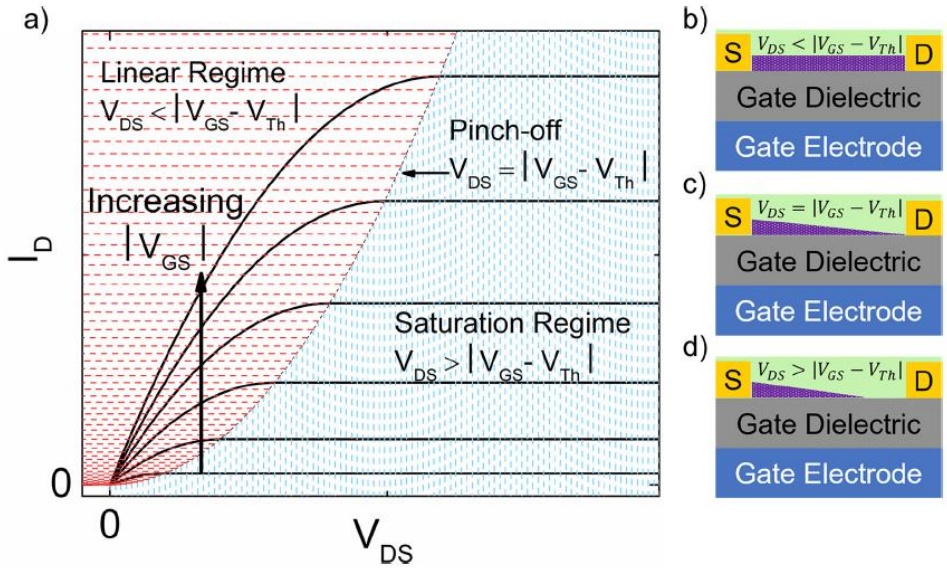


Figure 6. Representation of OFET output characteristics regimes. (a) Output characteristics curves observed for close-to-ideal OFETs. Evolution of I_{DS} in relation to increasing V_{DS}, where each curve is measured at a fixed V_{GS} value. The dashed line separating the red and blue regions depicts the transition from linear to saturation regime. (b-d) OFET representations showing the charge density in the conducting channel in purple: (b) in the linear regime, (c) at pinch-off, and (d) in the saturation regime. Adapted from ref.: [54].

When $|V_{DS}| < |V_{GS}-V_{th}|$ (where V_{th} is the threshold voltage), the OFET operates in a linear regime, in which the device acts as a V_{GS}-controlled resistor. In this scenario, I_{DS} has a linear relation with V_{DS} and depends on V_{GS} (*i.e.*, with higher V_{GS} there is an increase in the charge carrier density accumulated along the channel, and thus, a decrease in resistivity). Then, as assumed in Figure 6b, as long as V_{DS} is lower or close to V_{GS}, the decrease of charge density across the channel is relatively small, and it is possible to approximate the charge density as uniform [2,53,54].

In the case that $|V_{DS}| = |V_{GS}\text{-}V_{th}|$, the quasi-uniformity of charge density across the conducting channel is lost. Consequently, a considerable reduction of free charge carriers occurs at the region near the drain electrode, whereas the channel becomes "pinched off", as shown in Figure 6c. The real charge density at the OSC/dielectric interface is now a sum of remaining charges at $V_{GS} = 0$ and charges induced by an external voltage: $Q = CV_{GS} - CV_{th} = C(V_{GS} - V_{th})$, where Q is the charge, V is the bias applied, and C_{ins} is the capacitance per area of the gate insulator. Therefore, when $|V_{DS}|$ approaches $|V_{GS}\text{-}V_{th}|$: $Q_D = C[V_D - (V_G - V_{th})] < C[V_S - (V_G - V_{th})] = Q_S$. Thus, the charge density near the drain electrode is reduced and the resistivity of the conducting channel is enhanced, causing a reduction in the slope of the I_{DS} *vs.* V_{DS} curves, which starts to saturate [2,53,54].

Finally, once $|V_{DS}| > |V_{GS}\text{-}V_{th}|$, the OFET operates in the saturation regime. The charge density discontinuity at the conducting channel is larger and there is a substantial increase in resistivity (Figure 6d). In this case, I_{DS} is independent of V_{DS}, *i.e.*, the current is only dependent on the charge-carrier mobility and no longer on the accumulated charge-carrier density at the OSC/dielectric interface. Therefore, I_{DS} results from a space-charge limited current that flows across the conducting channel as the applied electric field forces the injected charge carriers to the drain electrode. [2,53,54].

The performance of an OFET can be quantified by assessing some important parameters extracted by assuming the standard Shockley FET equations (*i.e.*, the gradual channel approximation), such as field-effect mobility (μ), V_{th}, conductance (g_D), transconductance (g_m), and sub-threshold swing (S) [53–56]. The Shockley assumptions for a close-to-ideal OFET provide equations that give the drain current in the linear and saturation regimes [2,54,55]:

$$I_{DS_{lin}} = \mu_{lin} \frac{W}{L} C_{ins} \left[(V_{GS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad \text{for} \quad |V_{GS} - V_{th}| \gg V_{DS} \qquad \text{(I)}$$

$$I_{DS_{sat}} = \mu_{sat} \frac{W}{L} C_{ins} (V_{GS} - V_{th})^2 \quad \text{for} \quad |V_{GS} - V_{th}| < V_{DS} \qquad \text{(II)}$$

Where μ_{lin} and μ_{sat} are the linear- and saturation-regime field-effect mobilities, respectively. Mobility is a very important parameter that measures the charge transport in the semiconductor. Additionally, it plays a key role in improving device efficiency, high-performance OFETs often employ OSC with high μ values (above 1 cm²/Vs) [57–60]. Accordingly, proper extraction of mobility from experimental data is essential to ensure the reliability of reported values. To fulfill this requirement, transfer characteristics must show a linear dependence for $I_{DS}(V_{GS})$ in the linear regime (Figure 7a), and for $|I_{DS}|^{1/2}(V_{GS})$ in the saturation regime (Figure 7b) respectively, otherwise parameter extraction is not accurate [53,55].

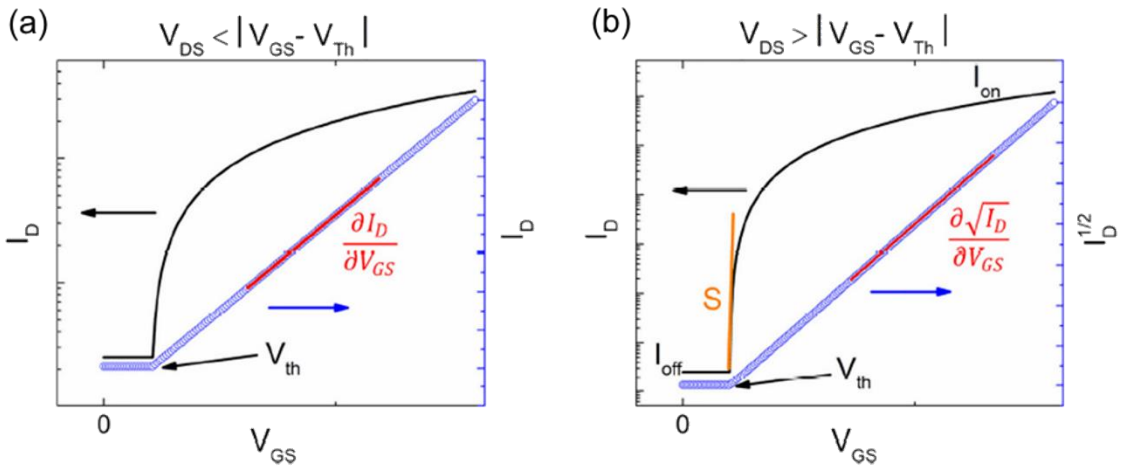


Figure 7. Ideal OFET transfer characteristics: (a) linear regime, and (b) saturation regime. Adapted from ref.: [54].

However, deviation from ideal characteristics of operation is often observed for OFETs, such as nonlinearities, hysteresis, and $V_{th} \neq 0$. These non-idealities might be associated with charge-carrier scattering at bulk and interfacial defects, charge-carrier trapping, short-

channel effects, and high contact resistance [48,54,55]. Also, the mobility values estimated from the saturation-regime linear fit have some drawbacks: charge-carrier mobility is highly dependent on the charge density along the conducting channel; thus, it is not constant in the saturation regime due to the large charge density discontinuity. Therefore, it is strongly recommended to extract the mobility using Equation I for the linear regime [53,55,56].

The FET equation for the saturation regime (Equation II) also yields the value for V_{th}, which can be determined as the intercept of I_{DS} with the V_{GS} axis (*i.e.*, when $I_{DS} = 0$). V_{th} is an additional V_{GS} bias applied to fill shallow and deep traps in the semiconductor and at the semiconductor/dielectric interface, which enables the accumulation of charge carriers, forming the conducting channel [53–56,61,62]. By means of performance and application, V_{th} indicates the operating voltage range, and for a cost-efficient device, it should show a value close to 0 V [54]. Similarly, the sub-threshold swing, *S*, also depends on the charge trap concentration and can be determined employing the following equation [54]:

$$S = \frac{\partial V_{GS}}{\partial(log_{10}(I_{DS}))} \quad \text{(III)}$$

Where it is reported with units of V/dec. *S* measures the V_{GS} value necessary to increase current by an order de magnitude, or in other words, the transistor power consumption to amplify current, *e.g.*, high-performance FETs are often reported with *S* values lower than 1 V/dec [54,56]. Last but not least, the amplification factors are very important performance merit figures, such as the intrinsic gain (g_m/g_D) and the *on*/*off* ratio (I_{ON}/I_{OFF}, where I_{ON} and I_{OFF} are current values at on and off states respectively). Large values (above 10^6) are interesting because the "on" and "off" states are visibly distinguishable, thus indicating a considerable current amplification [54,56,63].

2.3. VERTICAL ORGANIC FIELD-EFFECT TRANSISTORS

Vertical organic field-effect transistors (VOFETs) are an approach to overcome the limitations of traditional planar OFETs. Although the planar architecture has shown a continuous increase in performance and significant advances, it is hard to obtain large current densities and low operating voltages because of their relatively large conducting channel (*i.e.*, *L* around micrometers or even more) [4,31]. The main difficulty in achieving shorter channels typically resides in processing limitations to obtain lateral structuring at the nanometer scale. Using a vertically stacked architecture, *L* is determined by the thickness of the active layer, which can be controlled easily by many extremely precise and reproducible deposition methods, allowing the fabrication of devices with a conducting channel length of a few nanometers [4,31,32].

During recent decades, numerous devices showing vertical architecture have been developed and analyzed extensively, and a growing body of literature has emerged. Triode-like and FET-like structures are two major categories of vertical organic transistors thoroughly investigated [31]. In the triode-like vertical organic transistor, the three electrodes are denominated differently (base, collector, and emitter), there is no insulating material separating the OSC from one of the electrodes, and the intermediate electrode (base) is inserted between the other two electrodes and the OSC. A requirement for the base electrode is that it must be permeable to charge carriers injected into the OSC by the emitter, also, it must control this current by the potential applied, thereby, enhancing the current measured at the collector. This category includes devices such as organic permeable base transistors (OPBTs) and organic static induction transistors (OSITs) [31,32].

Meanwhile, considering device architecture and operation, the FET-like structures are more likely similar to the traditional planar OFETs than the triodes. Two examples of FET-like

architectures are the vertical organic field-effect transistors (VOFETs) and the Schottky barrier vertical organic field-effect transistors (SB-VOFETs). Figures 8a and 8b show examples of two types of step-edge VOFETs. In a step-edge structure, the OSC layer is deposited around a pre-defined edge in a way that the charge carriers injected are transported vertically from the source to the drain electrodes [31,32]. Figure 8a is a representation of a top-gate architecture, the edge was defined by employing an insulating layer separating the source and the drain electrodes. Alternatively, Figure 8b is a bottom-gate step-edge VOFET, the edge was sculpted on the substrate (*e.g.* by etching). In both architectures the entire OSC layer length is in contact with the gate dielectric, thus ensuring I_{DS} modulation when charge carriers accumulate at the OSC/dielectric interface. However, the term vertical organic transistor has been frequently misused in some cases. For example, many of these devices show a pseudo-vertical conducting channel, a combination of lateral and vertical transport, (*i.e.*, the lateral contribution occurs along several micrometers, whereas the vertical contribution occurs along a few nanometers) [31,32].

The FET-like category also includes SB-VOFETs (closely resembling the representation in Figure 8c). SB-VOFETs are generally composed of a vertical arrangement of drain electrode, OSC layer, source electrode, gate dielectric layer, and gate electrode. The key concept adopted in this architecture is that the drain electrode, OSC layer, and source electrode act as a metal-semiconductor-metal Schottky diode, showing very low I_{OFF} caused by the high injection barrier. The operation of an SB-VOFET relies on the modulation of the injection barrier height (*i.e.*, the Schottky barrier) by V_{GS}, hence resulting in variation of the contact resistance at the source/OSC interface rather than the modification of charge carrier densities at the conducting channel. Also, for an effective modulation, a continuous metal source electrode must be avoided therefore it would completely screen the gate field due to its natural shielding [4,31,32]. For meeting this particular requirement some approaches have been

thoroughly employed, for example, perforated and ultrathin source electrodes, and many others that will be further discussed in the following sections.

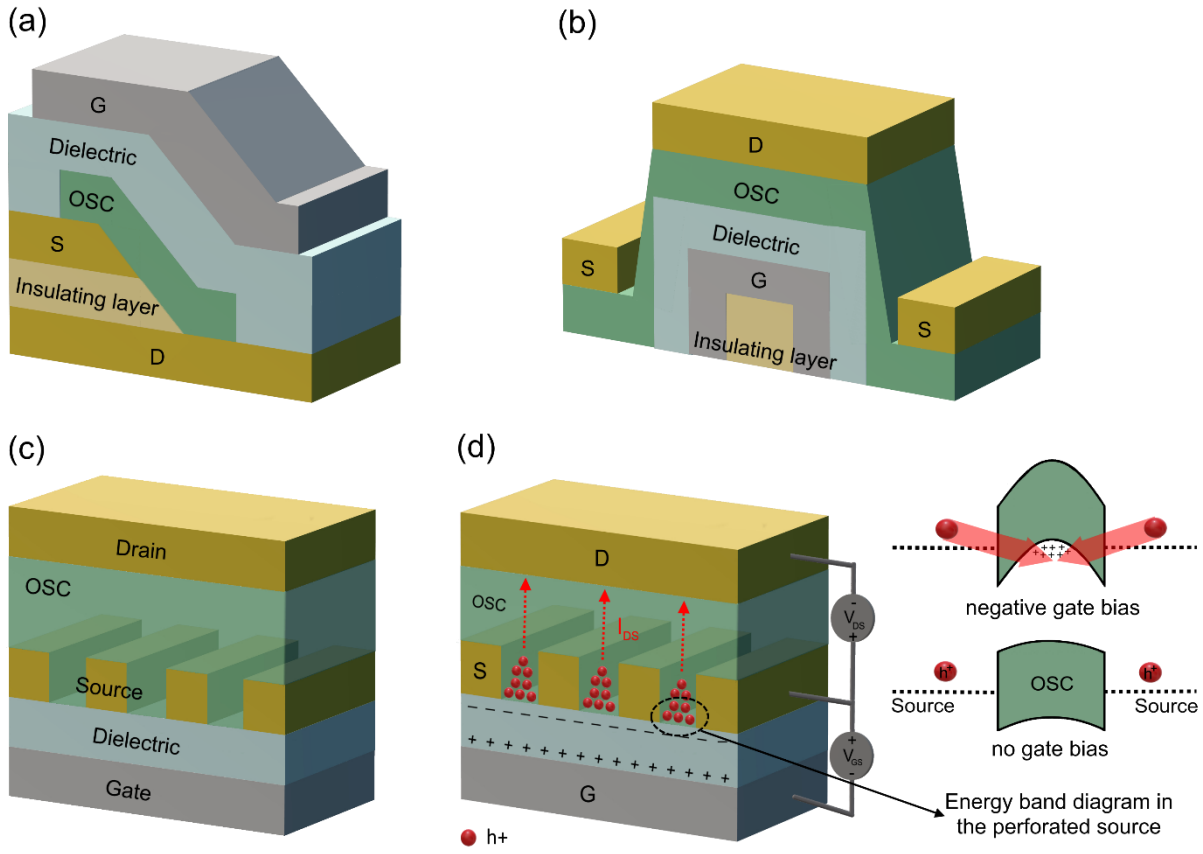


Figure 8. Schematic illustrations of FET-like architectures and device operation. (a) and (b) show examples of two types of step-edge VOFETs: (a) top-gate, and (b) bottom-gate. (c) SB-VOFET with a vertical configuration and a perforated source electrode. (d) Schematic representation of operation and current modulation for an SB-VOFET. On- and off-state band diagrams explain the current modulation mechanism through energy band bending. A lowering of the Schottky barrier is observed, which enables the formation of a vertical conducting channel perpendicularly to the OSC/dielectric interface. The OSC considered here is p-type, hence holes (h^+) are the majority charge carriers.

Figure 8d illustrates the operation and current modulation in an SB-VOFET. When V_{GS} is applied, the Schottky barrier at the perforated source/OSC interface is narrowed due to band bending. There is no more a large energy mismatch between the HOMO level of the OSC (p-type) and the Fermi level of the source electrode, and charge carriers can be easily injected from the source electrode into the OSC layer. Those injected charges accumulate at the gate dielectric/OSC interface forming a 'virtual contact'. With V_{DS} simultaneous application, the electric field forces these accumulated charge carriers from the OSC/dielectric interface

towards the drain electrode, resulting in a vertical diffusion of charge carriers [32,64,65]. The main difference in operation between this device and the planar OFET is that the channel transport is no longer restricted to the OSC/dielectric interface, but rather becomes distributed along the active layer volume (contributions in lateral and vertical directions). Also, the vertical transport is parallel to the gate electric field direction, therefore tuning I_{DS} [4,31].

2.3.1. Source Electrodes for SB-VOFETs

As discussed, the source electrode in SB-VOFETs plays a major role in the device operation: if a continuous metal source electrode is employed, it would completely screen the gate field due to a natural shielding effect observed in metallic films in the nanometer range, hence no modulation can be observed at the transistor conducting channel. In order to avoid this effect, several different approaches have been suggested such as ultra-thin metallic layer deposited through evaporation [24,66], metallic nanowires (NWs) films [22,67], perforated metal films defined by lithographic patterning [23,64,68,69], and carbon nanotubes [70].

The first SB-VOFET was presented by Ma and Yang in 2004 [24]. In contrast to conventional planar architectures, their study demonstrated an organic transistor with low working voltage (< 5 V), high I_{DS} (up to 10 mA), and impressive on/off ratio (over 10^6). It was possible by using a very thin source electrode, which showed a roughness comparable to its thickness, in combination with a high-capacitance cell [24]. A schematic cross-sectional view of the SB-VOFET proposed by Ma and Yang is shown in Figure 9a, illustrating the arrangement of the layers in the device's active region.

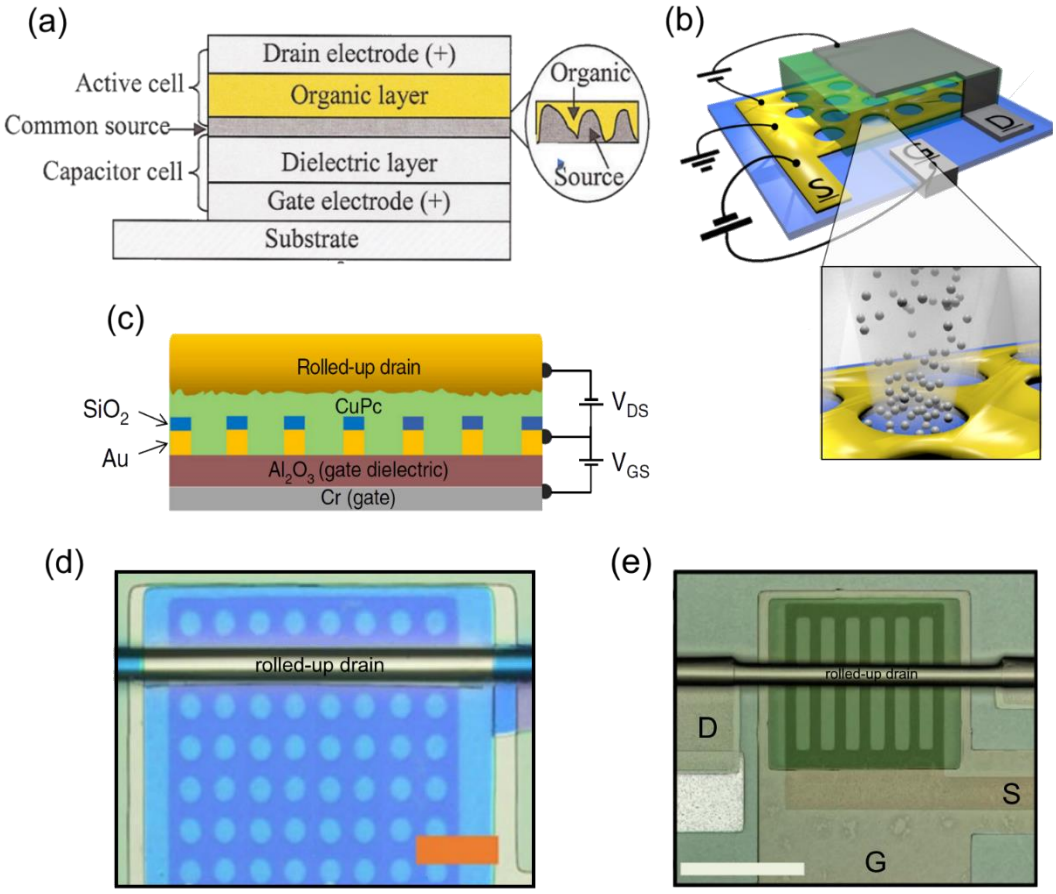


Figure 9. Overview of three outstanding SB-VOFET architectures. (a) Schematic cross-sectional view of the first SB-VOFET reported, which employed a very thin source electrode with a roughness comparable to its thickness, combined with a high-capacitance material as the gate dielectric. Adapted from ref.: [24]. (b) 3D cross-sectional view providing a clear visualization of an SB-VOFET with a nanopatterned metal electrode. The inset is the zoom-in image of the gap area showing the vertical flow of charge carriers. Adapted from ref.: [71]. (c) Schematic cross-sectional view of the rolled-up NM-based VOFET structure. Adapted from ref.: [21]. (d) and (e) Confocal laser scanning (CLS) microscopy images showing the two different patterns studied by Nawaz *et al.* (circular- and rectangular-shaped perforations, respectively). Scale bars correspond to 24 μm for (d) and 100 μm for (e). Adapted from ref.: [21].

Another attractive alternative to overcome the limitation of the source electrode is employing a patterned electrode (PE), which consists of an approach that has been successfully demonstrated by Ben-Sasson *et al* [23]. Their PE-VOFET (patterned-source vertical organic field-effect transistor) presented gaps in the source electrode with dimensions around 100 nm (a schematic tridimensional (3D) representation of the platform can be observed in Figure 9b), obtained through a soft lithography method based on a self-assembled block polymer of polystyrene (PS) and poly(methyl methacrylate) (PMMA). After selective removal of the

PMMA matrix, a physical mask made of PS nanoparticles is obtained and used for deposition of the source electrode. Then, the PS nanoparticles are removed through a lift-off process [23]. Therefore, Ben-Sasson and coworkers demonstrated a new and relatively high-resolution process that still maintained the low cost and simplicity associated with organic electronics. Also, it offers an easily controlled feature, the patterned source electrode, providing important benchmarks for new studies, including a better understanding of the platform operation as well as the means toward architecture optimization [23,65].

In 2020, Nawaz *et al*. reported a novel concept for SB-VOFET with a patterned source electrode, *viz.* the rolled-up nanomembrane-based VOFET. Such a device can entirely be processed via microfabrication techniques and photolithography-assisted patterning [21]. A schematic representation of the architecture can be observed in Figure 9c. The device employs a patterned source electrode with perforations defined through photolithography and deposition steps. The authors studied two different patterns with different perforation sizes (identical circular- and rectangular-shaped perforations, as shown in Figures 9d and 9e), showing how easily the perforation shape can be modified by employing this method.

Another important aspect of the platform is the use of a self-rolled nanomembrane (NM) as drain electrode, which allows reliable mechanical top contact with nanometer-thick organic semiconductors [21,27], as demonstrated by the scanning electron microscopy (SEM) image in Figure 10a.

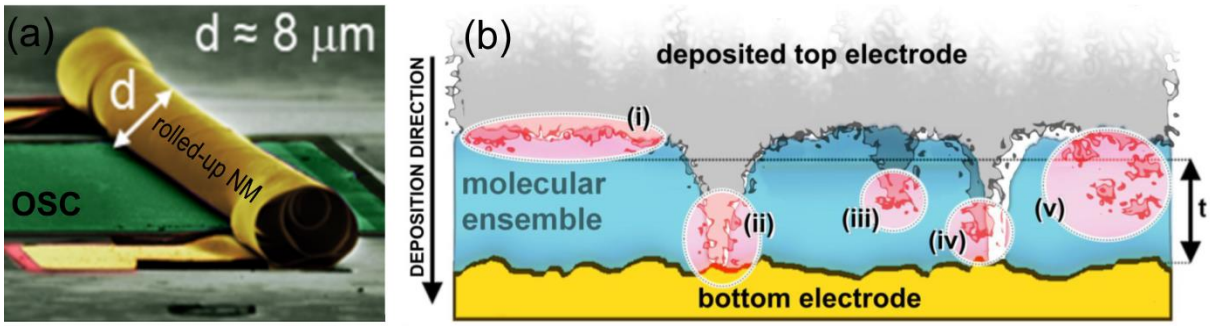


Figure 10. (a) False-color SEM image showing the mechanical top contact between the rolled-up drain electrode and the OSC layer for a rolled-up NM-based VOFET. (b) Schematic representation of common issues observed for top metal electrodes deposited over organic layers: (i) surface modification; (ii) short circuit; (iii) bulk modification; (iv) shortening of the conducting channel length; and (v) metal agglomerates into the organic layer. Adapted from ref. [21,26].

The rolled-up metallic NM employed as top drain-electrode works around some limitations commonly imposed by metal deposition on top of OSC films (*i.e.*, modification of OSC surface and/or bulk, short circuit, channel length shortening, and other examples illustrated in Figure 10b) [21]. The NMs are 2D structures with a thickness of a few nanometers and of lateral dimensions in the microscale, which can evolve into robust and flexible 3D structures (tube-like structures) able to stand freely in air or vacuum due to their large aspect ratio. The NM self-curling is possible because of a strain gradient originated during fabrication and depends on experimental conditions (*i.e.* the materials selected, layer thickness, and deposition rates) [28,72]. Therefore, NMs have proven attractive for various applications, such as ultracompact capacitors [73,74], heterojunctions [28,75,76], transistors [77–79], batteries [80], diodes [81,82], and so on.

Consequently, the rolled-up NM-based VOFET has one of the shortest channel lengths reported so far and exhibits a remarkable performance with ultra-low operating voltages (<3 V) as well as high current densities (~0.5 A cm^{-2}) [21].

2.3.2. Mechanism of Operation of SB-VOFETs

As previously stated, the SB-VOFET modulation relies on the gate electric field inducing a variation of the contact resistance at the source/OSC interface for charge carrier injection into the conducting channel. To facilitate the understanding of the modulation and operating mechanism, Figure 11a presents a cross-sectional view of a single source perforation of the PE-VOFET studied by Ben-Sasson *et al*. [2], illustrating the current behavior at off and at on states. When the device is turned off ($|V_{GS}|<|V_{th}|$), I_{OFF} is injected into the OSC from the top of the source electrode. In this case, the current injection is limited by a Schottky barrier, thus the current regime is the same expected for a Schottky diode, which is the Contact Limited (CL) behavior [2,65]. The current density for a PE-VOFET at off state is described by Equation IV [65]:

$$J_{off} = q\mu_n N_0 E_{\perp} \exp\left(-\frac{q\varphi_b}{kT}\right)(1 - FF) \qquad \text{(IV)}$$

Where q is the elementary charge, μ_n is the mobility for electrons (when considering an n-type OSC), N_0 is the density of states of the OSC, $E_{\perp}$ is the electric field perpendicular to the interface, φ_b is the energetic potential barrier, k is the Boltzmann constant, T is the temperature, and FF is the Fill Factor value (*i.e.*, the ratio between the total area of source perforations and the total area of the source electrode) [65].

In the on state ($|V_{GS}| \geq |V_{th}|$), the gate electric field is large enough to cause a lowering of the Schottky barrier in the source electrode/OSC interface, thereby enabling charge carrier injection into the OSC [2,65]. As shown in Figure 11a, the I_{ON} is established from the center of the perforation, where charge carriers are accumulated at the OSC/gate dielectric interface due

to gate bias [2]. In these circumstances, the large charge density at the center of the perforation creates an unlimited carrier reservoir (*i.e.*, a virtual contact), close to the behavior of an ohmic contact. Consequently, I_{DS} depends almost entirely on the semiconductor mobility and the charge density accumulated, thus the current regime expected to explain this behavior is the space-charge-limited current (SCLC) theory. [2,65]. The current density for a PE-VOFET at on state is described by the following equation [65]:

$$J_{on} = \frac{9}{8}\varepsilon_0\varepsilon\mu_n\frac{{V_{DS}}^2}{L^3}FF \qquad \text{(V)}$$

Where ε_0 and ε are the relative permittivity and the vacuum permittivity respectively. Additionally, for a better understanding of the current behavior at on state, Ben-Sasson *et al.* analyzed the charge concentration distribution in a single source perforation by employing two-dimensional (2D) numerical simulations (Figure 11b in logarithmic scale) [65]. The charge concentration displays a maximum close to the OSC/gate dielectric interface (virtual contact) and starts to reduce exponentially up to a certain point where it becomes constant (z-axis). This region is where the diffusion-controlled current is dominant, as indicated in Figure 11b. At the region with constant charge concentration, injected charge carriers are vertically pulled towards the drain electrode, forming the vertical channel. This inversion in the current direction occurs at a particular spatial location called the inversion point and depends on the electric fields from all three electrodes (lateral and vertical contributions). In this region, the drift-controlled current is dominant, as indicated in Figure 11b [2,65].

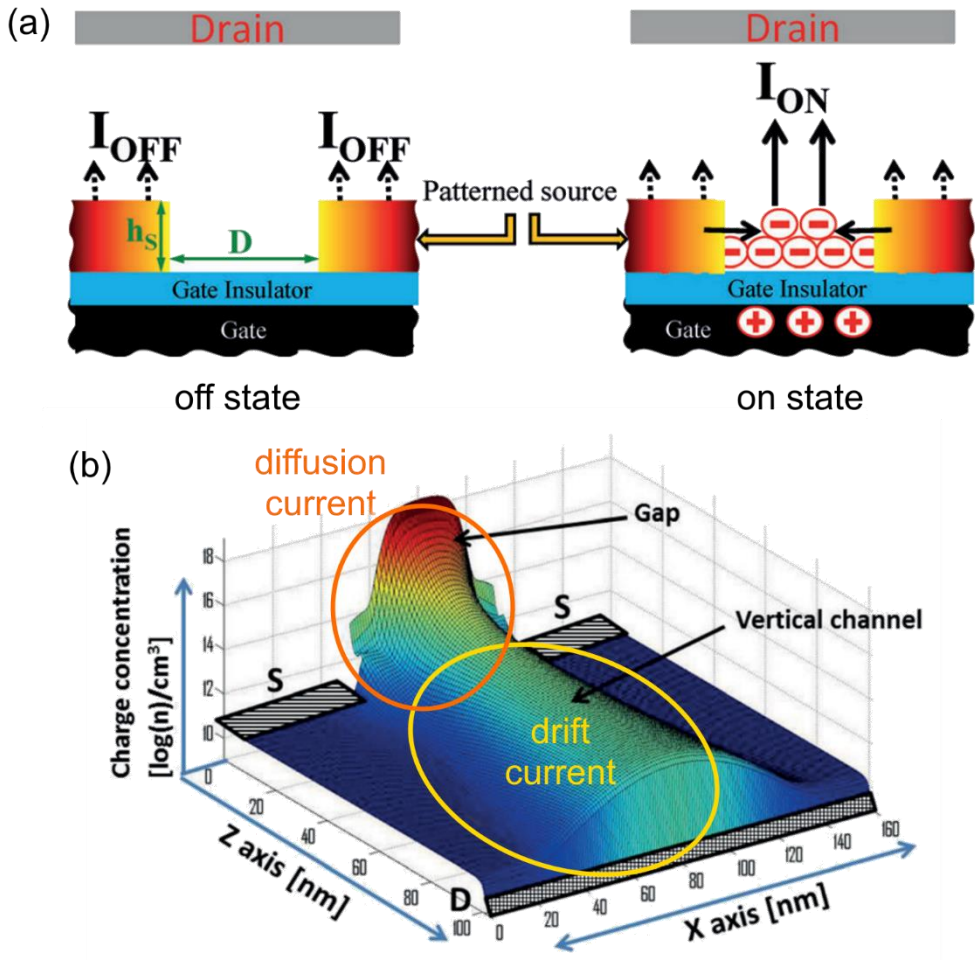


Figure 11. Representation of the mechanism of operation for an SB-VOFET with nanopatterned source electrode. (a) Schematic cross-sectional view for a single source perforation showing the current behavior while the device is at off and at on state. In the off state, I_{OFF} is injected from the top of the source electrode. In the on state, the I_{ON} is established from the center of the perforation, where charge carriers are accumulated (virtual contact) due to gate bias. Adapted from ref.: [2]. (b) 2D numerical simulation analyzing the charge concentration distribution in a single source perforation (logarithmic scale). The regions where diffusion- and drift-controlled current is dominant are indicated. The device studied has the following specs: 60 nm of perforation width (x-axis), 100 nm of conducting channel length (z-axis), and biasing conditions of V_{GS} = 5 V, V_{DS} = 2 V. Adapted from ref.: [65].

For instance, Nawaz *et al*. demonstrated that for an SB-VOFET with a patterned source electrode, the formation of the vertical conducting channel can occur in the center of the perforation or the vicinity of the source edges depending on the perforation size, and such feature might enhance current density [21]. Figure 12 shows their theoretical study performed in COMSOL Multiphysics. The upper panels illustrate schematic cross-sectional views for a single source perforation demonstrating the electric potential variation along the conducting

channel with a color gradient. The lower panels compare the normalized current density distribution within the conducting channel (along the region indicated by the dashed lines in the cross-sectional views).

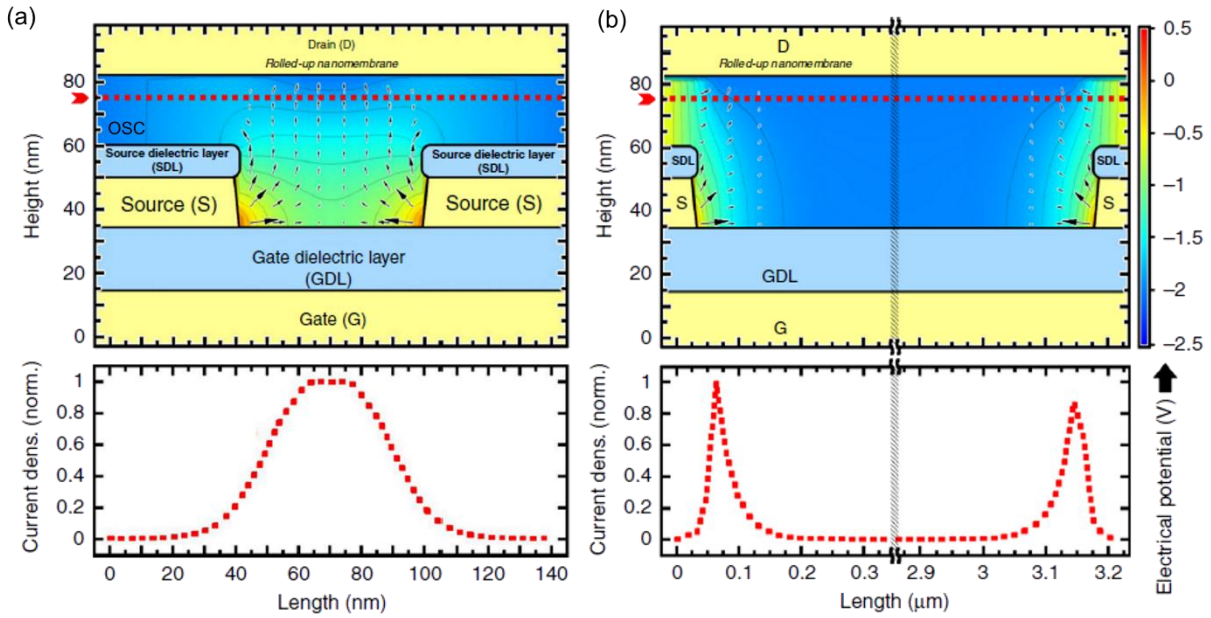


Figure 12. Theoretical simulations performed in COMSOL Multiphysics analyzing current density distribution in a rolled-up nanomembrane-based VOFET while at on state. The upper panels show a schematic cross-sectional view for a single source perforation demonstrating the electric potential variation along the conducting channel with a color gradient. And the lower panels show the normalized current density distribution within the OSC layer (along the regions indicated by the dashed lines in the cross-sectional view). (a) and (b) show the simulations performed for two different perforation sizes (50 nm and 3 μm respectively), while bias application of $V_{GS} = V_{DS} = -2$ V. Adapted from ref.: [21].

In Figure 12a, the device has a patterned electrode with nanometric perforations (resembling the PE-VOFET studied by Ben-Sasson *et al.* [23]), exhibiting high current density distribution concentrated at the center of the source perforation. In this case, the vertical channel is under a 'tunnel' effect as a result of considerable lateral electric fields caused due to the proximity between the source electrode edges. Considering the device performance, such a 'tunnel' is not ideal, because charge carrier flow is confined to a very narrow region, thus suppressing I_{DS} [21,65].

For a device with a patterned source electrode with perforations of 3 μm (resembling the PE-VOFET studied by Nawaz *et al.* [21]), the current density is concentrated close to the

source edges, since lateral electric fields are not substantial to cause any influence (Figure 12b). Therefore, the theoretical simulations allowed them to demonstrate that the formation of a vertical conducting channel occurs in the vicinity of the source edges, rather than being concentrated at the center of the micrometer-wide perforation [21]. Accordingly, this study raises the possibility that SB-VOFET output current may be enhanced, once it shows a relation with the number of source edges (n_{SE}).

2.4. ORGANIC PHOTOTRANSISTORS

To date, optoelectronic devices are one of the major roles played by semiconductor materials and have proved to be an important application due to encouraging and extensive improvements in many fields, including industrial, communication, and military. Optoelectronic devices can be classified into two main categories, photodetectors and emitters [83,84]. The concept of photodetectors is one of the most widely employed, they operate by converting an incident optical signal into light-induced current or voltage drop. Some examples are photoconductors, photodiodes, and phototransistors [83,85]. Since it was first reported in 1951 by Shockley *et al*. [86], phototransistors have proven to be an appealing option due to their operating mechanism, which combines optical detection converted into an electrical signal (photodiode functions) with the signal-amplification (transistor function), thereby demonstrating higher sensitivity and lower noise [84,87,88]. Some examples of high-performance phototransistors employ semiconductor materials such as metal oxides [89,90], transition metal dichalcogenides (TMDs) [91–93], and OSCs [94].

The phototransistor efficiency in converting optical power in electrical signal is commonly quantified by the figures of merit photosensitivity (P) and photoresponsivity (R), which are defined by the following equations [84,87]:

$$P = \frac{I_{light} - I_{dark}}{I_{dark}} \quad \text{(VI)}$$

$$R = \frac{I_{light} - I_{dark}}{P_{inc} A} \quad \text{(VII)}$$

Where I_{light} and I_{dark} are the measured I_{DS} values under illumination and in the dark respectively, P_{inc} is the power of incident light per unit area, and A is the effective device area. High-performance OPTs exhibit P values around 10^4 - 10^6 and R values around 10^2 - 10^5 [95–99].

Currently, great attention has been directed toward organic phototransistors (OPTs) owing to their outstanding electro-optical properties combined with low-cost processing, lightweight, and mechanical flexibility, therefore they have proven attractive for various applications, such as sensors [100–102], memory devices [103,104], optical switching [105], etc. The OPT operating mechanism depends on light-absorbing (*i.e.*, photons of energy equal to or higher than the absorption range of the OSC), then the exciton formation and dissociation in additional free charge carriers, resulting in amplification of output current [84,106]. However, exciton dissociation is not as favorable in organic semiconductors as in inorganic semiconductors. Also, as mentioned before, planar OFETs often show high operating voltages (>20 V), thus limiting the device efficiency because of the high energy consumption [84,88].

To address this issue, OPTs have been extensively studied and different methods have been proposed [94–99,103]. In particular, the combination of reduced channel length and low operating voltages observed for VOFETs effectively enhance photoelectric conversion (*i.e.*, high photosensitivity) with simultaneously fast response (*i.e.*, low subthreshold swing, S). On this regard, Figure 13 presents some examples of vertical OPTs developed recently. Wu and coworkers reported a vertical OPT for optical memory and data storage purposes [103]. Their device was a floating-gate transistor with a nanoscale conducting channel, as shown in

Figure 13a. The floating-gate layer (*i.e.*, gate dielectric) is a PMMA composite with CdSe/ZnS quantum dots (QDs), and the conducting channel is a p-type OSC copolymer poly[1,2,5]thiadiazolo[3,4-c]pyridine-4,7-diyl(4,4-dihexadecyl-4H-clopenta[2,1-b:3,4-b0]dithiophene-2,6-diyl)[1,2,5]thiadiazolo[3,4-c]pyridine-7,4-diyl(4,4-dihexadecyl-4H-cyclopenta[2,1-b:3,4-b0]dithiophene-2,6-diyl) (PCDTPT). Therefore, this combination resulted in OPTs exhibiting excellent memory window (73 V) with good responsivity (>104 A/W) [103].

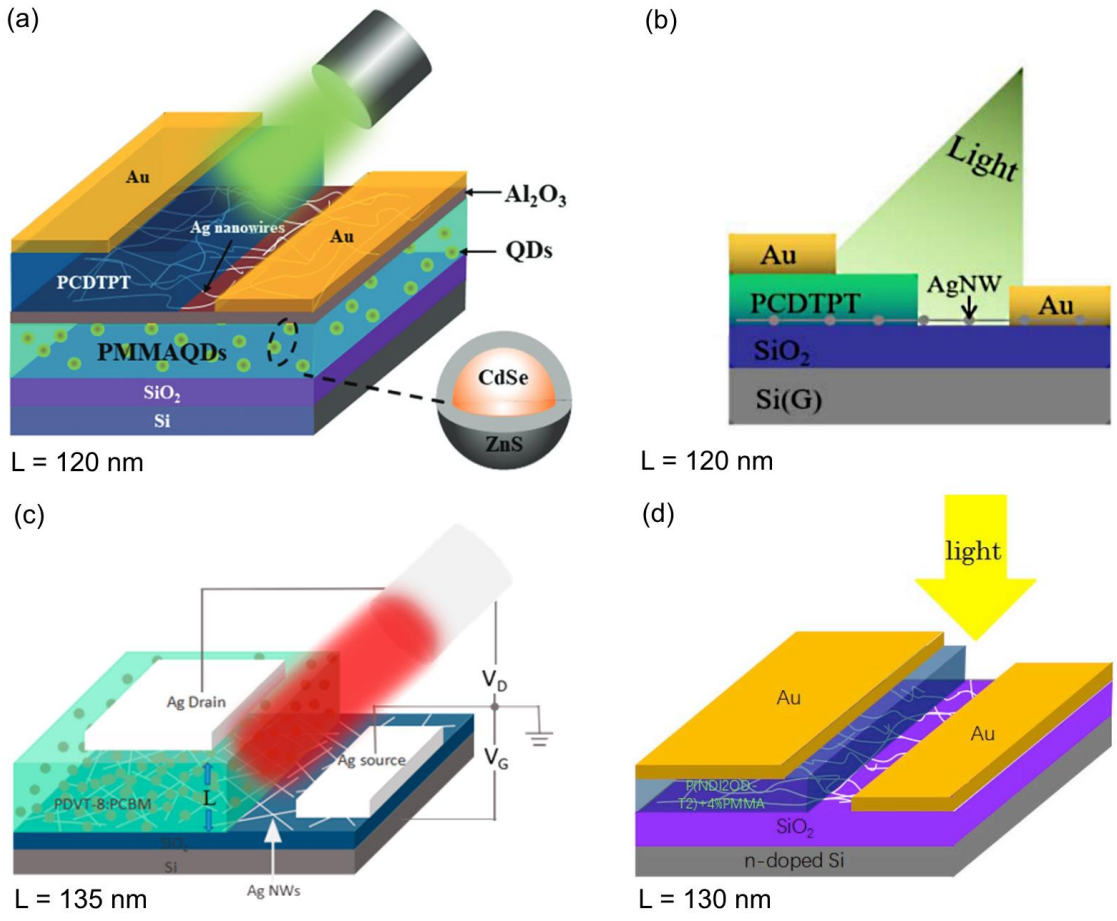


Figure 13. Examples of vertical OPT architectures: (a) OPT employing PCDTPT as conducting channel and a PMMA composite with CdSe/ZnS QDs as the floating gate dielectric. Adapted from ref. [103]. (b) OPT employing a copolymer PCDTPT as conducting channel. Adapted from ref. [107]. (c) OPT employing a polymer BHJ blend of PDVT-8/$PC_{61}BM$ as conducting channel. Adapted from ref. [99]. (d) OPT employing an n-type OSC mixed with PMMA as conducting channel. Adapted from ref. [94].

Similarly, aiming to compare OPT performance for planar and vertical architectures (Figure 13b), Zhang *et al*. investigated the effect caused when doping the OSC PCDTPT with [6,6]-phenylC_{61} butyric acid methyl ester ($PC_{61}BM$) [107]. The vertical devices showed impressive performance, including ultrahigh responsivity (~7×10^3 A/W) [107].

Zhong *et al*. proposed a novel vertical OPT with a conducting channel based on a polymer bulk heterojunction (BHJ) blend of poly[2,5-bis(alkyl)pyrrolo[3,4-c]-pyrrole-1,4(2H,5H)-dione-alt-5,5′-di(thiophen-2-yl)-2,2′-(E)-2-(2-(thiophen-2-yl)vinyl)-thiophene] (PDVT-8) and $PC_{61}BM$ as illustrated in Figure 13c. The devices showed high photoresponsivity (>750 A/W) and remarkable photosensitivity ($P = 10^6$) [99]. Most recently, Yeliu *et al*. demonstrated for the first time the use of an n-type OSC as the conducting channel for a vertical OPT (Figure 13d) [94]. Such a choice of OSC is considered unconventional because n-type OPTs often demonstrate poor performance. To overcome this difficulty, they doped the poly{[N,N′-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5'-(2,29-bithiophene)} P(NDI2OD-T2) with PMMA and PS, which improved free charge carrier generation efficiency, thus enhancing performance (R ≈ 30 A/W and P ≈ 10^4) [94].

Overall, the previous section has outlined some examples of alternative vertical architecture OPTs. These studies clearly support that there is a relationship between photoresponse and the transistor conducting channel length. Accordingly, the concept of the r-VOFET platform not only has one of the shortest conducting channels ever reported (tens of nanometers) but also demonstrates facilitated external stimuli with the active layer. In order to test whether these features allow surpassing the performance of state-of-the-art OPTs, in this work, we suggested some approaches to circumvent the limitations observed in the rolled-up NM-based VOFET architecture developed by Nawaz *et al*. [21], and fabricated optimized devices presenting improved performance and reproducibility. Furthermore, the fabrication and electrical characterization of these optimized devices are described in the following chapters.

3. METHODS AND MATERIALS

In this work, we present a VOFET platform with convenient device integration due to close structural similarity to planar OFETs. The on-chip devices were manufactured by microfabrication techniques, which provide high resolution associated with low-cost and low-complexity processes. Processing the devices entirely employing photolithography-assisted patterning effectively allowed a more careful control over shape and size to study the effect caused when changing electrode structures. Hence, the rolled-up NM-based VOFET architecture developed was based on Nawaz *et al*. study [21]. Our device fabrication comprises eight photolithography steps, eight thin-film depositions, and two etching steps. The architecture modifications and improving alternatives employed will be further discussed in Chapter 4.

3.1. DEVICE PATTERNING VIA PHOTOLITHOGRAPHY

The rolled-up NM-based vertical organic field-effect transistors (r-VOFETs) were fabricated on 9 x 9 mm^2 size, SiO_2 coated (2 µm thick)/<100> Si substrates. Figure 14a exhibits a confocal laser scanning (CLS) microscopy image (top view) of a fully fabricated microchip with a total of 35 devices, which was manufactured using conventional microfabrication processes, such as photolithography, thin-film deposition, and etching.

Photolithography is a technique used for the patterning of device structures on substrates/wafers. Thus, it employs a photoactive organic material (resist) modified locally to create patterns (as a physical mask) delimiting regions of the substrate/wafer surface, which later can be subjected to a step of etching, deposition, or other modification of the underlying material [108]. Figure 14b illustrates the photolithography patterning process step by step using

an image reversal resist, the same type employed for the fabrication of our devices (AZ 5214E purchased from Microchemicals GmbH). The steps depicted in Figure 14b are: (i) a few milliliters of resist is applied over the substrate/wafer by spin coating; (ii) a bake step to remove the resist solvent; (iii) photomask alignment to the patterns already defined on the substrate/wafer; (iv) exposure of uncovered-resist regions to ultraviolet (UV) light; (v) an additional bake to promote the diffusion of photogenerated molecules; (vi) an additional UV exposure responsible for changing the resist solubility in the developer due to crosslinking between molecules; and (vii) the development step, which the soluble resist regions are etched away. Step (viii) compares when a metal deposition occurs over a positive mode resist (positive undercut) and a negative mode resist (negative undercut) [108].

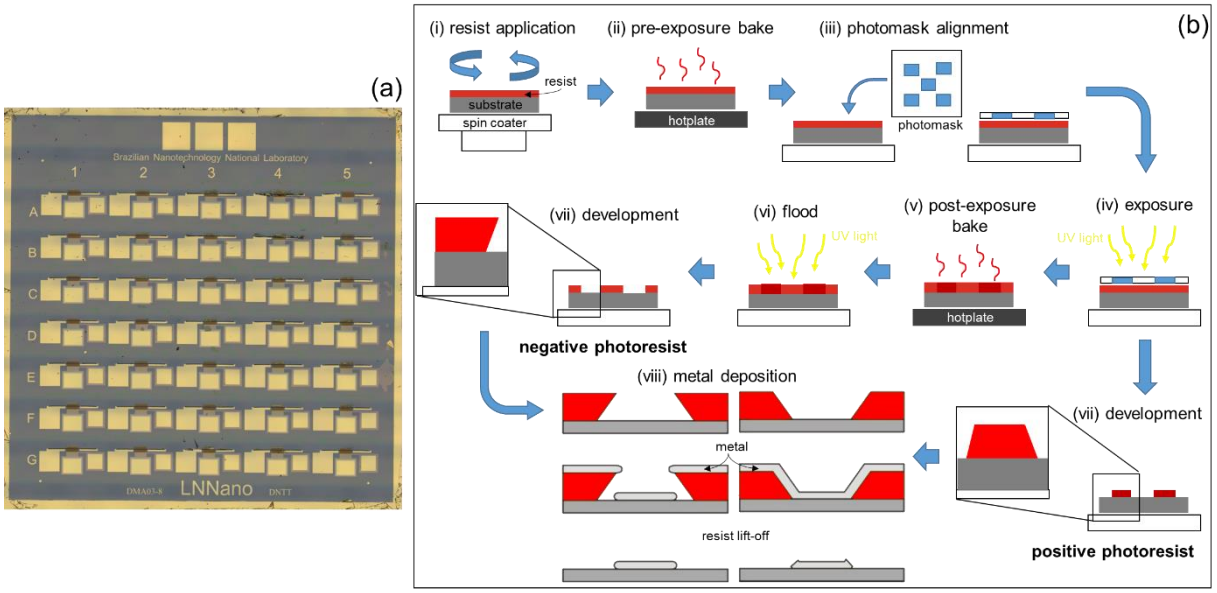


Figure 14. Microchip (9 x 9 mm^2) manufactured by microfabrication techniques and photolithography patterning steps. (a) CLS microscopy image of a fully fabricated microchip consisting of 35 r-VOFETs. (b) Schematic representation of the photolithography patterning process step by step using an image reversal resist. An image reversal resist can either be processed in positive or negative mode depending on additional processing steps. Adapted from submitted manuscript ref [110].

In terms of thin-film deposition methods, we employed thermal evaporation for the deposition of metallic and oxide films (e-beam deposition system (AJA International Inc.) shown in Figure 15a) and organic semiconductor thin films (resistive filament deposition

system (Leybold Univex 250) shown in Figure 15b) under a vacuum pressure of ~10^{-7} Torr. In the deposition chambers, quartz crystal microbalances were used to monitor the film thickness during growth.

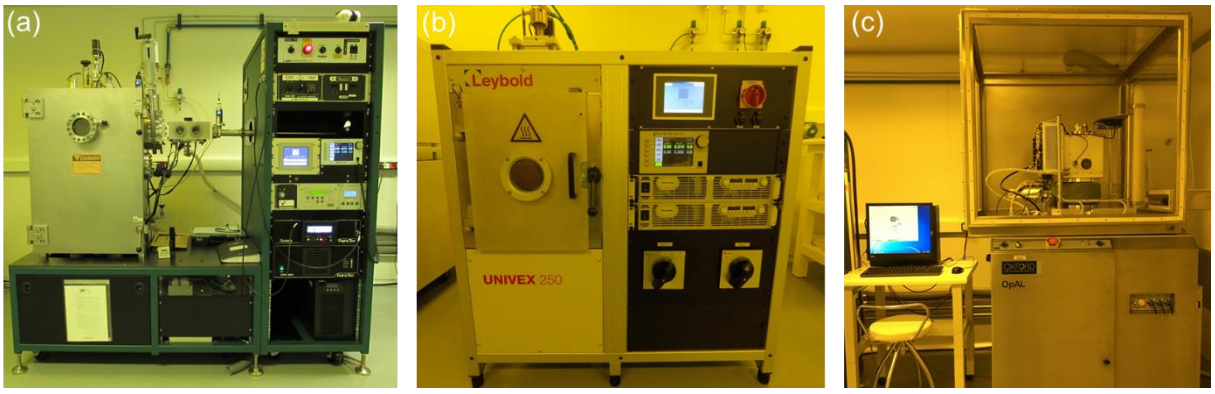


Figure 15. Thin-film deposition equipment employed in the r-VOFET fabrication. (a) Electron beam deposition. (b) Resistive filament evaporation. (c) Atomic layer deposition (ALD). Photographs adapted from ref.: [109].

In the electron beam and resistive evaporation deposition methods, high vacuum (>10^{-6} Torr) is used to ensure highly directional film growth. Localized heating into a crucible vaporizes the material and the evaporated atoms/molecules are transported directly to the substrate/wafer, where it is condensed and deposited as a thin film. Electron beam deposition is often used for low-melting-point metals and a few metal oxides, and resistive evaporation for the deposition of small organic molecules [108].

Accordingly, before the first microfabrication step, the substrates were cleaned in an ultrasonic bath using acetone and isopropanol (electronically graded, VLSI) for 30 min each, followed by exposure to oxygen plasma for 5 min. The cleaned substrates were then passivated with spin-coated hexamethyldisilazane (HMDS, obtained from Technic, Inc.) at 3000 rpm for 30 s, and thermally treated for 3 min at 100°C.

Figure 16 illustrates all the microfabrication steps necessary for obtaining a complete r-VOFET. Once the samples were passivated, a *mesa* structure was defined on the substrate surface (Figure 16a). This structure ensures a vertical contact between the rolled-up NM

(caused by the height difference between the *mesa* structure and the substrate surface) and the organic semiconductor film, and also it lessens substrate eddy current interference. Therefore, the *mesa* structure was patterned employing a reverse-mode lithography step (including gate and source electrode pads), followed by the deposition of 15 nm Cr, lift off of the resist using acetone, and last, 190 nm SiO_2 etching around the Cr structure (used as an etching mask besides acting as the transistor gate electrode). The Cr deposition was carried out at an evaporation rate of ~0.6 Å/s and the SiO_2 etching was performed by using a reactive ion technique (Oxford PLASMAPro 80 etching system). The etching gas employed was tetrafluoromethane (CF_4).

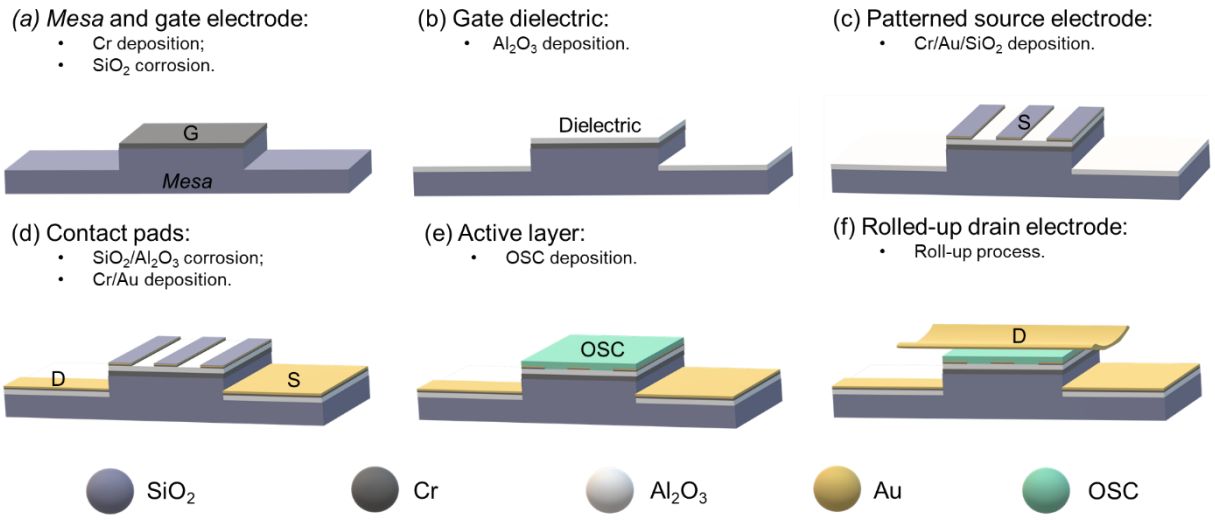


Figure 16. Schematic illustrations for each step of the r-VOFET microfabrication. (a) Definition of a *mesa* structure and the gate electrode with the deposition of a Cr thin film and SiO_2 etching. (b) Deposition of the gate dielectric (Al_2O_3) over the entire substrate. (c) Definition of the patterned source electrode by the deposition of Cr/Au/SiO_2 films. (d) SiO_2/Al_2O_3 etching from the pads and definition of the drain electrode and electrical contacts by the deposition of Cr/Au films. (e) Deposition of the OSC at the device active region. (f) The roll-up process promotes a soft mechanical contact between the tubular-shaped drain and the OSC thin film.

As the gate dielectric, 20 nm thick Al_2O_3 film was grown over the entire substrate using atomic layer deposition (ALD), which is a deposition method with great thickness control since the film is deposited one atomic layer at a time (Figure 16b). Also, the film is grown in pulses of precursor gas molecules reacting with the substrate surface atoms [108]. Al_2O_3 was chosen because of its high dielectric constant (~9) and wide bandgap (~2.7 eV). The deposition

was performed on a Cambridge NanoTech Savannah 100 ALD system (Figure 15c) employing trimethylaluminum (TMA; Sigma-Aldrich) and water as precursors. The temperature of the sample stage was kept at 150°C and the growth rate was 1.5 Å/cycle. The chamber pressure was set between 120–260 mbar, and argon was used as the carrier/purging gas at a flow from 30 to 100 sccm.

Afterward, the rectangular-perforated source electrode was defined (Figure 16c), which was patterned by employing a reverse-mode lithography step, a deposition step of 5 nm Cr, 10 nm Au, and 10 nm SiO_2 layers (carried out at an evaporation rate of ~0.6 Å/s), and lift-off of the resist. It is worth mentioning that, a SiO_2 10 nm thick film is deposited on the top of the patterned source to ensure that current injection takes place predominantly from the source edges into the organic semiconductor channel, either at on- or off-state, thus improving the transistor saturation [21]. Concerning electrical contact with the gate Cr film, Al_2O_3 was etched from the top of the gate electrode pad (Figure 16d). In order to perform the Al_2O_3 etching, first, a direct-mode lithography was employed to define an etching mask and protect the rest of the substrate, followed by a hard bake for 10 min at 100°C. Al_2O_3 was etched with hydrogen fluoride (HF) aqueous solution (1% v/v) for 18 s and the resist was removed concluding this step.

The next photolithography step was the definition of contact pads, a structure consisting of drain and gate pads, which main concern was good electrical contact, thus thicker metallic contact pads are deposited. A reverse-mode lithography was performed, and Cr and Au (10 and 50 nm) were deposited at a rate of ~0.6 Å/s, followed by lift-off. After that, a sacrificial layer of 20 nm thick Ge film was deposited, which was oxidized later in the H_2O_2 solution during the roll-up process. The structure was patterned through a reverse-mode lithography step. Then, an anchor layer of Cr (10 nm) was defined. This structure connects the sacrificial layer to the drain pad. Sequentially, the strained layer was defined by another reverse-

mode lithography step and deposition of 5 nm Au, 15 nm Ti, 20 nm Cr, and 15 nm SiO_2. The NM comprising Ti/Cr/SiO_2 films shows a strain gradient necessary for the roll-up process, while the Au film was employed as an electric contact between the OSC film and drain pad after the roll-up. In the last photolithography step, the OSC at the device active (Figure 16e) region and a trench structure were defined, the latter is employed to ensure that the roll-up solution would promote a selective removal of the sacrificial layer, and the device active region. As follows, the OSC was deposited at the device active region, a 35 nm thick dinaphtho[2,3-b:2′,3,-f]thieno[3,2-b]thiophene (DNTT) film. We employed a Leybold UNIVEX 250 deposition system at a rate of ~0.2 Å/s.

To complete the device architecture, the last step was the roll-up process assisted by the selective removal of GeO_x in H_2O:H_2O_2 (1:0.0025) solution, which releases the strained layer. The strained layer stored elastic energy promotes a curling-up of this planar structure until reaching the anchor layer, assuming a cylindrical shape (typical diameter of ~8 μm) and promoting a soft and reliable electrical contact between the drain electrode and the top of the OSC film (Figure 16f). The total roll-up time necessary for the NM to reach the trench structure lower limit took around 10 min, then the resist was removed in acetone and the sample was put back in the roll-up solution for more ~5 min so that the NM could reach the device active region.

3.2. ELECTRICAL CHARACTERIZATION

Prior to the electrical characterization, the devices were stored for around three days in vacuum of 10^{-2} Torr to remove solvents from the self-rolling process and preserve the as-fabricated properties. The r-VOFET characteristics were evaluated by measuring output (I_{DS} *vs.* V_{DS}) and transfer curves (I_{DS} *vs.* V_{GS}), which were acquired using a Keithley 4200 SCS coupled to a LakeShore EMPX-HF cryogenic probe station (Figure 17a). The device operation

was evaluated in environmental temperature with a controlled N_2 flow to carry H_2O vapor out of the chamber. Figure 17b shows a 3D schematic representation of the electrical measurement configuration employed and the positions where the voltage is applied to each electrode pad.

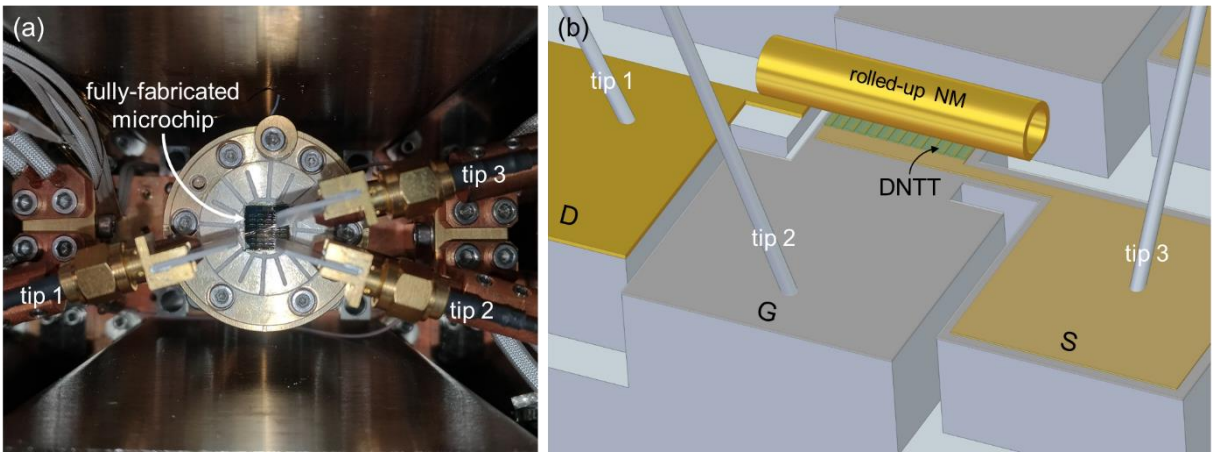


Figure 17. Rolled-up NM-based VOFET electrical characterization. (a) Photograph showing the electrical measurement configuration using a Keithley 2636B SourceMeter® coupled to LakeShore EMPX-HF cryogenic probe station. (b) 3D schematic representation of rolled-up NM-based VOFET during electrical measurement with the S, D, and G electrodes identified inset.

In order to investigate the photoelectric performance of our r-VOFETs when applied as OPTs, we conducted a series of electrical measurements under illumination employing different monochromatic light colors, *i.e.*, 450 nm (blue), 550 nm (green), and 700 nm (red). Therefore, an RGB light-emitting diode (LED) was coupled inside the cryogenic probe station chamber. The RGB LED illumination was controlled and adjusted using a two-channel Keithley 2636B SourceMeter® (Figure 18a). During electrical measurements, to ensure that the light would assess the r-VOFET active layer, the sample is illuminated from the top with an incident angle avoiding the rolled-up nanomembrane as illustrated in Figure 18b.

Also, to increase reliability, each device tested must be reset before electrical characterization, which is a step called the reset phase. The reset phase is done by applying a large negative V_{GS} value (V_{GS} = -4.2 V) simultaneously with a small V_{DS} value (V_{DS} = -0.1 V), therefore releasing trapped photogenerated charge carriers and promoting their recombination.

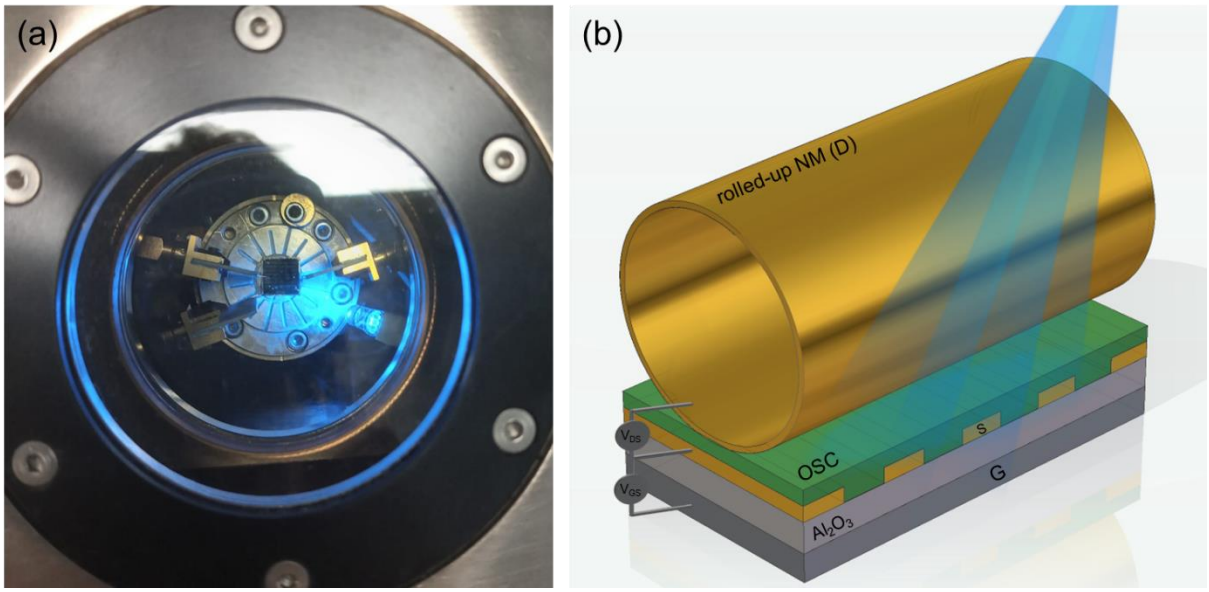


Figure 18. Study of the OPT characteristics for r-VOFETs. (a) Photograph showing the RGB LED coupled inside of the cryogenic probe station. (b) Cross-sectional view of the r-VOFET while top-illuminated by blue light. Adapted from submitted manuscript ref [110].

3.3. MICROSCOPY CHARACTERIZATION

During the r-VOFET fabrication, after each microfabrication step, optical microscopy images were taken employing a Zeiss Axio Imager.A2 microscope in order to carefully check the patterned structures. Once the samples were fully fabricated, images showing the r-VOFET architecture were acquired employing CLS microscopy (Keyence VK-X200 3D laser scanning microscope) and SEM (Inspect F50 scanning electron microscope).

For a morphological study, the DNTT film and the patterned source electrodes were characterized by atomic force microscopy (AFM) in tapping mode (Park Systems - AFM NX10).

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4. RESULTS AND DISCUSSION

This section summarizes and discusses the main findings of the work, focusing on two key themes: the r-VOFET performance optimization and the platform potentiality for sensor technologies. First, we detail our r-VOFET fabrication according to the method reported in 2020 by Nawaz *et al*. [21] intending to evaluate its reliability and reproducibility. Second, we evaluate the device's electrical characteristics when employing a high-performance OSC as our transistor-conducting channel. Third, we point out some optimizations in the fabrication process to improve reproducibility and performance, thereby allowing a more reliable extraction of some important device parameters and study of the operating mechanism. Finally, we report remarkable findings about the r-VOFET photoresponse, demonstrating that our platform is a promising approach to surpass the performance of state-of-the-art organic photodetectors.

4.1. r-VOFET FABRICATION

Our fabrication process is shown in Figure 19 by optical microscopy images taken after each step. Additionally, a schematic cross-sectional view of the layer arrangement at the device active region (red dotted line) is illustrated at the bottom of each panel. In the first step (Figure 19a), we patterned a *mesa* structure on a Si/SiO_2 wafer with the deposition of a Cr 15 nm thick film followed by the anisotropic SiO_2 etching (down to 190 nm) around it. The Cr-covered *mesa* is designed to play the role of the r-VOFET gate electrode. As the gate dielectric, we deposited a 20 nm thick Al_2O_3 film over the entire substrate surface by ALD. Afterward, we defined a source electrode with rectangular-shaped perforations employing photolithography and electron-beam evaporation techniques. Then the Al_2O_3 covering the gate-electrode pad was etched to provide a bare metal surface for electrical contact (Figure 19b).

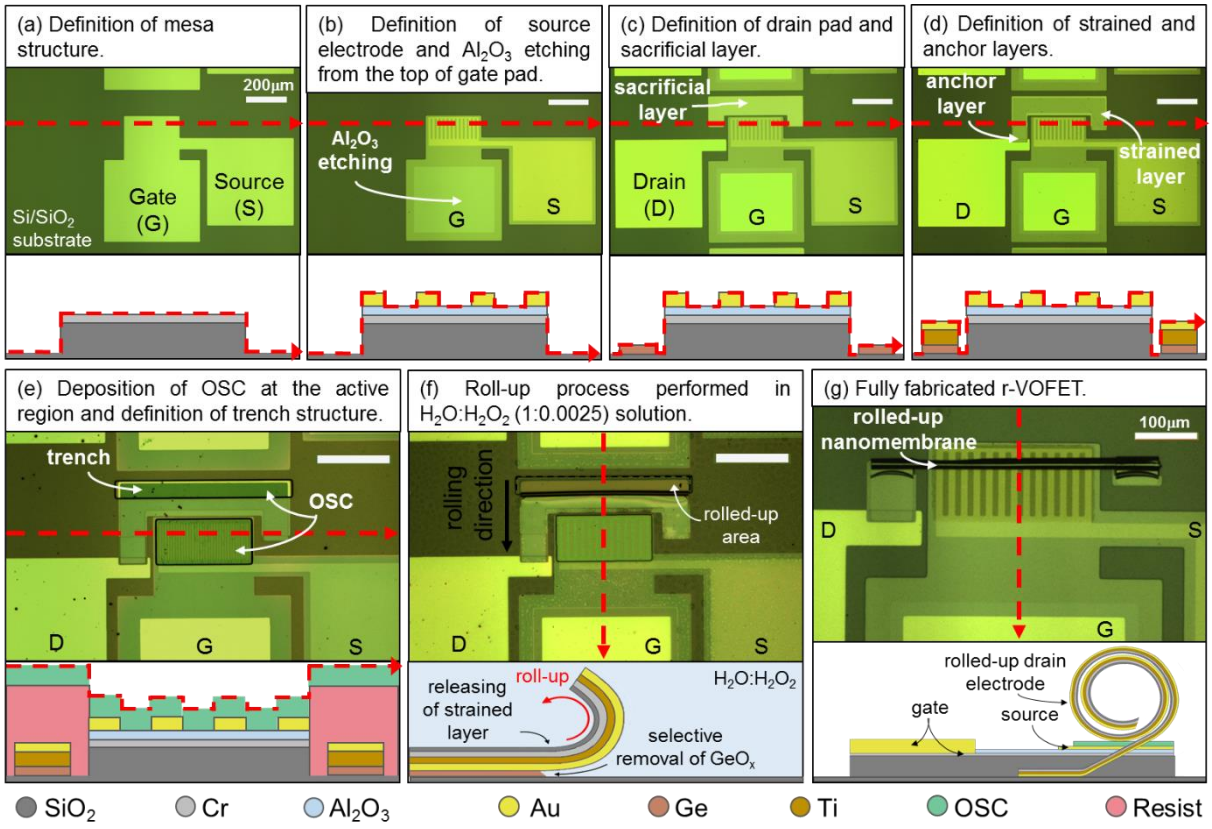


Figure 19. Optical microscopy images of each step of the r-VOFET microfabrication. The dashed lines indicate cross-sectional views for the layer arrangement at the device's active region, as shown in the bottom panels. (a) A *mesa* structure was defined with the deposition of a Cr thin film and SiO_2 etching. (b) An Al_2O_3 thin film, employed as the gate dielectric, was deposited over the entire substrate, followed by the definition of the patterned source electrode (Cr/Au/SiO_2 films) and Al_2O_3 etching from the top of the gate electrode pad. (c) The drain electrode (a Cr/Au bilayer) and the sacrificial layer (Ge thin film) were patterned on the substrate. (d) A Cr thin film (named as anchorage layer) was deposited, followed by the definition of the strained layer, an NM comprising Au/Ti/Cr/SiO_2 films. (e) Definition of a trench structure to allow the aqueous solution to access the sacrificial layer, and subsequent deposition of the OSC at the device active region. (f) NM roll-up process assisted by the selective removal of GeO_x and releasing of the strained NM (cross-section: thin film stacking of GeO_x sacrificial layer and strained layer). (g) Fully fabricated r-VOFET (cross-section: NM tubular shape forming a soft mechanical contact with the OSC thin film). Adapted from submitted manuscript ref [110].

In Figure 19c, the drain electrical contacting pad (*viz.*, a 60 nm thick Cr/Au bilayer) and the sacrificial layer (20 nm of Ge) were patterned, respectively, on the sample substrate. Then we deposited a 10 nm thick Cr film, named the anchor layer, to connect the sacrificial layer to the drain pad and the strained layer (*i.e.*, an NM comprising Au/Ti/Cr/SiO_2 films on top of the sacrificial and anchor layers), as shown in Figure 19d. The last photolithography step was performed to define a trench structure (Figure 19e), which ensures that the roll-up solution promotes a selective removal of the sacrificial layer (*i.e.*, oxidation of the Ge thin film, which

becomes soluble in water) with the simultaneous release of the strained NM that self-curls towards the device active region. Finally, the OSC thin film was deposited on the device's active region.

Figure 19f shows the NM roll-up process assisted by the selective removal of GeO_x, which releases the strained layer and promotes its self-curling until reaching the lower limit of the trench structure. After removing the resist, the NM continues to curl up and stops at the device active region, as shown in Figure 19g, the top-view of the r-VOFET active region at the end of the device fabrication. Notice that the rolled-up NM contacts the OSC film from the top (Figure 19g, bottom panel), promoting a reliable soft electrical contact between the self-rolled drain electrode and the nanometer-thick OSC layer.

Figure 20a shows a false-color SEM image of the active region for a fully fabricated r-VOFET, consisting of a rolled-up drain electrode (in yellow), OSC film (in green), and patterned source electrode with rectangular perforations (gap of 9 μm with a total of 26 source edges). To provide a clear visualization of the device architecture, Figure 20b shows a 3D cross-sectional view of the thin film vertical arrangement at the active region (*i.e.*, the location where all layers overlap) considering two source perforations. From bottom to top, our device has the following structure: gate electrode (Cr), gate dielectric (Al_2O_3), patterned-source electrode ($Cr/Au/SiO_2$), OSC thin film, and rolled-up drain electrode ($Au/Ti/Cr/SiO_2$).

Crucially different from conventional VOFET architectures [24,25,66,67], in the r-VOFET platform, the patterned source-electrode with rectangular perforations is the alternative to lessen the electrode screening effect, allowing both the gate field penetration and the current modulation at the semiconducting channel. Accordingly, as proposed by Nawaz *et al*. in 2020, this feature also allows one to control the current density distribution along the channel. They reported high current density concentrated close to the source edges or at the center of the perforation depending on the source perforation geometry (as demonstrated in Figure 12) [21].

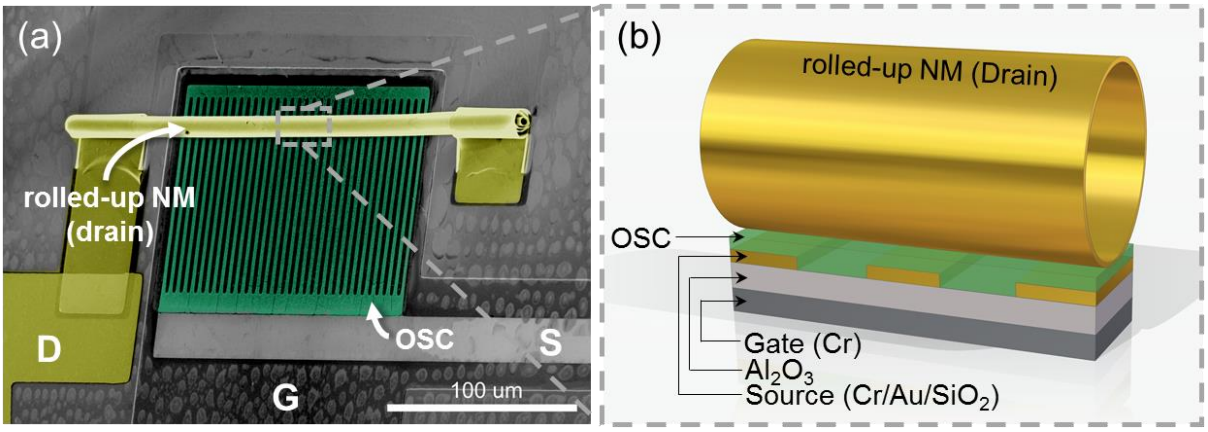


Figure 20. Fully fabricated r-VOFET. (a) False-color SEM image emphasizing the main features of the r-VOFET platform: the patterned source with rectangular perforations (9 μm gap), and the rolled-up drain electrode. (b) The 3D cross-sectional view provides a clear visualization of the device architecture and the rolled-up NM soft contact with the OSC layer.

The main limitation observed for the r-VOFETs reported by Nawaz *et al*. was the relatively low *on/off* ratio ($<10^2$), although this is in accordance with previous studies employing pristine copper phthalocyanine (CuPc) as the transistor semiconducting channel [66,111,112]. Hence, our first attempt to improve device performance was to incorporate a high-mobility OSC. A detailed discussion of the findings employing this approach is given in the following section.

4.2. DNTT AS SEMICONDUCTING CHANNEL OF THE r-VOFET PLATFORM

Prior to evaluating our r-VOFET performance employing a different OSC as the semiconducting channel, it is worth restating the platform mechanism of operation to better understand how such modification might impact the electrical characteristics. To illustrate the vertical-transistor operation as well as the formation of the vertical conducting channel, Figure 21a shows a 3D cross-sectional view of the r-VOFET for a single source perforation while bias application. Specifically, the representation depicts the edge-driven operating mechanism, as proposed by Nawaz *et al*. in 2020 [21]. According to their findings, a high

current density (*i.e.*, the formation of a vertical conducting channel within the VOFET semiconductor bulk) can be observed concentrated close to the source edges (edge-driven effect) or at the center of the perforation (tunnel effect) depending on the source geometry [21,71]. Regarding the use of a high-mobility OSC, it may cause an increase in I_{ON} as well as I_{OFF}, thereby not affecting the *on/off* ratio significantly.

Moreover, on account of being an SB-VOFET, the principle of operation is based on gate voltage V_{GS} application that results in an effectively Schottky barrier modulation (*i.e.*, reducing the energy mismatch between source-electrode work function and the OSC HOMO/LUMO level), thus switching on the device. Hence, the charge injected from the source electrode accumulates close to the perforation edge at the gate dielectric interface, forming a virtual contact. With the simultaneous application of V_{DS}, a vertical channel toward the drain electrode is formed from this virtual contact [32,64,65]. In this case, the OSC HOMO/LUMO levels and the source-electrode work function will dictate the I_{OFF}, and this can influence the *on/off* ratio.

Having defined the device mechanism of operation, let us now turn to the r-VOFET semiconductor channel. In our devices, we employed a dinaphtho[2,3-b:2′,3,-f]thieno[3,2-b]thiophene (DNTT) thin film (the chemical structure is shown in Figure 21b inset). DNTT is an air-stable high-mobility small molecule, *i.e.*, it operates under ambient conditions without degradation and shows excellent p-type transport with mobilities usually $>10^{-2}$ cm²/Vs [69,113–115], thus it is widely used as the active layer of state-of-the-art organic transistors [69,113,114,116–119].

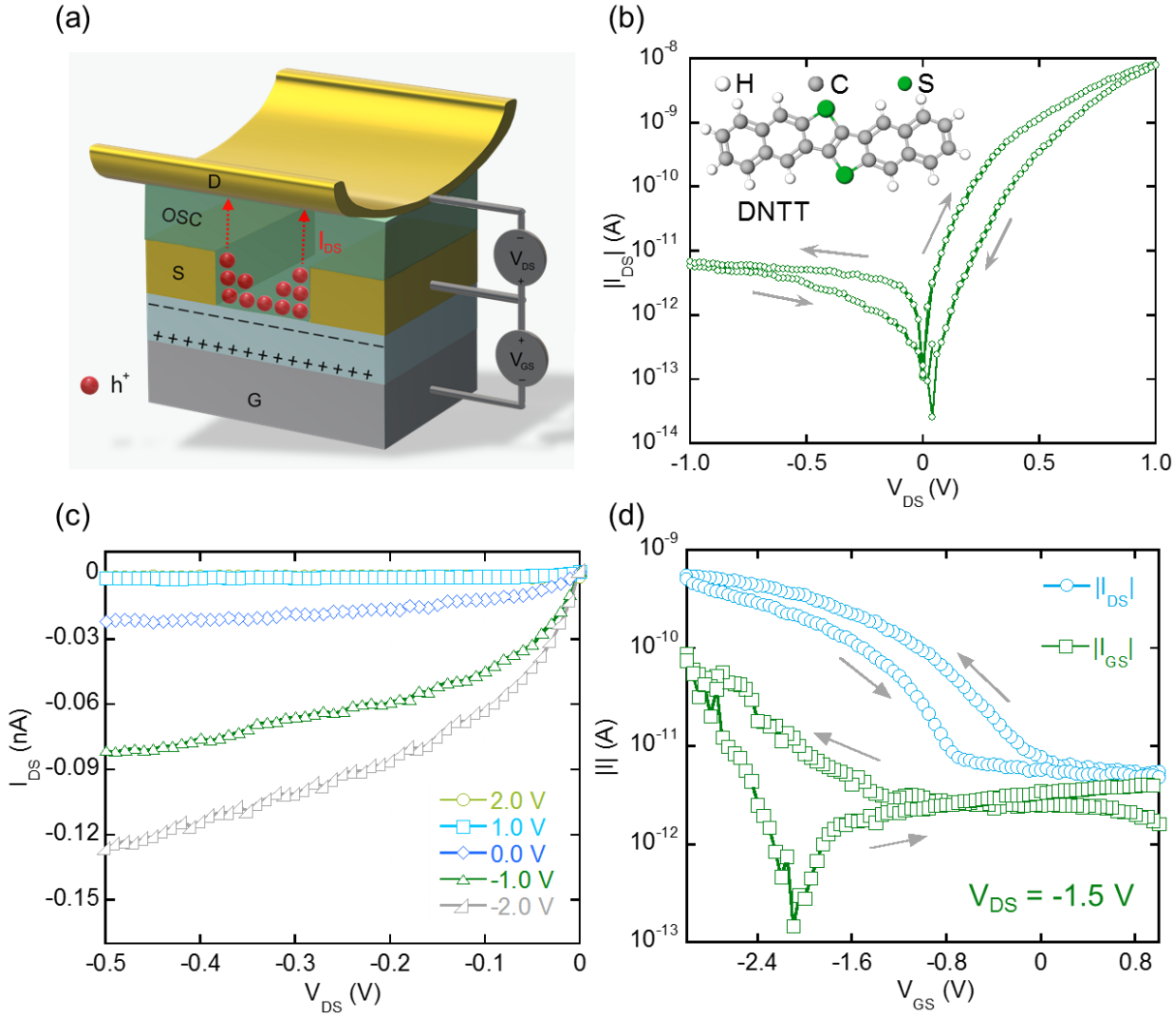


Figure 21. Electrical characterization of DNTT-based r-VOFETs. (a) Schematic representation of the r-VOFET operation considering a single source perforation (two source edges). (b) $|I_{DS}|$ *vs.* V_{DS} characteristics for a floating gate. The arrows indicate the voltage sweep direction. Inset: DNTT chemical structure. (c) Output curves (I_{DS} *vs.* V_{DS}) at different V_{GS} values. (d) Transfer characteristics ($|I_{DS}|$ *vs.* V_{GS}) at V_{DS} = -1.5 V. The respective gate leakage curve is also shown, whereas the arrows denote the hysteresis behavior.

To investigate the electrical characteristics of our DNTT-based devices, we performed an output characteristics measurement ($|I_{DS}|$ *vs.* V_{DS}) with a floating gate (Figure 21b). The r-VOFET diode part (rolled-up drain electrode/DNTT thin film/patterned source electrode) presents a current-rectifying behavior (*i.e.*, very low I_{DS} for $V_{DS} < 0$). Several factors could explain this observation. Firstly, we could attribute this result to the fact that although there is not a large energy mismatch between the Au/DNTT contact (Au work function of 5.1 eV [3] and DNTT HOMO level of 5.4 eV [115]), our source electrode is a combination of Cr/Au/SiO_2,

thus indicating a possible contribution of the Cr/DNTT contact (Cr work function of 4.5 eV [3]). Another alternative explanation is that it is due to a high density of charge carrier traps at the source/OSC interface, thereby affecting charge carrier injection (*i.e.*, altering the injection mechanism because of increased contact resistance) [51]. We believe a possible source for these traps might be the multiple fabrication steps and exposure to solvents, water (H_2O), oxygen (O_2), light, temperature, etc.

Figure 21c shows the output curves (I_{DS} *vs.* V_{DS}) at different V_{GS} values (from +2 V to -2 V). As expected, our DNTT-based devices show a typical p-type behavior and remarkably low operating voltages. Also, these results are in agreement with Nawaz's (2020) findings which showed output curves presenting saturation tendency. VOFET devices are known for not showing saturation in the output characteristics caused by the short-channel effect [4,31,65]. Meanwhile, by covering the top source facets with a SiO_2 thin film, we restrained current injection only in the lateral parts of the source in the same way as demonstrated previously for CuPc-based r-VOFETs [21].

As can be seen from Figure 21d, a gate sweep performed for fixed V_{DS} = -1.5 V resulted in an *on/off* ratio ~10^2, which is far below those observed by previous studies employing DNTT-based OFETs (10^3-10^7) [69,77,113,117,120]. We attribute this low current amplification to an inefficient charge accumulation at the OSC/dielectric interface, thus limiting the charge carrier density necessary to create the virtual contact and vertical conducting channel. It is difficult to explain this result, but it might be related to the large gate-leakage current ($|I_{GS}|$): in the off state $|I_{GS}| \approx |I_{DS}|$, and in the on state $|I_{GS}|$ is only an order of magnitude lower than $|I_{DS}|$. This level of leakage current may be due to the gate dielectric thickness (~20 nm thick Al_2O_3 film) and the large intersection area between gate and source electrodes (this issue is discussed further in the following section).

If we now turn to the significant hysteresis observed in Figure 21d, it is explained by the presence of traps in the semiconductor bulk or at the semiconductor/dielectric interface. During the forward voltage sweep, some charge carriers are trapped, thereby contributing to a differential current in the reverse voltage sweep [51,54,61]. There are two likely causes for this behavior: the device fabrication process and the conducting channel formation. Due to the complex architecture, VOFETs require more lithography steps and consequently are more often exposed to multiple solvents and water that generate additional trap states on the OSC and dielectric thin films. Also, the channel transport is no longer restricted to the OSC/dielectric interface, but rather becomes distributed along the OSC volume. Therefore, improving OSC crystallinity and passivation of dielectric surface are approaches largely employed to suppress charge trapping, thus lessening hysteresis [61,62]. Recently, Chang, J. F., and coworkers demonstrated that the dielectric interface modification employing self-assembled monolayers (SAMs) improves VOFET performance by enhancing DNTT mobility and lessening hysteresis. In their study, the unmodified device exhibited the largest hysteresis as well as the lowest mobility (0.7 $cm^2\ V^{-1}s^{-1}$), indicating the presence of a large number of trap states. In contrast, the SAM-modified devices exhibited smaller hysteresis along with enhanced mobility (~4.0 cm^2/Vs) [69].

In summary, our findings agree with those observed by Nawaz, *et al*. for the CuPc-based r-VOFETs: the DNTT-based devices exhibit remarkable low operating voltage (<-3 V) as well as a saturation tendency for output characteristics. However, our devices still show inferior performance when compared to the state-of-the-art VOFETs (*viz.* relatively low *on/off* ratio, high gate-leakage current (up to 10^{-10} A), and significant hysteresis). Therefore, the following section moves on to discuss some approaches to circumvent these limitations.

4.3. r-VOFET FABRICATION OPTIMIZATION

We performed some modifications to the r-VOFET platform by employing engineering approaches, such as low-cost processing and batch fabrication (*i.e.*, microfabrication and strain-engineering techniques), aiming to address the shortcomings outlined previously. Hence, the following part moves on to describe in greater detail the procedures and methods used in this investigation and the main findings.

The first attempt was focused on lessening the gate-leakage current. Besides the small r-VOFET injection area (reported by Nawaz *et al.*, to be $A_{geo} \approx 1.3 \times 10^{-6}$ cm^2 [21]), the main difficulty in achieving high I_{DS} values is likely a result of the substantial gate-leakage current observed. This discrepancy could be attributed to the large intersection area between gate and source electrodes (the Cr thin film employed as gate electrode covers the whole *mesa* structure, including both gate and source pads, as shown in the optical microscopy image in Figure 22a), and to the gate dielectric layer thickness (20 nm thick Al_2O_3 thin film).

Therefore, the first architecture modification employed was limiting the gate-source intersection area to only the device's active region. Figure 22b demonstrates this modification, the *mesa* structure was patterned on the Si/SiO_2 substrate with anisotropic SiO_2 etching (down to 190 nm), and afterward, we deposited a 15 nm thick Cr film only over the region designated for the gate pad. Such an approach resulted in a reduction of 82% of the gate-source intersection area. The other modification was using a thicker gate dielectric layer: 20 nm to 30 nm thick Al_2O_3 film.

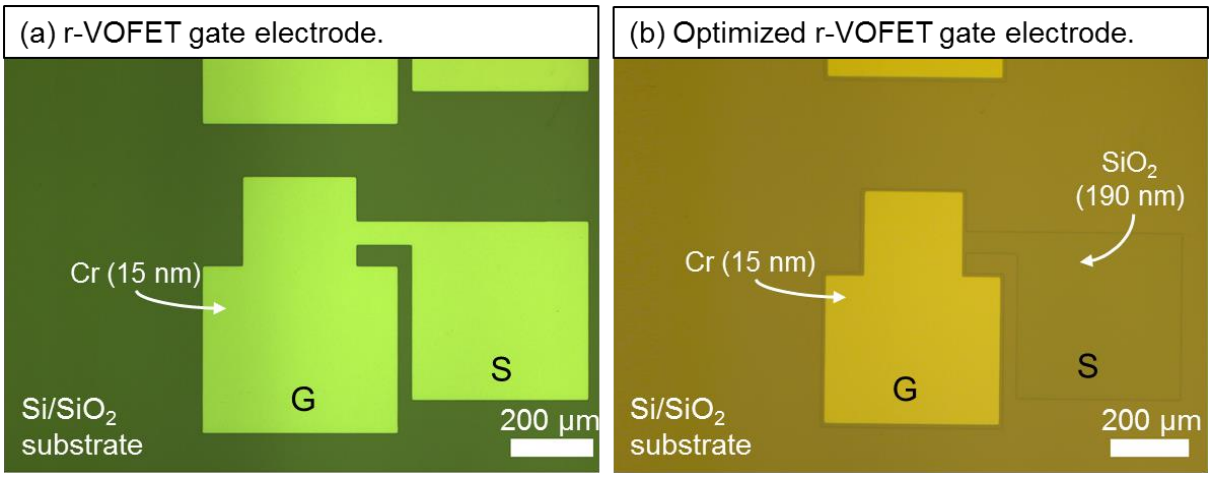


Figure 22. Study for lessening gate-leakage current. (a) Optical microscopy image of the gate electrode based on the study proposed by Nawaz *et al.* [21], Cr thin film was deposited over the whole *mesa* structure, including both gate and source pads. (b) Optical microscopy image of the optimized gate electrode, Cr thin film is deposited only over the gate pad.

The second strategy that we proposed was the modification of the patterned source electrode. To ensure an effective current modulation in the VOFET architecture, it is of tremendous importance to employ a source electrode that shows some level of permeability to the gate electric field [4,31,32]. Taking this variable into account, Nawaz and coworkers proposed for the r-VOFET platform a novel source-electrode concept, the patterned source electrode with identical rectangular perforations defined by photolithography-assisted patterning [21]. This strategy allows more careful control over the electrode shape and dimensions and guarantees that the rolled-up drain tube overlaps the whole source-electrode length evenly (including metal stripes and perforations).

Figure 23a shows an optical microscopy image for this rectangular-patterned source electrode based on the study proposed by Nawaz *et al*. [21]. In this case, the electrode has dimensions for length (*a*) and width (*b*) of 248 µm and 132 µm respectively. Also, these devices employed perforations of $L_P \approx 9$ µm as well as source electrode stripes of $L_S \approx 9$ µm (as shown in the zoom-in image), resulting in $n_{SE} = 26$.

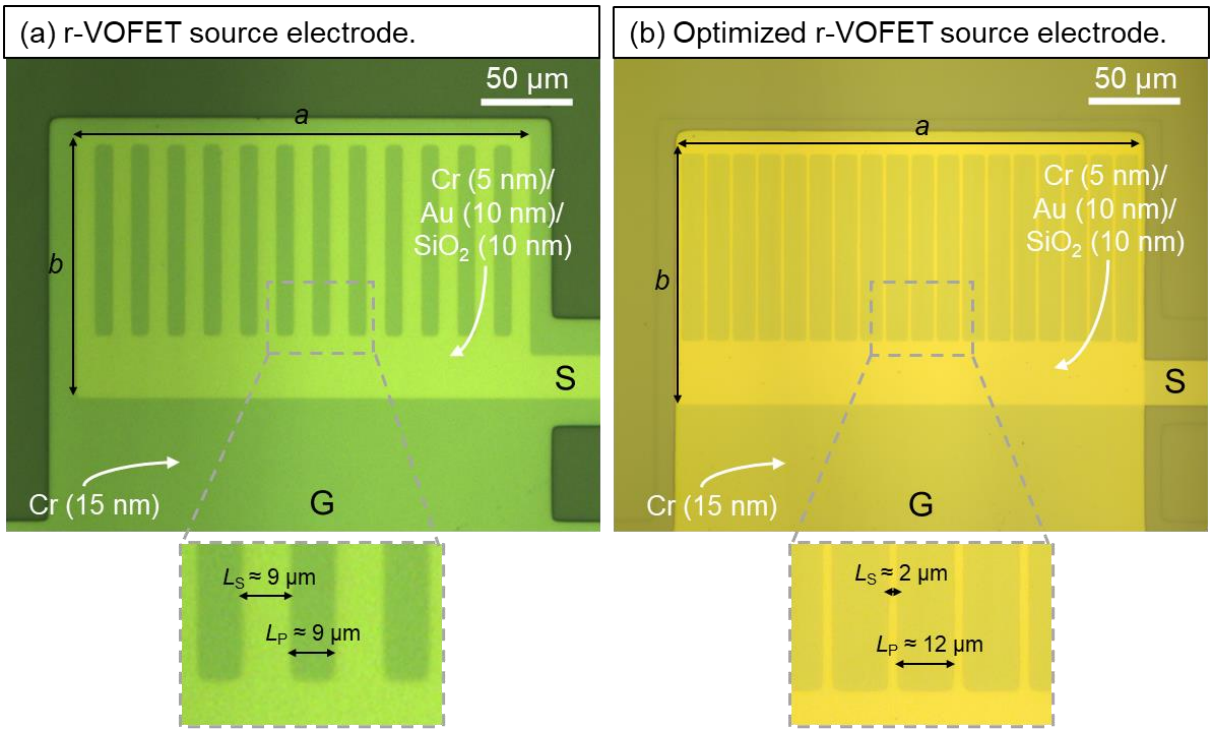


Figure 23. Patterned source electrode optimization for study of edge-driven effect. (a) Optical microscopy image of source electrode based on the study proposed by Nawaz *et al.* [21]. This patterned source electrode has 26 source edges and dimensions of $a \approx 248$ µm and $b \approx 132$ µm. The inset is a zoom-in image showing the dimensions for source electrode stripes and perforations ($L_S \approx L_P \approx 9$ µm). (b) Optical microscopy image of the optimized source electrode. This patterned source electrode has 38 source edges and dimensions of $a \approx 250$ µm and $b \approx 143$ µm. The inset is a zoom-in image showing the dimensions for source electrode stripes ($L_S \approx 2$ µm) and perforations ($L_P \approx 12$ µm).

In order to study the edge-driven operating mechanism, it was necessary to take both n_{SE} and the Fill Factor value (*FF*) into account, so it would be possible to assess more information about the source electrode. As previously stated, the *FF* parameter was first defined by Ben-Sasson *et al*. in 2011 [65], which is the ratio between the total area of source perforations and the source-electrode total area, thus it measures the source electrode "permeability" to the gate electric field. Ben-Sasson *et al*. investigated the operation of a patterned electrode VOFET fabricated using block copolymer lithography (source electrode with nano perforations). They proposed that for devices with larger source perforations and increasing *FF* values, a more efficient barrier modulation is observed due to the reduced influence of lateral electric fields from source electrode edges, thus facilitating current injection into the semiconductor [65].

Compared to conventional VOFETs [23–25,69,121,122], the effective injection area in the r-VOFET platform is not the same as the patterned source-electrode total area. This area is defined by the mechanical contact between the rolled-up drain electrode and the OSC thin film, which is highly dependent on the electrode and OSC's topography [21,27,28]. Hence, it is of fundamental importance to adapt the *FF* parameter taking into consideration this r-VOFET feature. Consequently, the n_{SE} and *FF* values were calculated for our devices as shown in the following equation [65]:

$$n_{SE} = (n_P \times 2) + 2 \quad \text{(VIII)}$$

$$FF = \frac{n_P \times L_P}{a} \times 100\% \quad \text{(IX)}$$

Where n_P is the number of rectangular source perforations. When we employed Equation IX for the patterned source electrode shown in Figure 23a (n_{SE} = 26), we obtained *FF* ≈ 45%. However, the main disadvantage of employing this patterned source electrode structure (*viz.* $L_S = L_P$) is that it fails to provide a high variation in *FF* when varying n_{SE}, *i.e.*, for a source electrode with the same *a* but $L_S = L_P$ =3 μm, n_{SE} = 83 and *FF* ≈ 50%.

Therefore, we fabricated devices employing rectangular-patterned source electrodes with different perforation sizes (~L_P = 12, 8, 6, 3, and 2 μm). An example is shown by the optical microscopy image of a patterned source electrode with $L_P \approx 12$ μm and n_{SE} = 38 (Figure 23b). Despite the different perforation sizes, it is worth mentioning that the electrodes still maintained the same length and width regarding both the electrode active region (*viz.* *a* ≈ 250 μm and *b* ≈ 143 μm) as well as the electrode stripe length ($L_S \approx 2$ μm). These aspects guaranteed r-VOFETs with the following features as shown in Table 1:

Table 1. List of the patterned source electrode features employed to study the r-VOFET operating mechanism.

n_P (#perfurations)	18	25	31	50	62
n_{SE} (#edges)	38	52	64	102	126
***FF* (%)**	87	79	74	54	45

The last modification in the r-VOFET fabrication was the roll-up process calibration. Figure 24a shows optical microscopy images for the roll-up process proposed by Nawaz *et al*. [21]: (a.1) sacrificial layer etching and strained layer release that is limited by the trench structure; (a.2) trench structure removal and roll-up process end with the rolled-up NM reaching the transistor active region. This method's reproducibility yielded a 75 ± 13% rate of fully fabricated r-VOFETs per chip.

However, when the original r-VOFET fabrication process has undergone gate- and source-electrode modifications to improve device performance, the roll-up process proved to be inefficient. We observed a drastic drop from ~75% to 0% reproducibility rate. As a result, the roll-up process was adapted according to these architectural modifications as demonstrated in Figure 24b. To ensure the required strain gradients during the roll-up process (Figure 24b.1) as well as the subsequent formation of the vertical contact between rolled-up NM and the DNTT thin film (Figure 24b.2), we changed the following features: (i) the shape and dimensions of sacrificial, strained, and anchor layers; (ii) the anchor layer was defined during the step for drain pad and electrical contacts (gate and source pads), and (iii) a roll-up solution with half of the concentration of H_2O_2 (*i.e.*, H_2O:0.00125 H_2O_2).

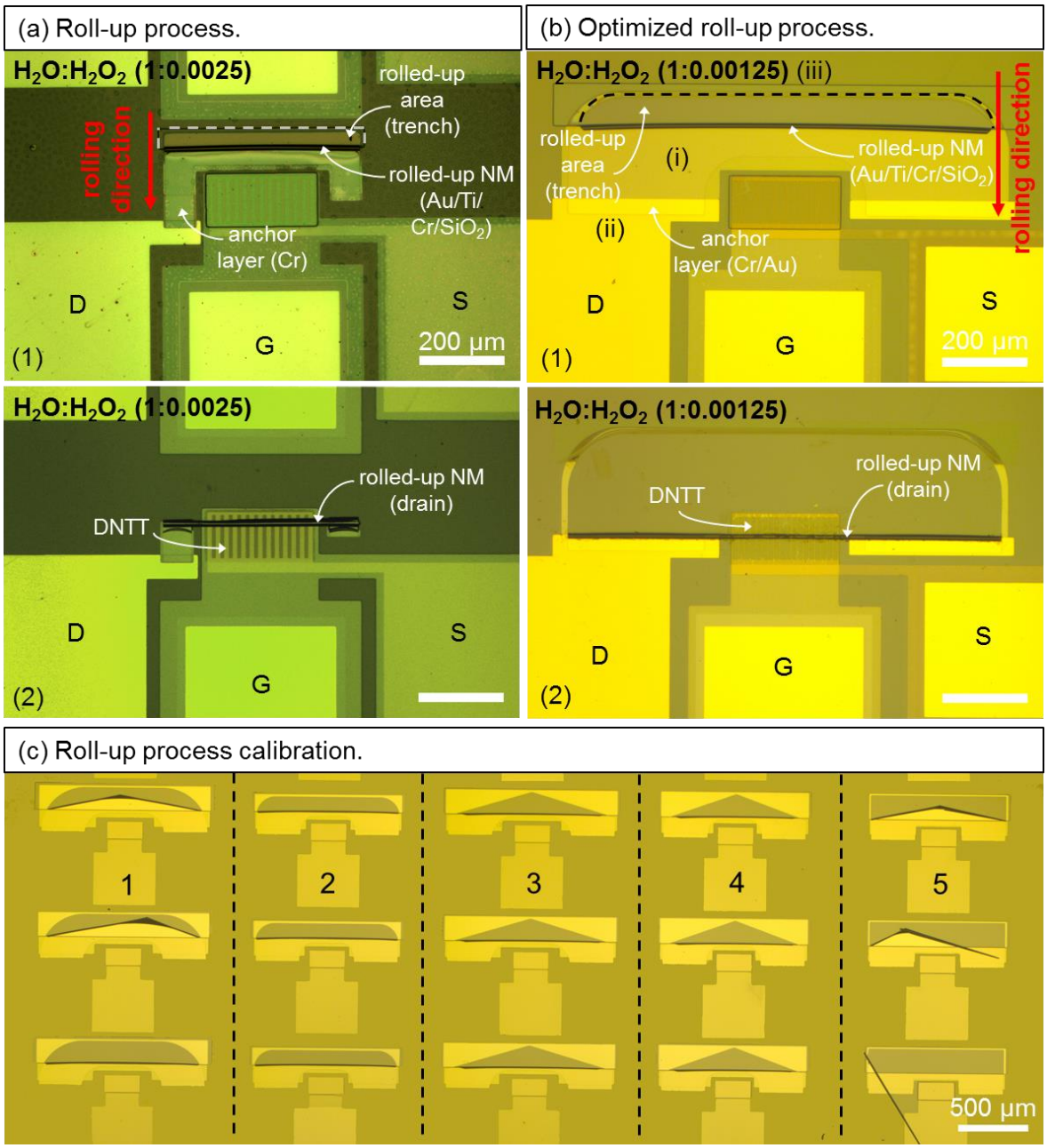


Figure 24. Study for increasing the roll-up process reproducibility. Optical microscopy images showing an r-VOFET during the roll-up process based on (a) the study proposed by Nawaz *et al.* [21], and (b) optimized r-VOFET architecture. (c) Optical microscopy image showing the roll-up process calibration employing five different structure shapes for the sacrificial and strained layers.

We carried out a study employing different shapes and dimensions for the sacrificial and strained layers in order to assess which combination would be best to improve our roll-up process effectiveness and viability. Figure 24c shows an optical microscopy image of the result obtained for this roll-up process calibration. In the same chip, we tested five different shapes

and dimensions for sacrificial (Ge) and strained (Au/Ti/Cr/SiO_2) layers. The results of this study demonstrate that NMs 2, 3, and 4 have improved reproducibility (~100% rate), while NMs 1 and 5 show problems forming a tube-like structure and reaching the trench inferior edge. Overall, to decide between options 2, 3, and 4, we have taken into consideration that the NMs with triangular shape exhibit considerable radius variations along the tube length. Therefore, we chose structure number 2 to be employed in our optimized devices (as shown in Figure 24b), which provided a 65 ± 16% rate of fully fabricated r-VOFETs per chip.

The strategic changes in the roll-up process not only consider the reproducibility but also accounts for enabling device performance improvement by employing approaches to control OSC crystallinity as well as the dielectric surface passivation (*e.g.*, the SAM modification) [69,116,123]. A drawback in the r-VOFET platform when modifying the gate dielectric surface, it is not possible to define the trench structure using a photolithography step before the roll-up process. In this scenario, the SAM molecules would be exposed to UV light and multiple chemical processes, thereby changing the passivation properties. With that in mind, our roll-up process calibration study has made a substantial contribution to addressing this issue: the proposed NM structures ensure the required strain gradients for a roll-up process with enhanced reproducibility without the trench structure definition. Hence, our findings circumvent this issue and allow SAM modification in future studies.

Together these modifications provide a device as shown in Figure 25a, a CLS microscopy image (top view) of a fully fabricated r-VOFET. Additionally, in order to investigate the topography of our patterned source electrode (*i.e.*, the transistor active region), we carried out AFM measurements before (Figure 25b) and after (Figure 25c) the deposition of the DNTT thin film. The patterned source electrode displayed an average roughness (*RMS*) of 2.2 ±0.4 nm for both the SiO_2-covered source stripe and the Al_2O_3 thin film at the source perforation.

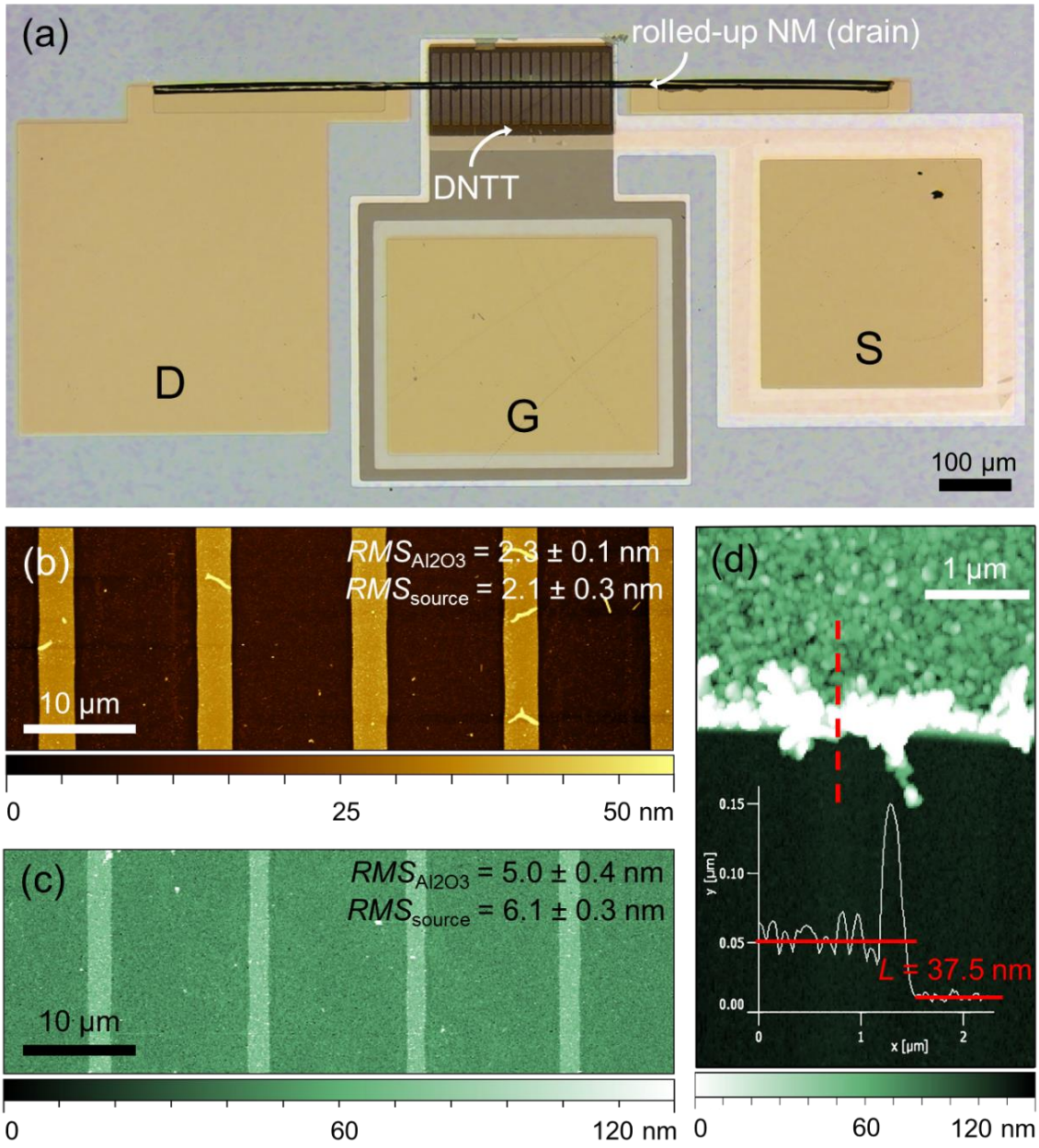


Figure 25. Optimized r-VOFET platform. (a) CLS microscopy image of a fully fabricated r-VOFET with a source electrode of 38 edges. AFM images of the patterned source electrode active region (b) before and (c) after the deposition of the DNTT thin film. (d) DNTT thin film topography acquired by AFM. The inset shows the measured step height profile along the dashed line. Adapted from submitted manuscript ref [110].

On the other hand, after the deposition of the DNTT thin film, the *RMS* roughness acquired over the source stripe and source perforation are approximately 6.1 ± 0.3 nm and 5.0 ±0.4 nm, respectively. These findings suggest that the DNTT film may exhibit different molecular packing depending on the device counterpart surface it is grown. Such a structural

difference along the DNTT semiconducting channel may impact the r-VOFET's electrical properties (*e.g.*, charge carrier mobility, transconductance, gain, among others) [61,62].

Turning now to the experimental evidence on our r-VOFET's conducting channel length, *L*, Figure 25d exhibits the AFM topography image acquired from the DNTT thin film that was deposited at the device active region. The measured step height profile revealed that the DNTT thin-film thickness is 37.5 nm (*i.e.*, *L*), as shown in Figure 25d inset. Also, one may observe there are homogeneously distributed DNTT aggregates on the thin-film surface, resulting in the topography smooth variation.

The findings in this section demonstrate that with a few architectural modifications to improve the r-VOFET performance, it was necessary to adapt some processes to accommodate those changes effectively. The next sections, therefore, move on to discuss the electrical characterization of these optimized r-VOFETs and the platform application as a phototransistor.

4.3.1. Electrical Characterization

Based on these findings, here we provide some experimental evaluation of the optimized r-VOFETs' electrical characteristics. Prior to commencing this study, a method was used to normalize the differences in the experimental data. We observed a noticeable difference in I_{DS} values for devices employing a source electrode with the same n_{SE} (and *FF*). We believe that the main reason for these discrepancies is associated with the r-VOFET injection area as illustrated in Figure 26a. The effective injection area obtained from the mechanical contact is highly determined by the rolled-up NM and DNTT's roughness [21,27]. Hence, considerable variations in I_{DS} might be found for devices with the same architectural features because of topography differences.

Turning now to the patterned source electrode influence, Figure 26b provides a correlational analysis of the r-VOFET injection area as a function of n_{SE}. The injection area was calculated by the relation $J \alpha E$ used to describe the electrical current in a diode [3,27]. First, we determined the current density and the electric field considering a planar OFET with the following specs: 30 nm of DNTT thin film, conducting channel dimensions of L = 20 µm and W = 166 µm, and biasing conditions of V_{GS} = 0 V, V_{DS} = 1 V, and I_{DS} = 0.41 pA. Once a correlation was found, we determined the current density for our r-VOFETs with different n_{SE} values and a biasing condition of V_{GS} = 3.6 V and V_{DS} = 3.6 V. The results were then used to acquire the mean injection area and the respective standard error (Figure 26b).

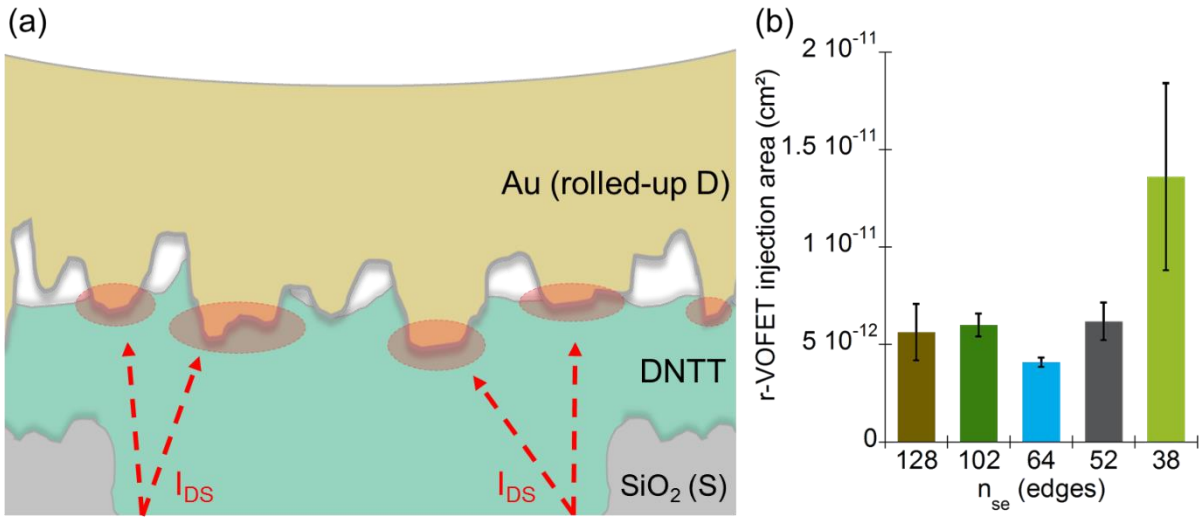


Figure 26. (a) Schematic cross-sectional view of the rolled-up NM vertical contact with the semiconducting layer at the r-VOFET active region. The representation illustrates the drain electrode and the DNTT thin-film roughness and how it affects the injection area. (b) r-VOFET injection area as a function of n_{SE}.

Overall, in the study of the r-VOFET injection area as a function of n_{SE}, the only notable difference is observed for n_{SE} = 38, and it is not possible to draw any strong conclusions about the relationship between those parameters. Further experiments, using a broader range of samples, would be necessary to provide more definitive evidence.

To investigate the edge-driven operating mechanism demonstrated by Nawaz *et al.* [21], we fabricated r-VOFETs with five different n_{SE} and *FF* values as shown in Table 1.

Figure 27a exhibits optical microscopy images of these studied source electrodes. Because of the high variation for injection area, the error bars were significantly large for I_{DS} values. When the data are normalized using this consideration, these errors are largely reduced as reported in Figure 27b, which shows the output characteristics (I_{DS} *vs.* V_{DS}) at different gate voltages (from +3.6 V to -3.6 V) for different n_{SE} values. We found that the optimized DNTT devices displayed clear saturation tendency, low operating voltages (<5 V), and effective current modulation with increasing V_{GS}. These observations are consistent with the results reported for the old architecture.

In the case of the transfer characteristics (Figure 27c), the results surpass Nawaz's work [21] and our old DNTT devices in terms of lower hysteresis and higher *on/off* ratio (~10^4-10^5). Furthermore, we also presented a remarkable improvement in gate-leakage current, reducing it by around two orders of magnitude, thereby showing that the changes in the device architecture were effectively suitable.

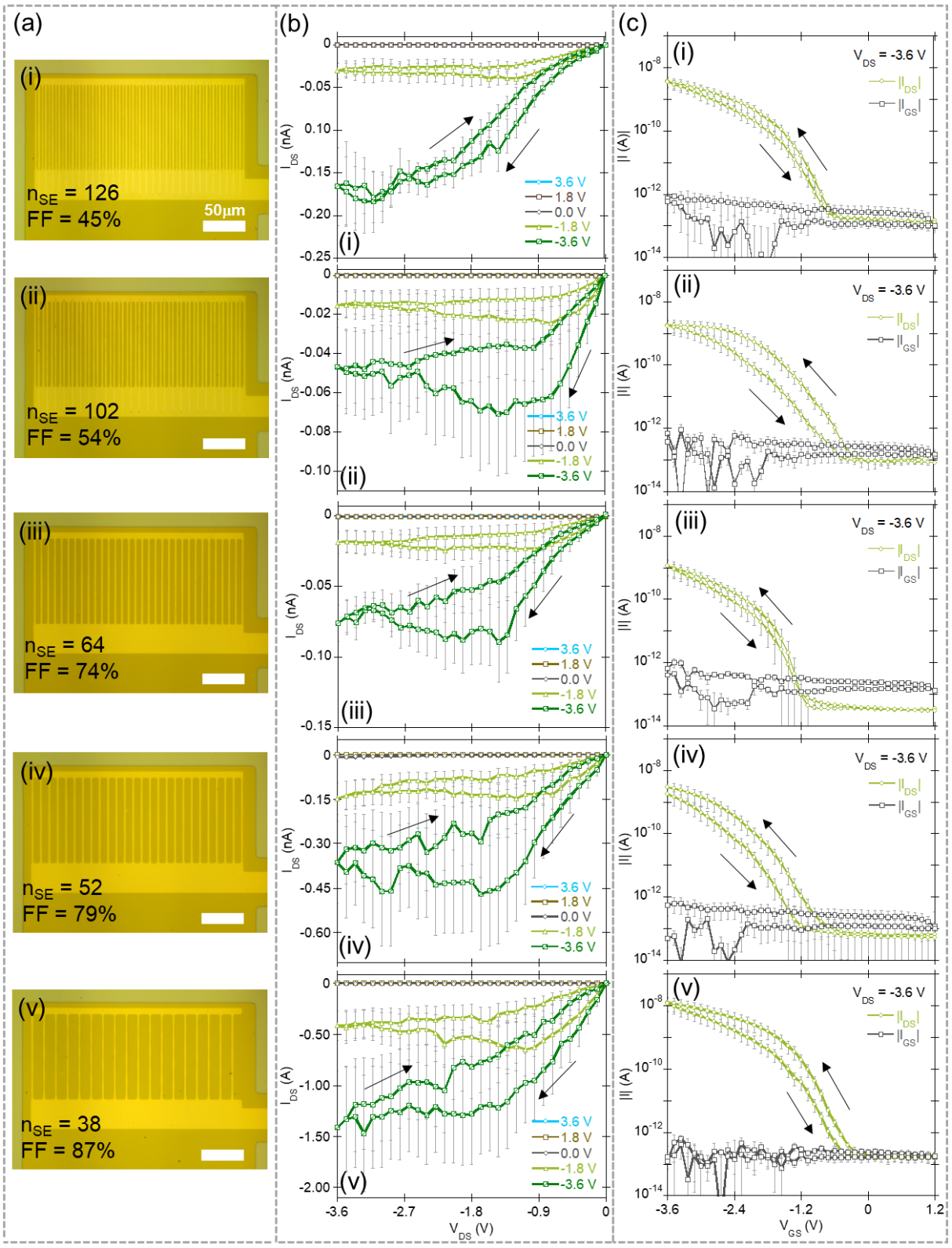


Figure 27. Optimized r-VOFET electrical characterization. (a) Optical microscopy images of different rectangular-perforation source electrodes having (i) 38, (ii) 52, (iii) 64, (iv) 102, and (v) 126 edges. (b) Output characteristics curves (I_{DS} *vs.* V_{DS}) measured for the same n_{SE} values shown in (a), at different V_{GS}. (c) Transfer characteristics (log|*I*| *vs.* V_{GS}) measured for the same n_{SE} values shown in (a), at V_{DS} = -3.6 V. The respective gate-leakage current ($|I_{GS}|$) is shown in panel (c), whereas the arrows denote the hysteresis direction. Adapted from submitted manuscript ref [110].

To determine whether the n_{SE} value (or *FF* value) affects the r-VOFET performance, we estimated the performance parameters assuming the standard Shockley FET equations, which are applicable when the transfer characteristics show a linear dependence for $I_{DS}(V_{GS})$ in the linear regime and $|I_{DS}|^{1/2}(V_{GS})$ in the saturation regime respectively, otherwise, parameter extraction is not accurate [54,55]. Figure 28a shows the transfer curves measured for fixed V_{DS} = -0.5 V (linear regime) and V_{DS} = -3.6 V (saturation regime), comparing devices with different n_{SE} values. The red lines correspond to extended linear fits. Despite some nonlinearities (*e.g.*, substantial threshold voltage and an I_{DS} plateau for high V_{GS} values) and additional uncertainties for vertical architectures due to short-channel effect, contact resistance and the conducting channel formation, all devices fulfill a linear current-voltage relation. Therefore, the extended linear fits for experimental data at the linear regime were employed to extract performance parameters such as g_D, g_m, and $W\mu C$ (Equation I), and at the saturation regime to determine V_{th} (Equation II). These criteria were used to rule out the possibility of non-uniformity of charge distribution along the conducting channel (effect observed in the saturation regime) and the considerable contact resistance contribution in vertical architectures compared to channel resistance (shorter channel lengths), which can disturb the current-voltage linear relation [31,53,55].

The results acquired from the linear fits, the performance parameters (i) intrinsic gain (g_m/g_D); (ii) $W\mu C$; (iii) V_{th}; and (iv) *on/off* ratio, are presented in Figure 28b. They are plotted as a function of n_{SE} and reported with the respective standard errors. Here we report the field-effect mobility values as the figure-of-merit $W\mu C$ because of our distinct device architecture. When we turn to gain and the *on*/*off* ratio (*i.e.*, the transistor amplification factors), both performance parameters have average values of around 10^4, showing a quite small variation with the values that fall within the error bars. Meanwhile, $W\mu C$ values present larger variations for different n_{SE}, and the reported errors are relatively more significant. Hence, it is not yet clear

whether n_{SE} and *FF* are responsible for the variation reported for these parameters and to what extent.

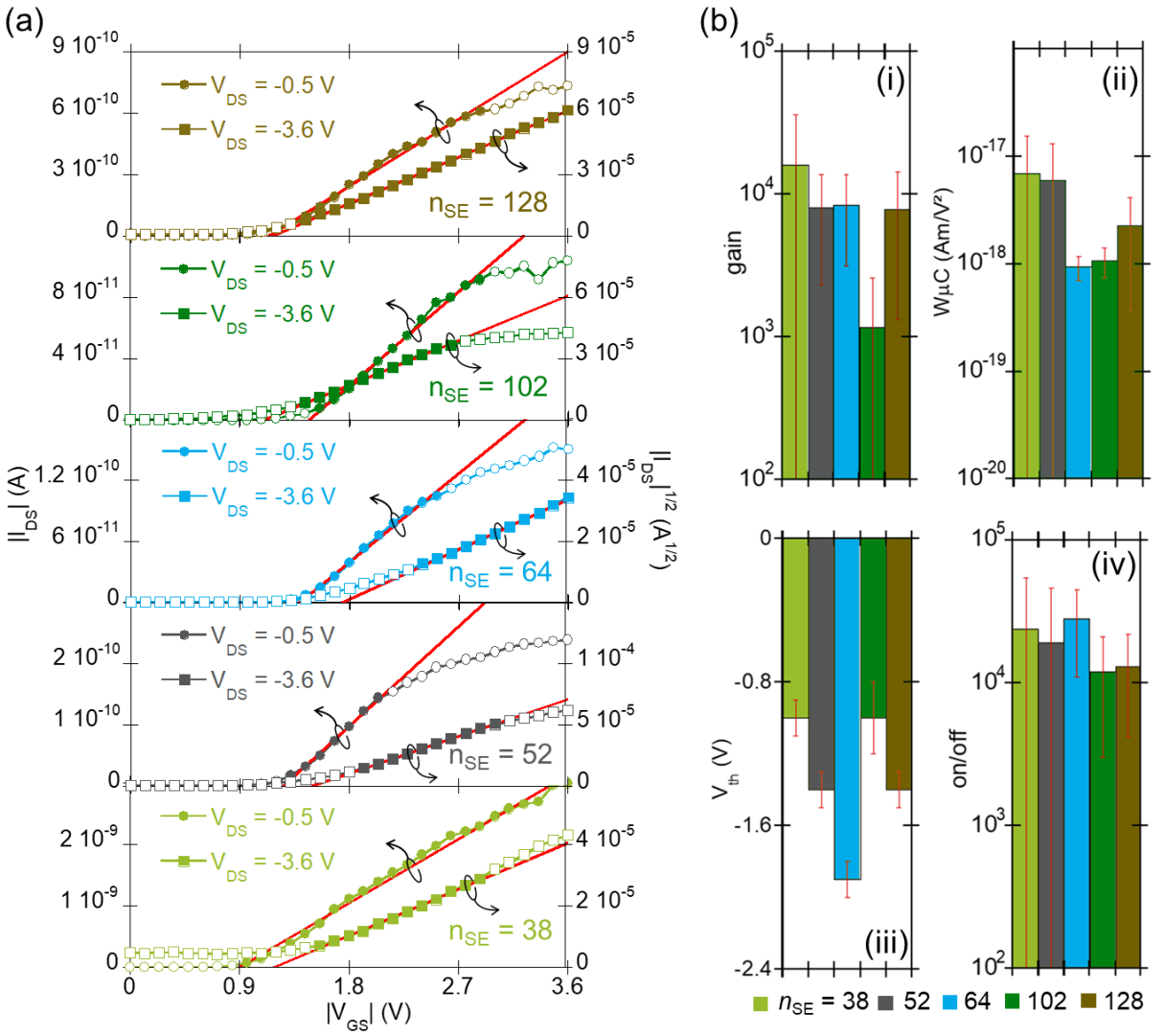


Figure 28. Extraction of performance parameters employing Shockley FET equations for the optimized r-VOFETs with non-ideal characteristics. (a) Forward transfer curves for devices with different n_{SE} values in the linear regime (V_{DS} = -0.5 V) and in the saturation regime (V_{DS} = -3.6 V), both in linear-scale plots. A linear fit (red line) based on the Shockley model ($|I_{DS}|(|V_{GS}|)$ and $|I_{DS}|^{1/2}(|V_{GS}|)$ respectively) was employed to estimate performance parameters. (b) Performance parameters for r-VOFETs with different n_{SE} values. Adapted from submitted manuscript ref [110].

The most surprising aspect of the data demonstrated in Figure 28b is the correlation found between V_{th} and n_{SE}. r-VOFETs employing source electrodes with larger n_{SE} (and consequently lower *FF*) show a slight increase in V_{th} values. This is explained by the decrease in the source electrode permeability to the gate electric field, thereby resulting in a less effective

barrier lowering for current injection into the semiconductor [65]. However, one unanticipated finding was that V_{th} starts dropping for n_{SE} = 102 edges, suggesting that likely there is a transition in the operating mechanism, the same observed by Nawaz (2020), in which n_{SE} affects the formation of the vertical conducting channel [21]. Therefore, it could conceivably be hypothesized that an operating mechanism transition occurs from 'edge-driven effect' to 'tunnel effect', implicating that V_{th} might be affected differently by factors such as the trap density and the injection barrier lowering at each case [54,61].

Overall, the reported findings reveal several notable strengths of this work such as the enhanced performance that was achieved by architectural modifications and the improved reproducibility in device fabrication and electrical characteristics. In order to compare quantitatively our r-VOFET performance with published works, we list some of them in Table 2. Our results showed some improvement over standard approaches, demonstrating impressive values for J_{DS} and *on/off* ratio that can be compared to several state-of-the-art VOFETs. The large J_{DS} (>10 A/cm^2) and the low operating voltage ($|V_{DS}| < 5$ V) are attributed to the reduced conducting channel length (L) and effective injection area (A), which are features in accordance with the fundamental idea behind the use of the vertical architecture for OFETs.

Moreover, the results obtained may have implications for understanding the edge-driven effect and its influence on the transistor operating mechanism. Our investigation showed a contrary outcome that differs from Nawaz's assumption [21] for the source edge-driven mechanism: no linear dependence between n_{SE} and I_{DS} is observed. We reported lower I_{DS} for devices employing source electrode with increasing n_{SE} value due to a decrease of permeability to the gate electric field (*i.e.*, lower *FF* value). Meanwhile, for devices with $n_{SE} > 102$ was observed an unexpected increase in I_{DS} and a drop in V_{th}, which we believe might be due to a transition in the operating mechanism ('edge-driven effect' to 'tunnel effect'), thereby, changing the source/OSC injection barrier lowering and vertical conducting channel formation.

Table 2. Summaries of VOFETs reported in literature employing different source electrode approaches.

Source electrode	OSC	*L* (nm)	*A* (cm²)	J_{DS} (A/cm²)	V_{DS} (V)	*on/off*	Ref
Photolithography patterned	DNTT	35	$\sim 1\times10^{-11}$	$\sim 1\times10^{3}$	-3.6	10^{4}-10^{5}	This work
Photolithography patterned	CuPc	35	1.3×10^{-8}	$\sim 1\times10^{-2}$	-1.0	10-10^{2}	[21]
Sn thin film	CuPc	80	4×10^{-2}	1.5×10^{2}	-5.0	~10	[66]
Ultrathin film	C_{60}[a]	90	2.5×10^{-3}	$\sim 4\times10^{-1}$	-4.0	$\sim 10^{6}$	[24]
Graphene	DPA[b]	100	3.8×10^{-5}	$\sim 5\times10^{-2}$	-5.0	$\sim 10^{5}$	[124]
Nanowires	P(NDI2OD-T2)[c]	~100	1×10^{-4}	1×10^{-3}	5.0	$\sim 10^{4}$	[22]
Nanowires	C_{60}	~120	4×10^{-2}	$\sim 1\times10^{-3}$	1.5	$\sim 10^{3}$	[67]
Nanosphere lithography patterned	DNTT	400	1×10^{-2}	$\sim 1\times10^{-2}$	-2.5	10^{4}	[69]

(a) Fullerene (C_{60}).
(b) 2,6-diphenyl anthracene (DPA).
(c) n-type semiconducting polymer.

However, this work is also limited by some aspects as the large variation in I_{DS} and the impossibility to extract some device architectural parameters due to the effective injection area that is determined by the rolled-up NM and DNTT's roughness. Therefore, this is only a limited study, and the full potential of the approach has not been proven. Future research should therefore seek to address this issue by employing a larger number of samples and different n_{SE} values, so several measurements can be done to reduce the uncertainties.

Furthermore, the devices with improved performance that we obtained by the optimized fabrication process proposed in this study, encouraged us to further investigate the r-VOFET architecture's remarkable features such as its multi-sensing capability reported by Nawaz *et al* [21]. The following section moves on to describe in greater detail an investigation of the r-VOFET potential when applied as a phototransistor.

4.3.2. The r-VOFET Platform as a Phototransistor

In 2020, Nawaz found clear variations in the I_{DS} values when investigating external stimuli response (exposure to humidity and light). The authors attribute these findings to the narrow effective contact between the rolled-up drain electrode and the top of the OSC thin film that facilitates direct interaction between external analytes and the device's active layer surface [21]. Here we investigate the r-VOFET photoresponse to obtain a further in-depth understanding of the illumination effect on the device operation and its potential in sensor technologies.

Phototransistors have become an attractive optoelectronic application for OFETs due to combining optical detection and signal amplification functionalities into a single device. The physical operation is based on light absorption, exciton formation, dissociation in additional free charge carriers, and amplification of the electrical signal [84,87]. However, compared to inorganic counterparts, OPTs still face challenges such as inefficient exciton dissociation with a high recombination loss. Great efforts have been made to address these problems. Initially, several OSCs have been widely designed and synthesized aiming for high light sensitivity and carrier mobility [95,125–128]. Another approach, thoroughly investigated in recent years, is exploring novel device architectures. In particular, vertical architectures show a combination of reduced channel length and large electric fields, thus enhancing the photoresponse [64,94,107,124]. Therefore, the concept of the r-VOFET platform seems promising to surpass the performance of state-of-the-art OPTs, owing to the ultrashort conducting channel (tens of nanometers) and facilitated external stimuli with the device's active layer.

Here, we provide some experimental evaluation of the photoresponse of r-VOFETs with different n_{SE} and *FF* values in order to identify the best combination for application as an OPT. We used the photosensitivity, *P*, as the figure of merit to quantify the photoelectric

response. To calculate this parameter for our devices, we carried out measurements of transfer curves with and without the illumination of blue light. Figure 29a shows the P values obtained as a function of V_{GS} for different n_{SE} values. From this graph, we extracted the maximum value of photosensitivity (P_{max}) for each n_{SE} value, as shown in Figure 29b. The results showed that our r-VOFET exhibited high photosensitivity (~10^4) and no significant variation of P_{max} for different n_{SE} values. The impressive photoelectric performance is attributed to the ultra-short channel length that reduces charge recombination and scattering by defects, and also it enhances exciton dissociation and charge separation due to higher electric field levels [99,103,107].

The only significant difference that stands out here is the V_{GS} value at which the P_{max} occurs. A steep shift towards V_{GS} = 0 V is observed for smaller n_{SE} and higher FF values, which is similar to that found for V_{th} values as a function of n_{SE}. Hence, we believe the same explanation is valid here, the higher permeability to the gate electric field that is observed for r-VOFETs with source electrode with lower n_{SE}. Such effect contributes to the source/OSC injection barrier lowering (*i.e.*, threshold voltage shift) and enhances the generation of photo-excited charge carriers, which increases the additional electrons that become trapped near the source electrode, thus also facilitating holes injection into the conducting channel [84,98,106]. Therefore, this data indicates that the r-VOFET with 38 edges demonstrates the best photoelectric performance among the n_{SE} values studied, demonstrating high P_{max} combined with a lower V_{GS}.

With this in mind, we carried out electrical measurements employing different monochromatic light colors, *i.e.*, 450 nm (blue), 550 nm (green), and 700 nm (red) for an r-VOFET with n_{SE} = 38 edges and FF = 87%. Figures 29c and 29d show the output and transfer curves acquired during illumination. As can be seen from the data, the device presents significantly higher photoswitching properties under blue light illumination; I_{blue} is around two orders of magnitude higher compared to I_{dark}, both at off and on states. In accordance with the

present results, previous studies have demonstrated that DNTT OPTs exhibit larger photoresponsivities to blue light [88,98,104,106]. This effect is explained by the fact that organic semiconductors absorb light with a specific wavelength depending on conjugated bounds and bandgap [87]. For DNTT, phonons with a wavelength of around 450 nm have enough energy to promote more efficient exciton formation [87,98,104,106].

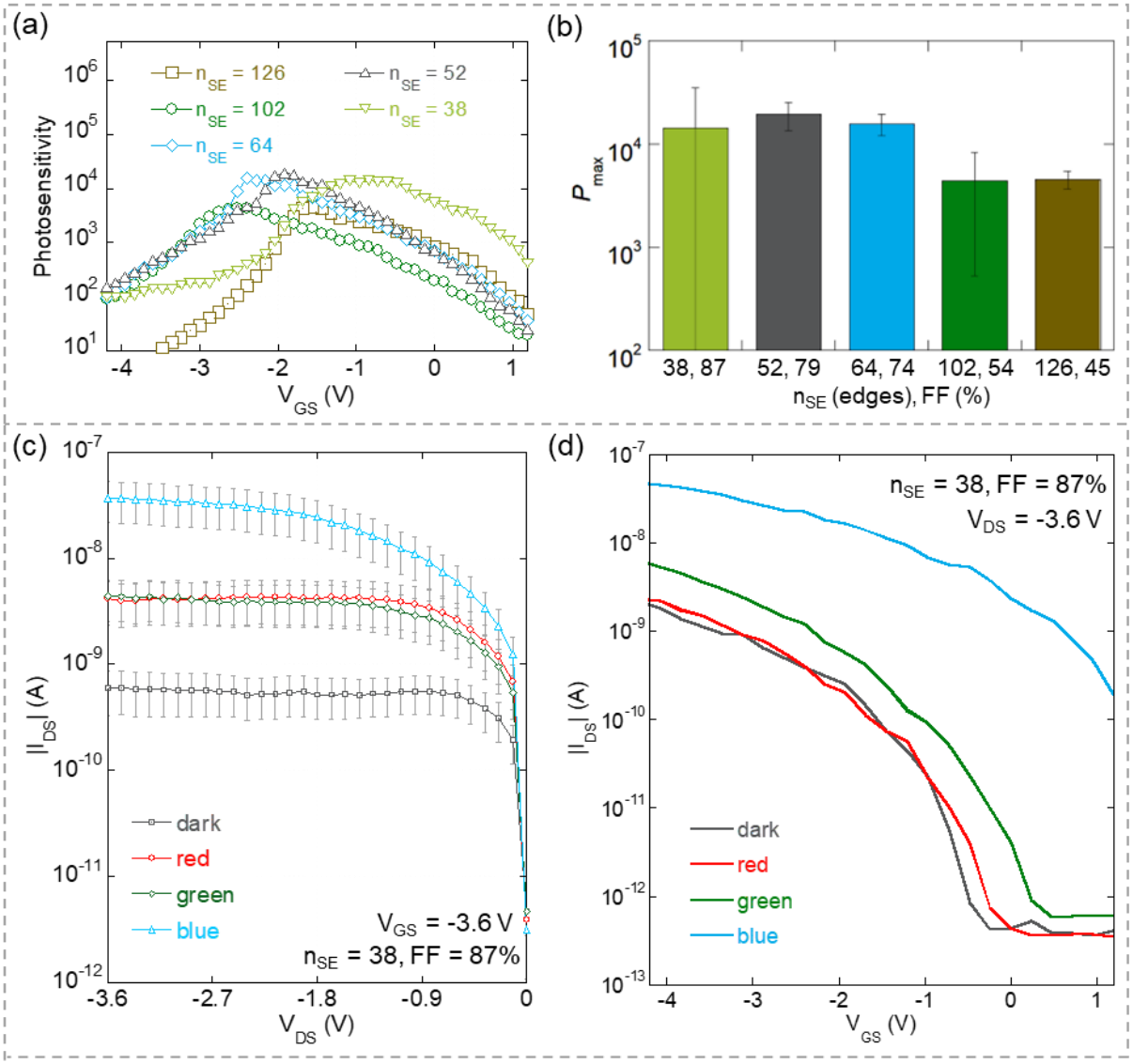


Figure 29. Investigation of the r-VOFET photoresponse. (a) Photosensitivity (I_{DS_blue}/I_{DS_dark}) *vs.* V_{GS} for r-VOFETs under blue-light illumination. The photosensitivity values were extracted from the forward transfer characteristics for different n_{SE} values. (b) P_{max} obtained in (a) for each studied n_{SE}. (c) Output and (d) transfer curves acquired for an r-VOFET with n_{SE} = 38 edges measured under illumination with different light colors. Adapted from submitted manuscript ref [110].

Additionally, with blue-light illumination, the devices demonstrated a V_{th} shift towards more positive gate voltages when compared to the transfer characteristics in the dark and under illumination with red and green light. Previous studies mostly understood this phenomenon as a trapping of photo-generated carriers at the semiconductor/dielectric interface. The Al_2O_3 thin film shows a large density of hydroxyl groups (OH^-) that act as trap centers for electrons; consequently, photo-generated electrons are trapped at the dielectric surface [95,106,129,130]. This large concentration of trapped electrons creates an additional charge sheet, which facilitates the accumulation of opposite charges at the OSC/dielectric interface, leading to the formation of the drain-source conducting channel.

In 2015, Milvich and coworkers reported this behavior for DNTT-based OTFTs with AlO_x thin film as the gate dielectric [106]. Under blue-light illumination, their DNTT OPTs showed a strong but slow threshold voltage shift (~2 V after t_{int} = 600 s) that was assumed to be described by a trap-related process. It was also found that with longer transistor channel lengths (*i.e.*, larger values for L), the light-induced V_{th} shift takes more time to saturate. This result was explained by the fact that in short-channel OPTs, the rate of photo-generated hole-electron recombination is lower [95,106,129]. With that in mind, we designed a study based on Milvich's procedure to assess in more detail the illumination time effect over the V_{th} value.

Figures 30a and 30b illustrate the biasing conditions for a proper read-out of the illumination effect: (a) the reset phase, and (b) the integration phase. In the reset phase, we subjected the device to the simultaneous application of a large negative V_{GS} and a small negative V_{DS} for approximately 10 min (Figure 30a). The negative bias at the gate electrode acts as a repulsive Columbic force for photo-generated electrons trapped at the dielectric layer. Therefore, these electrons tend to recombine with photo-generated holes in the semiconductor layer, returning the device to its initial state. Accordingly, the integration phase contributes to a fast V_{th} shift under illumination with blue light during an integration time (t_{int}), so we applied

a large positive V_{GS} simultaneously with a small negative V_{DS} for approximately t_{int} (Figure 30b). The large positive V_{GS} tends to attract more photo-generated electrons at the dielectric surface, thus increasing the trapping rate and producing a fast and controlled V_{th} shift.

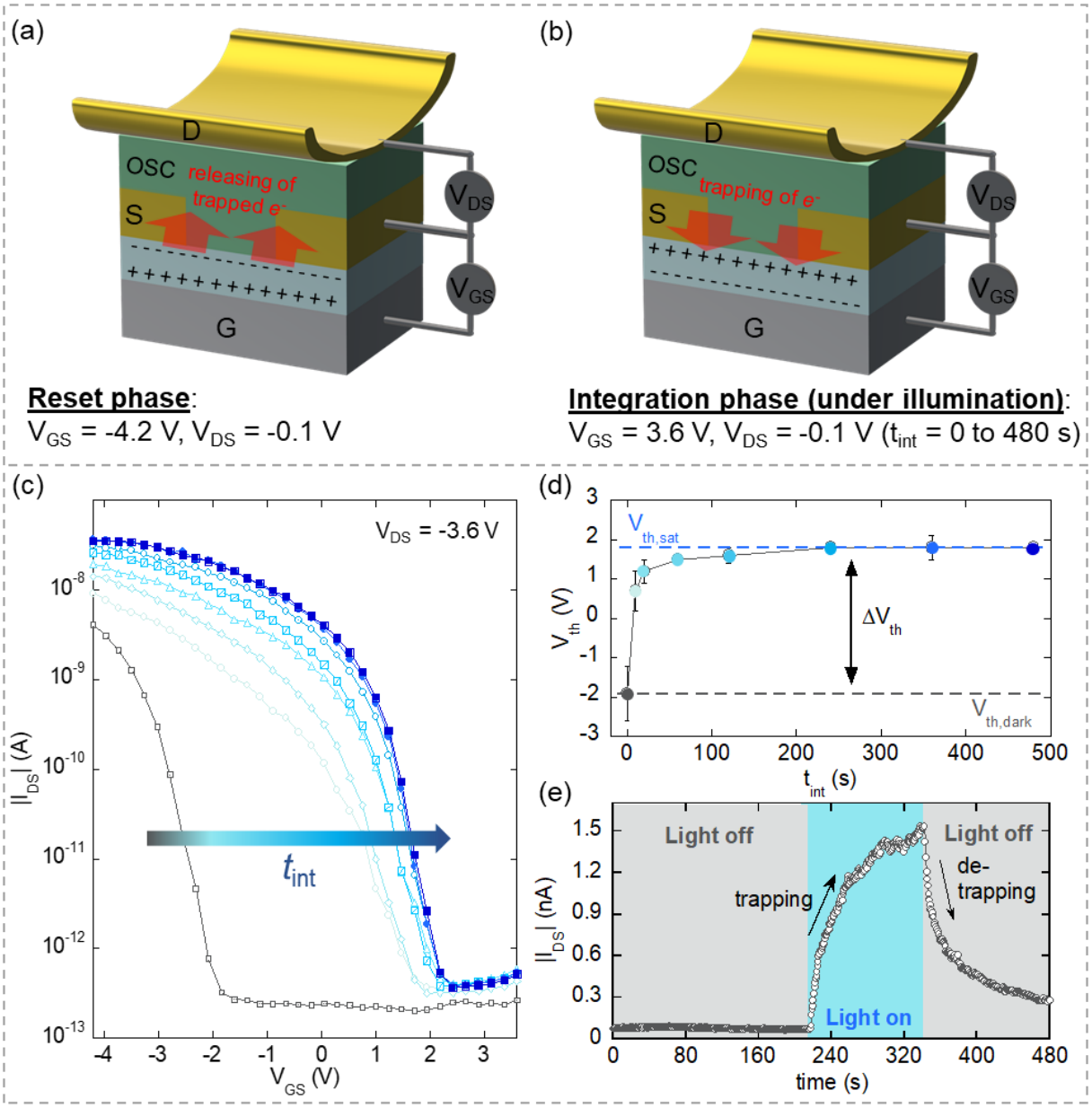


Figure 30. Light-induced V_{th} shift investigation for an r-VOFET with n_{SE} = 38 edges. 3D schematic representations of the r-VOFET during (a) reset phase and (b) integration phase, which are different biasing sequences for a proper read-out of the illumination effect. (c) Each transfer curve was acquired after illumination with blue light for a certain time. (d) V_{th} *vs.* t_{int} showing the V_{th} shift saturation. (e) Linear-scale plot for the temporal response of $|I_{DS}|$ at constant V_{DS} = V_{GS} =-3.6 V in the dark and under blue light illumination. The arrows indicate the contribution of electron trapping during illumination and electron de-trapping after illumination. Adapted from submitted manuscript ref [110].

Figure 30c shows the transfer characteristics after various t_{int} values for fixed V_{DS} = -3.6 V. Interestingly, after a short time of light exposure, our devices demonstrate a significant shift to positive V_{GS} values when comparing to the dark state (t_0). In addition, after a long time, the curves start overlapping. This suggests that the shift saturates after t_{sat}.

To establish whether our results corroborate with the findings of Milvich, *et al.*, we employed the Shockley FET equation for the saturation regime (Equation II) to calculate the V_{th} values. The results for each transfer curve in Figure 30c were plotted as V_{th} *vs.* t_{int} (Figure 30d). When the device is under illumination for t_{int} = 10 s, the V_{th} shifts approximately ΔV_{th} = 2.6 V compared to in the dark, and for t_{int} > 300 s the V_{th} value starts saturating ($V_{th} \approx$ 1.8 V). Therefore, our r-VOFETs show a ΔV_{th_sat} = 3.7 ± 0.8 V comparing the dark and saturated states. Consistent with the literature, the curve obtained for V_{th} *vs.* t_{int} demonstrates an exponential behavior that can be assumed as a trap-related process, thereby allowing the extraction of a time constant (τ) by employing the following equation [106]:

$$V_{th}(t_{int}) = \Delta V_{th_sat} \exp\left(-\frac{t_{int}}{\tau}\right) + V_{th_sat} \quad \text{(X)}$$

The yields in this investigation were improved compared to those of Milvich, *et al.* The notable V_{th} shift after a short t_{int} resulted in τ = 8.2± 2.0 V s, which denotes a fast response time for our OPTs. This difference can be explained in terms of the r-VOFET ultrashort conducting channel, and consequently its enhanced photosensitivity (Milvich OTFT's L = 10 µm, and our r-VOFET's L = 35 nm).

In order to support the electron-trapping hypothesis, Figure 30e shows the r-VOFET's $|I_{DS}|$ temporal response with and without blue-light illumination. During illumination, $|I_{DS}|$ reveals a steep rise for a few seconds because of additional photo-generated carriers, and then

there is a gradual decline in this I_{DS} increase. This result indicates that there are two different electron-trapping rates caused by the increase of trapped electron density at the OSC/dielectric interface, thereby increasing the Columbic repulsion and retarding the trapping rate. Additionally, when the illumination is turned off, I_{DS} drops slowly due to the absence of exciton generation and the increase of recombination between holes and de-trapped electrons. Another interesting result was that the r-VOFET exhibits a high retaining time for the photoresponse (*i.e.*, more than 200 s to return to the initial state), which is a very interesting property to be exploited in applications such as memory devices [103,104,129,130].

5. CONCLUSIONS

In the present work, to further investigate the edge-driven operating mechanism observed in rolled-up NM-based VOFETs, we fabricated on-chip devices employing photolithography-assisted patterning that allowed a more careful control over the patterned source electrode geometry. Additionally, a high-mobility OSC was employed in our platform in order to further evaluate its electrical characteristics (DNTT-based r-VOFETs). Our findings agree well with existing studies on CuPc-based r-VOFETs. However, the DNTT-based r-VOFETs demonstrated inferior performance (*viz.* relatively low *on/off* ratio, significant hysteresis, and high gate leakage) when compared to the state-of-the-art VOFETs. Therefore, we additionally suggested some approaches that might circumvent these limitations and improve device performance.

Hence, we fabricated devices employing rectangular-patterned source electrodes with features that guaranteed devices with different n_{SE} and *FF* values. The electrical characterization displayed a clear saturation tendency along with low operating voltages, lower hysteresis, and higher *on/off* ratio (~10^4-10^5), mainly attributed to the steep reduction in gate leakage. The optimized DNTT-based r-VOFETs presented a remarkable improvement in performance and reproducibility, thereby showing that the changes in the device architecture were effectively suitable.

When investigating the device's operation mechanism, our findings differ from Nawaz's assumptions about the edge-driven mechanism: no linear dependence between n_{SE} and I_{DS} was observed. In contrast, we discovered a surprising correlation between V_{th} and n_{SE}: r-VOFETs with larger n_{SE} (and consequently lower *FF*) show a slight increase in V_{th} values. This is explained by the fact that the permeability to the gate electric field decreases, thus resulting in a less effective barrier lowering for current injection into the semiconductor. However, V_{th}

starts dropping for n_{SE} = 102 edges, suggesting that likely there is a transition in the operating mechanism.

Therefore, we demonstrated the great potential of the rolled-up NM-based VOFET platform based on the encouraging improvements in performance that eventually could be comparable to the high-performance OFETs obtained by sophisticated processing techniques. Also, we reported remarkable findings about the r-VOFET's photoresponse: high photosensitivity (~10^4), impressive fast response time (~8.2 s), and high retaining time for the photoresponse. These results suggest that our devices are a promising alternative to surpass the performance of state-of-art photodetectors and memory technologies.

Even though our work had certain limitations, it has made a substantial contribution to the field of organic transistors. Further studies using a broader range of samples should be undertaken to explore in a quantitative framework how variables such as injection area, n_{SE}, and *FF* affect the r-VOFET operation and performance. Moreover, a reasonable approach considering these considerations could establish more definitive evidence.

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