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Semiconducting and Insulating oxides applied to electronic devices

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Tese apresentada como requisito à obtenção do título de Doutor à Universidade Estadual Paulista "Júlio de Mesquita Filho", Programa de Pós-Graduação em Ciência e Tecnologia de Materiais, sob orientação do Prof. Dr. Luis Vicente de Andrade Scalvi.

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ATA DA DEFESA PÚBLICA DA TESE DE DOUTORADO DE MIGUEL HENRIQUE BORATTO, DISCENTE DO PROGRAMA DE PÓS-GRADUAÇÃO EM CIÊNCIA E TECNOLOGIA DE MATERIAIS, DA FACULDADE DE CIÊNCIAS - CÂMPUS DE BAURU.

Aos 09 dias do mês de fevereiro do ano de 2018, às 09:00 horas, no(a) Anfiteatro do Departamento de Química da Faculdade de Ciências, reuniu-se a Comissão Examinadora da Defesa Pública, composta pelos seguintes membros: Prof. Dr. LUIS VICENTE DE ANDRADE SCALVI - Orientador(a) do(a) Departamento de Física / Faculdade de Ciências - UNESP/Bauru, Prof. Dr. IVO ALEXANDRE HÜMMELGEN do(a) Departamento de Física / Universidade Federal do Paraná, Prof. Dr. VALMOR ROBERTO MASTELARO do(a) Departamento de Física e Ciência dos Materiais / Instituto de Física - USP/São Carlos, Prof. Dr. CARLOS FREDERICO DE OLIVEIRA GRAEFF do(a) Departamento de Física / Faculdade de Ciências - UNESP - Bauru, Prof. Dr. JOSE HUMBERTO DIAS DA SILVA do(a) Departamento de Física / Faculdade de Ciências de Bauru, sob a presidência do primeiro, a fim de proceder a arguição pública da TESE DE DOUTORADO de MIGUEL HENRIQUE BORATTO, intitulada **Semiconducting and insulating oxides applied to electronic devices**. Após a exposição, o discente foi arguido oralmente pelos membros da Comissão Examinadora, tendo recebido o conceito final: APROVADO. Nada mais havendo, foi lavrada a presente ata, que após lida e aprovada, foi assinada pelos membros da Comissão Examinadora.

Prof. Dr. LUIS VICENTE DE ANDRADE SCALVI

Prof. Dr. IVO ALEXANDRE HÜMMELGEN

Prof. Dr. VALMOR ROBERTO MASTELARO

Prof. Dr. CARLOS FREDERICO DE OLIVEIRA GRAEFF

Prof. Dr. JOSE HUMBERTO DIAS DA SILVA

"Um especialista é um homem que fez todos os erros que podem ser feitos em uma estreita área (do conhecimento)."

“An expert is a man who has made all the mistakes which can be made, in a narrow field”

Niels Bohr

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Resumo

Este trabalho compreende o estudo de óxidos semicondutores (Sb:SnO_2 e TiO_2) e isolantes (ZrO_2) obtidos via sol-gel, e a investigação de suas propriedades, de modo a avaliar estes materiais como alternativa para aplicação em dispositivos eletrônicos, tais como Capacitor Metal-Isolante-Metal (MIM), transistores de filmes finos (TFT) e memristores. Os filmes finos de SnO_2 foram obtidos através de duas soluções com diferentes tempos de envelhecimento. Os filmes finos de ZrO_2 também foram obtidos a partir de duas soluções, produzidas por dois métodos distintos, não-alcoóxido e polimérico. A deposição dos filmes finos foi realizada por *dip*- e *spin-coating*, e as caracterizações foram realizadas através das técnicas de DRX, AFM, MEV, Microscopia Confocal, EDX, RBS, TG/DSC, Espectroscopia no espectro UV-Vis, Voltametria Cíclica e Espectroscopia de Impedância, afim de melhor compreender as relações entre propriedades morfológicas e estruturais dos filmes e suas propriedades elétricas. As características de filmes finos de Sb:SnO_2 e ZrO_2 foram analisadas em dispositivos TFT e MIM, respectivamente. Alternativamente, TiO_2 foi acoplado ao Sb:SnO_2 e juntos foram aplicados em memristores devido às propriedades elétricas da junção destes semicondutores. Os resultados das análises dos diferentes tipos de dispositivos eletrônicos investigados neste trabalho são discutidos considerando suas diversas características, e são também propostas opções de possíveis melhorias para tais dispositivos tornarem-se comparáveis aos estados-da-arte já existentes.

Palavras-chave: Óxidos inorgânicos, SnO_2, ZrO_2, Dispositivos eletrônicos.

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Abstract

This work comprises the study of oxide semiconductors (Sb-doped SnO_2 and TiO_2) and insulating materials (ZrO_2) obtained by sol-gel, and the investigation of their properties, aiming to evaluate these materials as alternative for application in electronic devices, such as Metal-Insulator-Metal (MIM) capacitors, Thin Film Transistors (TFT), and Memristors. The SnO_2 thin films were obtained by two solutions with different aging times. The ZrO_2 thin films were also obtained by two solutions, synthesized from two distinct methods, non-alkoxide and polymeric. The thin film deposition occurred mainly by dip- and spin-coating techniques, and the characterizations were performed through the techniques of XRD, AFM, SEM, Confocal Microscopy, EDX, RBS, TG/DSC, UV-Vis Spectroscopy, cyclic voltammetry and Impedance spectroscopy, in order to better understand the relations between the morphological and structural properties of these films and their electrical properties. The properties of Sb:SnO_2 and ZrO_2 thin films were analyzed in TFT and MIM devices, respectively. Alternatively TiO_2 was coupled with Sb:SnO_2 and applied to Memristors due to the electrical properties of this semiconductor junction. The analysis and results of the different devices investigated in this work are discussed considering their several characteristics, and it is also suggested options for possible enhancements for these devices become comparable to existent state-of-the-art devices.

Keywords: Inorganic oxides, SnO_2, ZrO_2, Electronic devices.

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Scientific Contribution Published:

1) **Boratto, M.H.**, Congiu, M., dos Santos, S.B.O., Scalvi, L.V.A., "Annealing temperature influence on sol-gel processed zirconium oxide thin films for electronic applications", Ceramics International, 44(9), 770-776, 2018.
2) **Boratto, M.H.**, Ramos Jr, R.A., Scalvi, L.V.A., "Investigation of sensing properties of sol-gel processed 4at%Sb:SnO_2/TiO_2 thin films", Journal of Materials Science: Materials in Electronics, 29(1), 467-473, 2017.
3) **Boratto, M. H.**, Ramos Jr, R. A., Congiu, M., Graeff, C. F. O., Scalvi, L. V. A. "Memristive Behavior of the SnO_2/TiO_2 Interface deposited by sol-gel", Applied Surface Science, 410, 0278-281, 2017.
4) Albano, L. G. S., **Boratto, M. H.**, Nunes-Neto, O., Graeff, C. F. O, "Silver Nanowires Grid Electrode-Based Vertical Organic Field Effect Transistor", Organic electronics, 50, 311-316, 2017.
5) Ramos Jr, R. A., **Boratto M. H.**, Li, M.S., Scalvi L. V. A, "Emission Properties Related to Distinct Phases of Sol-Gel Dip-Coating Titanium Dioxide, and Carrier Photo-Excitation in Different Energy Ranges" Materials Research, 20(4), 866-873, 2017.
6) **Boratto M. H.**, Scalvi L. V. A., Goncharova L. V., Fanchini G., "Effects of Solution History on Sol-Gel Processed Tin-Oxide Thin-Film Transistors", Journal of the American Ceramic Society, 99, 4000-4006, 2016.
7) **Boratto M. H.**, Scalvi L. V. A., "Deposition of Al_2O_3 by resistive evaporation and thermal oxidation of Al to be applied as a transparent FET insulating layer", Ceramics International, 40, 3785-3791, 2014.
8) **Boratto M. H.**, Scalvi L. V. A., Maciel Jr J. L. B., Saeki M. J., Floriano E. A. "Heterojunction between Al_2O_3 and SnO_2 Thin Films for Application in Transparent FET" Materials Research, 17(6), 1420-1426, 2014.
9) Ravaro L. P., Scalvi L. V. A., **Boratto M. H.** "Improved electrical transport in lightly Er-doped sol-gel spin-coating SnO_2 thin films, processed by photolithography" Applied Physics A, 118, 1419-1427, 2015.
10) **Boratto M. H.**, Scalvi L. V. A., "Al_2O_3 Obtained through Resistive Evaporation for use as Insulating Layer in Transparent Field Effect Transistor", Advanced Materials Research, 975, 248-253, 2014.

Motivation and Objectives

The motivation of this work is based on the necessity of new materials obtained by cost-effective processes to follow the advances in research and developing of new electronic devices. This issue requires high-quality materials for improvement of the properties of devices to reduce their size and final consumed energy. Among these materials, high-*k* insulating materials have a very important role in transistors, which can reduce their consumed energy through the higher control of the conduction channel and smaller leakage current within the device. ZrO_2 films obtained through the relative simple sol-gel process is a very promising material for such application. Semiconductors are also important materials used in transistor and other electronic devices due to their charge carrier mobility and electronic density that produces devices operating at low voltages and low energy consumption.

The objectives of this work are to present a study about the semiconductor and dielectric materials above mentioned as well as their applications in MIM, TFT and memristor devices. It is also worth noting that this is one of the first works in UNESP, campus Bauru-SP, and in the program POSMAT, about the evaluation of materials applied to different electronic devices.

The semiconductor tin oxide (SnO_2) obtained by the sol-gel process was studied and presented interesting results when coupled with other semiconductors (SnO_2/TiO_2, SnO_2/PCBM) and applied in devices such as Memristors and TFTs, whereas zirconia obtained by two different routes showed promising results through high impedance and capacitance values, comparable to values found in SiO_2.

General Considerations

An impressive part of the modern research in the field of advanced electronics is nowadays focused on the study and application of Memristors and Field-Effect thin-film transistors (TFT). TFT is a version of the Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) that are the fundamental building blocks for a large variety of electronic systems, including very large-scale integrated circuits, flat screens in portable electronics, telecommunications microcircuits and microprocessors that may contain billions of operating MOSFETs. Doped transparent oxides such as tin oxide (SnO_2) and zinc oxide (ZnO) are currently extensively explored as candidate materials for active layers in TFTs of flat panel displays.

Chapter 1 presents concepts of conductivity in materials, as well as the working mechanisms of MOSFETs and TFTs, and the leakage mechanisms that occur in real devices, which reduces their performance. In chapter 2 the concepts of the preparation and characterization of samples related to the work developed here are presented.

In the chapters from 3 to 6, alternatives of sol-gel processed materials for application in electronic devices are presented. In chapter 3, results concerning the TFTs investigation are presented, in order to understand the role and properties of the semiconductor antimony-doped tin oxide ($Sb:SnO_2$) obtained by two different solutions. The deposition of organic PCBM (Phenyl-C_{61}-butyric acid methyl ester) on top of the $Sb:SnO_2$-based transistors is accomplished in order to obtain a hybrid device with increased ambipolar conduction characteristic influenced by the organic layer. The chapter 4 and 5 presents the study of thin films of zirconium oxide (ZrO_2), an insulating and dielectric material, deposited by two different suspensions. This dielectric layer is proposed as an alternative to SiO_2 in order to improve the channel modulation in FETs. Within the chapter 6, the combination of two semiconductors obtained by sol-gel process is presented, SnO_2 and titanium dioxide (TiO_2), which was applied in resistive random-access memory (RRAM) devices. The study of these devices with the SnO_2/TiO_2 working as storage layer assists the understanding of the conduction mechanisms occurring within the semiconductors.

Chapter 1

Fundamentals of transistors

INTRODUCTION

Important concepts on materials and their conduction nature and processes are presented in this chapter. The concepts related to some devices such as MOSFET and TFT transistors are also introduced. Special attention is given to semiconductors that in the past half century have been studied and applied in electronic devices, being developed and improved at an incredible rate [1,2] in certain way that solid-state devices are now elementary part of any consumer electronics.

1 Metal, Semiconductor and Insulating Materials

Metal, semiconductor and insulating materials are fundamental for any electronic application. Metals are responsible for charge transfer and electronic conduction, while insulators are materials that are used to obstruct the electronic conduction, which is essential in many applications. The semiconductors are responsible for controlling the electrical transport due to their intermediate electronic conduction. The electronic conductivity is highly dependent on the free charge carriers concentration present in these materials, that are responsible for their electric and thermal conduction, thermal capacity and magnetic susceptibility [3].

Negative free carriers, electrons, are responsible for the materials conductivity and are preferentially located at the bottom of the conduction band of metals, semiconductors, and insulators, as schematic represented in figure 1.1. The figure shows the conduction (CB) and valence bands (VB) and a forbidden region between them, the bandgap. Insulators present a high gap of energy, while smaller gap is found for semiconductors, and finally, metals present the conduction band partially filled even at 0 K without the presence of bandgap [3].

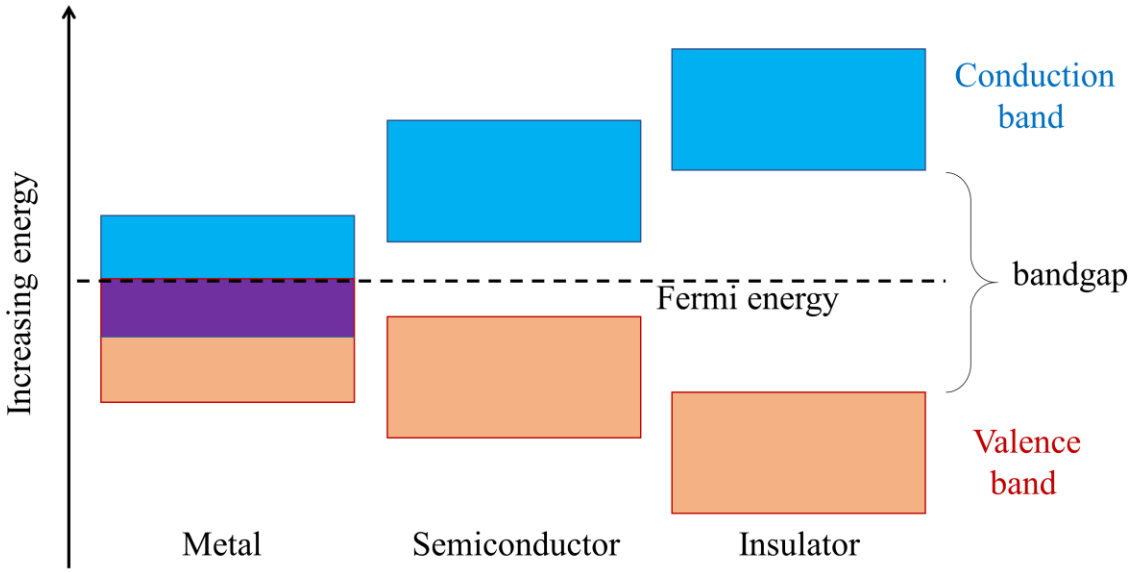

Figure 1.1: Schematic diagram showing different valence and conduction band for Metal, Semiconductor, and insulating materials. (adapted from http://energyeducation.ca/encyclopedia/Band_gap, accessed in 27/11/2017)

The red color region represents the valence band that contains the electrons in the materials lattice, which are used in chemical bonds, therefore are not free for conduction under applied potential. Semiconductors with bandgap require energy to break covalent bonds and produce free electrons into the conduction band that usually presents abundantly empty states [4]. The same occurs for insulating materials, but due to the higher bandgap energy, higher energy is required to release electrons from chemical bonds. At room temperature some semiconductors have enough thermal energy to present reasonable free electron concentration and fair electrical conduction, while insulators present high electrical resistance. Intrinsic semiconductors present the Fermi energy centered between the conduction and valence bands at T = 0 K, that means their free concentration of electrons and holes are equal. Semiconductors can be doped by different types and concentration of impurities in order to modify their conductivity [5]. N-type doping in semiconductors consists of inserting atoms with more electrons than the original atom of the lattice. The concentration of electrons (n) added by the dopant may be found by the equation 1.1 [6]:

$$n = n_i \exp\left(\frac{E_F - E_i}{k_B T}\right) \tag{1.1}$$

Where n_i is the intrinsic carrier density of the non-degenerate semiconductor, E_F and E_i are the Fermi and intrinsic Fermi level, respectively, k_B is the Boltzmann constant, and T is the absolute temperature. The Fermi energy is shifted upward, towards the CB bottom for n-type doping. On the other hand, the Fermi level is shifted downward, towards the VB top, upon p-type doping.

Insulating materials are generally dielectrics, that under electric field exhibit electric dipoles through the separation of positive and negative entities in molecular and atomic level. These dipoles are opposite to the applied electric field, which reduces the resultant electric field and current through the material. The dielectric constant (k), also known as relative permittivity (ε_r), is the ratio of the absolute permittivity of the material (ε) and the vacuum ($k = \varepsilon_r = \varepsilon/\varepsilon_0$). Insulating materials with high k are of great interest in applications in devices like capacitors and field effect transistors [7,8].

2 Electronic and Ionic Conductivities

Electric current is the result of the movement of charge carriers due to an applied electric field. The electronic (σ_e) and ionic (σ_i) conductivity occur by electrons and holes, and ions, respectively. The electronic conductivity is related to the elementary charge (q), density of electrons (n) and holes (p) and their respective mobility (μ_e and μ_h):

$$\sigma_e = q\ (n\ \mu_e + p\ \mu_h) \tag{1.2}$$

The lower conductivity present in nanocrystalline or amorphous semiconducting materials is related to their lattice defects and impurities that difficult the charge transport and reduce the mobility of the charge carriers in the material through scatterings within the material [5].

The ionic conduction occurs predominantly in ionic materials [4,6] and relies on the temperature and on defects in the material, such as interstitial atoms, ion concentration, and vacancies, allowing the ions to diffuse through the material under electric field. The ionic conductivity σ_i is given by the Nernst-Einstein equation,

$$\sigma_i = 2\ d\ q\ D\ k_B\ T \tag{1.3}$$

which is related to volume density of ions (*d*), ion diffusion coefficient through the material (*D*), and absolute temperature (*T*) [9]. In ionic materials, such as Al_2O_3 and ZrO_2, the conduction may occur by both types of carriers and the resultant conduction (σ_R) is their sum ($\sigma_R = \sigma_e + \sigma_i$). Important factors concerning the predominance of one conductivity over the other, are the type of material (e.g. semiconductor, insulator, metal), purity, and temperature [4,6].

3 Transistors

Transistor, a contraction for transfer resistor, is a multi-junction semiconductor device. It is normally integrated with other circuit elements for voltage, current or signal-power gain. Opposite to Field Effect Transistors (FET) where predominantly only one kind of carrier participates in the conduction process, a bipolar transistor is a semiconductor device in which both electrons and holes participate in the conduction process. In the past decades both FET and bipolar transistors have been extensively studied and applied in high-speed circuits, and power applications [6].

3.1 Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

The metal–oxide–semiconductor field-effect transistor (MOSFET) is the main component of the microelectronic industry. MOSFETs are the building blocks of memory chips, telecommunication microcircuits and microprocessors [5] that may contain billions of transistors. MOSFETs are multipurpose but mainly used as switches in logic microcircuits [10].

A typical architecture of a n-type MOSFET (NMOS) is shown in figure 1.2 and comprises two highly doped n^+-type semiconductor regions, called source and drain, separated by a p-type substrate. A gate contact is separated from the substrate by a thin insulating material, the gate oxide. The source is grounded and a positive voltage is applied to the drain. A p-type MOSFET, or PMOS device, would have the opposite doping in the source and drain (p^+-type) and substrate (n-type) regions [10].

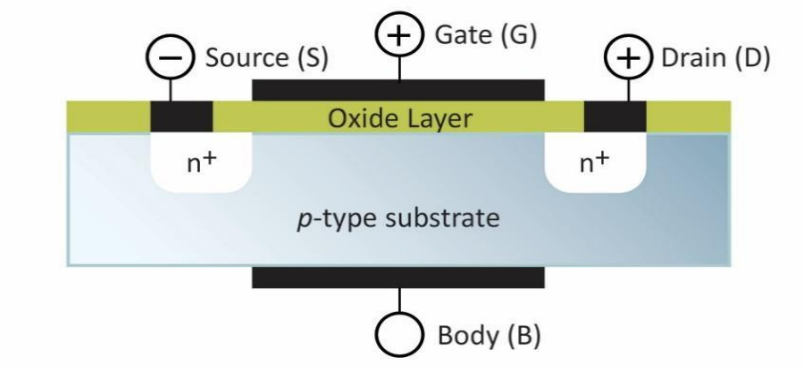

Figure 1.2: Architecture of a NMOS with electrical connections. Source is grounded, gate and drain are positive biased (adapted from https://www.doitpoms.ac.uk/tlplib/semiconductors/mosfet.php, accessed in 27/11/2017).

At first, between drain and substrate there should not have electrical current because the p-n junction is reverse biased, as well as between source and substrate, due to zero bias across the source p-n junction. Therefore, there is no drain-source current and the transistor is in the off-state, as an open switch [10]. The creation of a conduction channel starts when a positive gate voltage (V_G) greater than a threshold voltage (V_T) is applied relative to the grounded source. This channel is formed by electrons (e^-) injected by the electron-rich region, the source, by induction into the p-type semiconductor-insulator interface. This interface repels the positive carriers from the p-type substrate and a continuous electron bridge, called the channel, is formed between the source and drain, that flows current under drain positive potential bias relative to the source (V_{DS}).

There are three different types of conduction in FETs: Accumulation, Depletion and Inversion. For NMOS the electronic bands of the semiconductor are bended downward when positive V_G is applied, and the bottom of the conduction band (CB) of the semiconductor layer bends closer to the Fermi level (E_F), as shown in figure 1.3a. In this case the transistor operates in accumulation regime, the "on-state", like a closed switch [10–12]. The electron depletion mode occurs at zero or negative applied gate voltage that bends the CB upwards and reduces the free electron concentration on the channel (figure 1.3b), turning the device into the off-state. The inversion regime occurs when a much larger negative voltage is applied to the gate, and both the CB and valence band (VB) bend even more upward and the intrinsic Fermi level (E_i) eventually crosses the Fermi level, which causes the density of holes to exceed the density of electrons, and a predominant hole conduction start to flow [12,13] as shown in figure 1.3c.

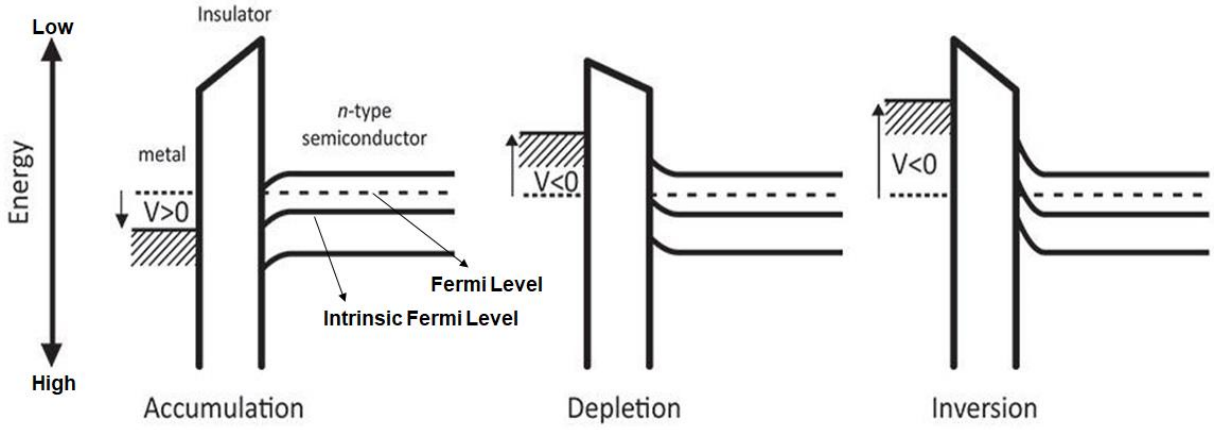

Figure 1.3: (a) Accumulation, **(b)** depletion, and **(c)** inversion modes in n-type FET. (adapted from [12]).

An ideal and perfect switch should present zero current when off and maximum current, without resistance, when on, being capable of switching instantly from these two states. However, real transistors are imperfect switches with electrical current different of zero in the off-state and a limited on-current occurs, and consequently requires time in the switching process. As transistors are being shrunk in size, their switching behavior tends to become worse. Ferain and collaborators [13] suggest the change of the planar gate configuration into a channel-rounded by a gate electrode. In that way, the electrostatic control of the channel is improved and could allow the further shrinking in size without downgrading transistor performance.

The linear plot of the output characteristic of a generic n-type transistor (figure 1.4a) shows no significant current below a particular minimum gate voltage applied, called the threshold voltage (V_T). Above the threshold voltage, the current initially increases linearly with the applied gate bias, at constant V_{DS} [10]. For a constant V_G, the current also increases linearly with the V_{DS}, then gradually levels off into a constant value within the saturation regime [12]. The equation 1.4 presents the linear dependence of V_T as function of free charge carrier concentration (N_e) [12–14]:

$$V_T = \frac{q\, t\, N_e}{C_i} \tag{1.4}$$

where q is the elementary charge, and t and C_i are the dielectric layer thickness and capacitance per unit area, respectively. Therefore, V_T is influenced by higher doping level and thicker dielectric layer. Park et al [14] presented a study about the control of the transistor threshold

voltage by adjusting the dielectric thickness rather than chemical doping technique, without any modification of essential properties of the transistors, whereas Moon et al [15] added a layer of transition metal oxide with high work function on the gate interface with the dielectric. Moreover, the V_T can also be extracted either from transfer curves ($I_D^{1/2}$ *vs* V_G) as presented in figure 1.4b of the transistor in the saturation region, or by plotting $(I_D)^{1/2}$ *vs* V_G and extrapolating the linear curve to $I_D^{1/2} = 0$ [16].

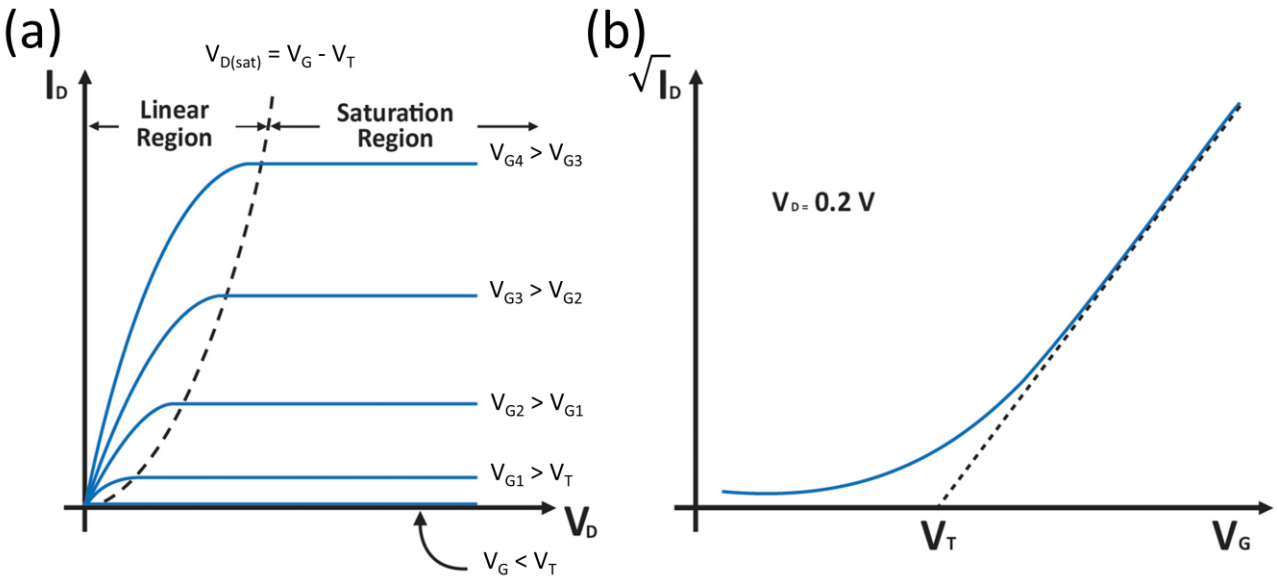

Figure 1.4: (a) Output and **(b)** transfer curves of a generic n-type transistor. **(a)** A region of linear current occurs prior the saturation region. **(b)** The V_T indicates the minimum gate voltage required to create the conduction channel, increasing significantly the drain current. (adapted from http://www.rfwireless-world.com/Terminology/Depletion-MOSFET-vs-Enhancement-MOSFET.html, accessed in 27/11/2017).

Both linear and saturation output currents shown in figure 1.4a are related to dimensions of the channel and intrinsic properties of the semiconductor material that forms the conducting channel on the interface with the dielectric layer. Equations 1.5 and 1.6 present these relations [12]:

(Linear) $$I_D = \frac{W \mu C_i (V_G - V_T) V_D}{L} \quad (1.5)$$

(Saturation) $$I_D = \frac{W \mu C_i (V_G - V_T)^2}{2 L} \quad (1.6)$$

where μ is the mobility of the charge carriers in the channel, W and L are the channel width and length, respectively.

The ratio of the maximum and minimum current (I_{ON}/I_{OFF}) that can be verified on the transfer curves (I_D *vs* V_G) is an important characteristic for transistors along with the channel transconductance (g_m), expressed in Siemens (S), given by the linear variation of I_D as function of the gate voltage applied on the transfer curves [12,17], as presented in the equation 1.7 [17]:

$$g_m = \frac{\partial I_D}{\partial V_G}_{V_{D.lin}=const} = \frac{W}{L}\,\mu_{FE}\,C_i\,V_D \tag{1.7}$$

for small values of V_D, representing the linear region on output curves. μ_{FE} is the field-effect charge carrier mobility induced by the transconductance [18]. At saturation region in output curves the transconductance is obtained by equation 1.8 [16]:

$$g_m = \frac{\partial I_D}{\partial V_G}_{V_{D,sat}=const} = \frac{W}{L}\,\mu_{FE}\,C_i\,(V_G - V_T) \tag{1.8}$$

Another fundamental characteristic of transistor is the subthreshold current (I_{OFF}) that occurs at $V_G < V_T$. It is a sort of leakage current undesirable for a transistor, where at an ideal case a transistor would present $I_{OFF} = 0$ and an infinite g_m. The subthreshold slope (SS) indicates how effectively a transistor can be turned off as function of V_G (for $V_G < V_T$) [19]. The SS is presented in equation 1.9 as the inverse of the slope in the subthreshold region presented in figure 1.5.

$$SS = \frac{dV_G}{d(\log_{10} I_D)} \equiv \frac{k_B\,T}{q}[\ln(10)]\,n \tag{1.9}$$

where *n* is the body factor, that represents the electrostatic control efficiency of the gate voltage on the channel region, inversely proportional to change in channel potential (Φ_{CH}): $n = dV_G/d\Phi_{CH}$. The SS is expressed in millivolts per decade of current (mV/decade). In the ideal case, where the electrostatic coupling between the gate and the channel region is 100% effective at room temperature *n* would be equal to 1, leading the minimum value for SS to be 59.6 mV/dec [10]. However, one shall notice that in real cases *n* varies between 1.2 and 1.5, which results in larger SS values, from 70 to 90 mV/dec. The SS = 70 mV/dec obtained on single-walled carbon nanotube (SWNT) FETs with ZrO_2 film as dielectric is superior to devices with bottom gates with either Al_2O_3 or SiO_2 as dielectrics (SS~180 and 400 mV/dec,

respectively) [20]. They also present better performance with extremely low static power dissipation than single-gate silicon MOSFET with SS of 80 mV/dec. Thus, the SWNT FETs present excellent switching capabilities, as well as on–off ratio greater than 10^4, that are features required from a successor of the silicon based MOSFETs. For conventional FETs, these features require the bandgap of the semiconductor material to be larger than 0.4 eV, therefore, n- and p-channel FETs with this range of bandgap and symmetrical threshold voltages for e^- and h^+ charges that present bipolar conduction are also desired for application on complementary MOS (CMOS) operations [10,17].

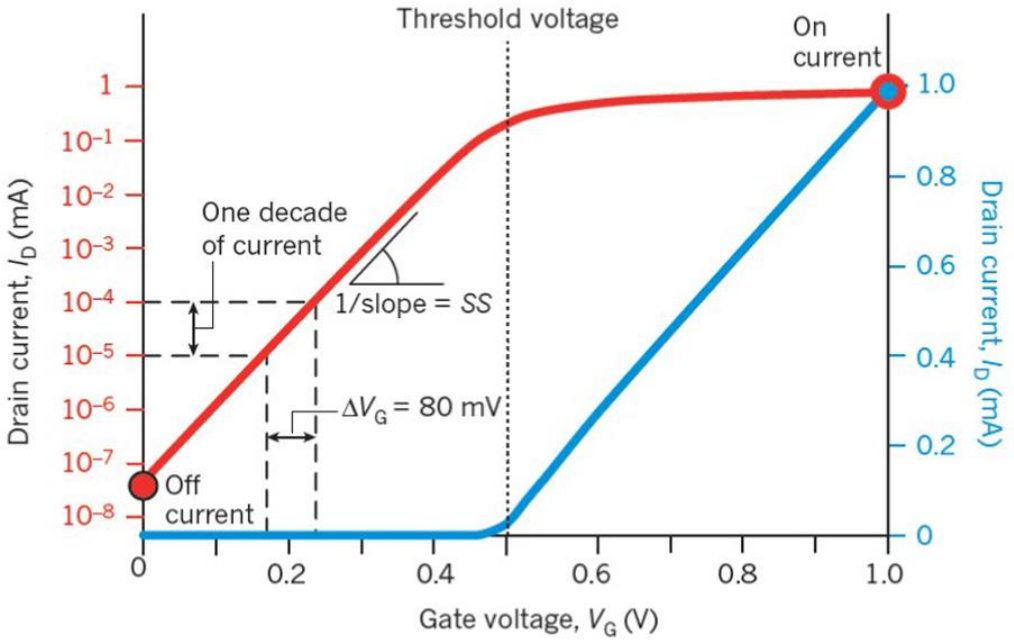

Figure 1.5: Logarithmic and linear scale of I_D *vs* V_G. The log (I_D) shows the contribution of SS on the current for $V_G < V_T$. (adapted from [10]).

3.2 Thin-Film Transistor (TFT)

Thin-film transistor (TFT) concept was first introduced by Weimer in 1962 [12]. The main difference from MOSFETs is the substrate, because in the MOSFET the substrate works as an active semiconductor (e.g. silicon wafer), while the substrate of TFTs only supports the films. The TFT presents a simpler structure compared to MOSFETs, composed of metal (gate)/insulator/semiconductor/metal (drain and source), as shown in figure 1.6a. The source and drain electrodes ideally form ohmic electric contacts directly to the conduction channel, with no depletion region to turn-off the device, unlike the p-type substrate on n-MOSFETs that acts

as depletion region. Thus, the I_{OFF} depends directly on the low conductivity of the semiconductor and on the V_G (< V_T) to reduce charge carriers on the channel. Therefore, these devices are better enhanced when using low conductivity semiconductors such as amorphous silicon [12] or SnO_2 [21] and C_{60} that are active semiconductors used in the TFTs investigated in this work. Some TFTs architectures are shown in figure 1.6. Other kind of transistors with different architectures and functionalities exist [12] but are not considered in this work.

The working process of n-TFT is similar to the process presented for n-MOSFETs which occurs through the accumulation of electrons and forms the channel on the insulator-semiconductor interface under $V_G > V_T$. These charges are driven by the voltage difference between the source and drain electrodes. Therefore, by changing the gate voltage, the number of accumulated electrons can be varied from accumulation to depletion, or even inversion, modes which results in the variation of the channel conductivity. The scheme of how the depletion region arises in these devices is presented in the figure 1.6b. When high negative V_G is applied, electrons are repelled from the semiconductor/insulator interface by the electric field, and an accumulation of minority charges (h^+ in n-TFTs) grows up into the semiconductor/insulator interface creating a depletion region (I_1) that reduces the current by electrons (I_2). At higher negative applied V_G, the accumulation of holes become predominant and starts to conduct in the channel (I_D) in the inversion mode.

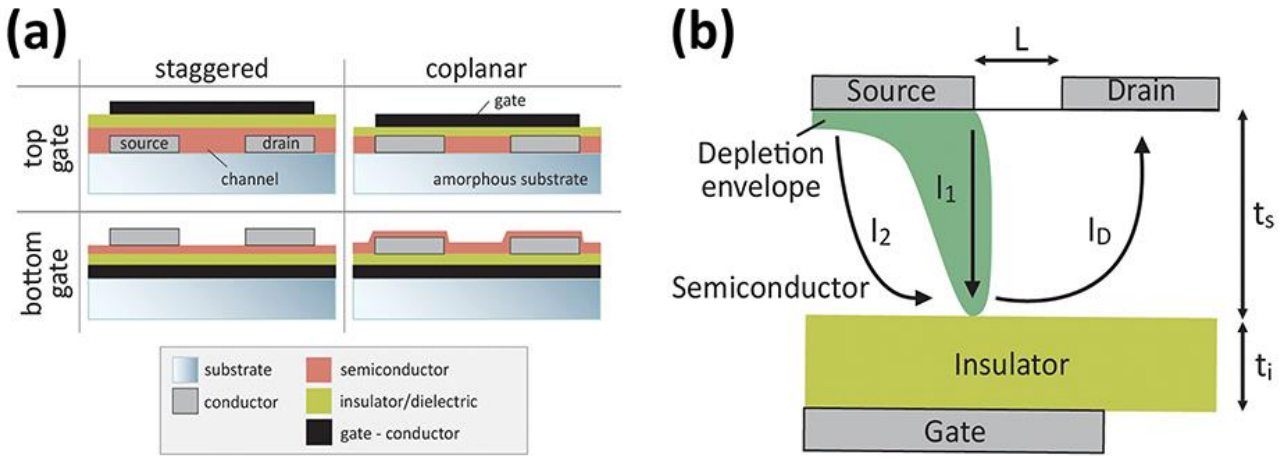

Figure 1.6: (a) Four different possible architectures for TFT devices with top and bottom gate electrode. **(b)** Diagram of the mechanism for depletion mode in TFT devices. ((a) and (b) are adapted from https://en.wikipedia.org/wiki/Thin-film_transistor, accessed in 27/11/17.

4 Leakage mechanisms

The miniaturization of transistor devices through the reduction of channel length and dielectric oxide thickness present adverse effects called short-channel effects (SCE) which may increase the leakage current of the transistor. To maintain a reasonable SCE immunity while scaling down the channel length, oxide thickness must be reduced nearly in proportion to the channel length. Decrease of the oxide thickness results in increase in the electric field across the gate oxide, that along with low oxide thickness result in considerable current flowing through the gate of a transistor [5,19,22]. This current destroys the classical infinite input impedance assumption of MOS transistors and thus affects the circuit performance severely. Figure 1.7a shows the main leakage mechanisms that occur in transistors. The major contributors to the gate leakage current are gate oxide tunneling (I_{gate}) and the injection of hot carrier (I_{HC}) from the substrate to the gate, illustrated in figure 1.7b. Gate-induced drain leakage (GIDL) is another significant leakage mechanism that occurs in depletion mode at the drain surface, below the gate-drain overlapping region. Subthreshold leakage (I_{sub}), GIDL and channel punch-through current are off-state leakage mechanisms, while $I_{junction}$ (for reversed V_D) and I_{gate} occur in both ON and OFF states. Gate current can occur in the off-state due to hot-carrier injection but typically occurs during the transition bias states of the transistor [19]. In Si-SiO_2 MOSFET the injection is more likely for electrons than holes, as electrons have a lower effective mass than that of holes and the barrier energy for holes (4.5 eV) is higher than for electrons (3.1 eV) [19].

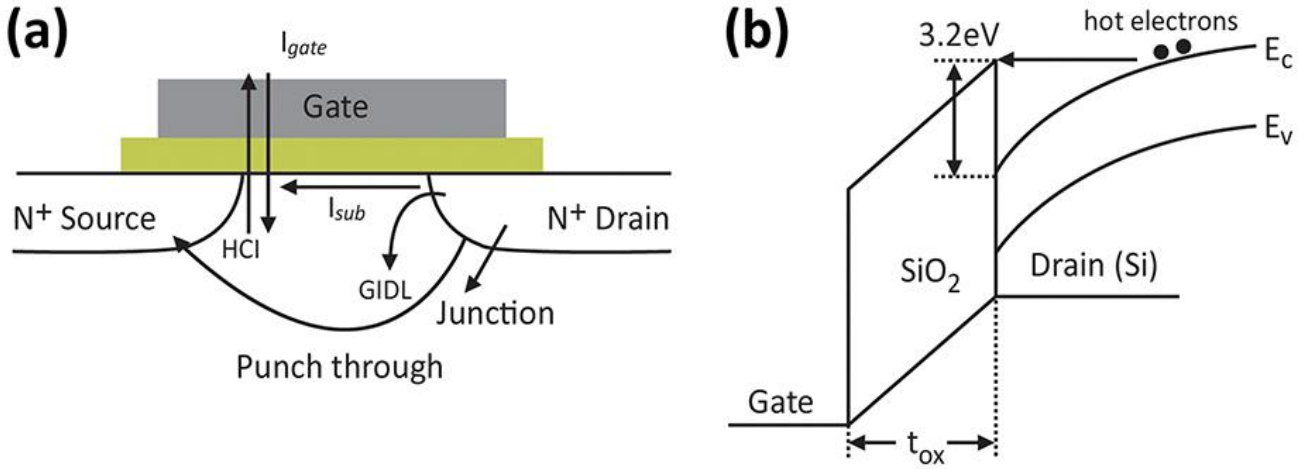

Figure 1.7: (a) Different types of leakage mechanisms in n-MOSFET devices. **(b)** A gate leakage mechanism, the hot carrier injection (I_{HC}), occurs at high electric fields, where electrons gain enough energy to cross the interface potential barrier to enter the gate electrode. (adapted from [5]).

REFERENCES

[1] R. Chau, B. Doyle, S. Datta, J. Kavalieros, K. Zhang, Integrated nanoelectronics for the

future, Nat. Mater. 6 (2007) 810–812. doi:10.1038/nmat2014.

[2] F. Liu, Y. Zhou, Y. Wang, X. Liu, J. Wang, H. Guo, Negative capacitance transistors with monolayer black phosphorus, Npj Quantum Mater. 1 (2016) 16004. doi:10.1038/npjquantmats.2016.4.

[3] C. Kittel, Introdução à Física do Estado Sólido, 8th ed., LTC, Rio de Janeiro, 2006.

[4] R. Enderlein, N.J.M. Horing, Fundamentals of Semiconductor Physics and Devices, World Scientific, Singapore, 1997.

[5] S.M. Sze, K.K. Ng, Physics of Semiconductor Devices, John Wiley & Sons, Hoboken, 2007.

[6] S.M. Sze, Semiconductor Devices: Physics and Technology, 2006. doi:10.1016/S0026-2692(82)80036-0.

[7] J. Robertson, B. Falabretti, Band offsets of high K gate oxides on III-V semiconductors, J. Appl. Phys. 100 (2006) 0–8. doi:10.1063/1.2213170.

[8] M.H. Boratto, L.V.A. Scalvi, Deposition of Al2O3 by resistive evaporation and thermal oxidation of Al to be applied as a transparent FET insulating layer, Ceram. Int. 40 (2014) 3785–3791. doi:10.1016/j.ceramint.2013.09.041.

[9] P.P. Kumar, S. Yashonath, Ionic conduction in the solid state, J. Chem. Sci. 118 (2006) 135–154.

[10] I. Ferain, C. a. Colinge, J.-P. Colinge, Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors, Nature. 479 (2011) 310–316. doi:10.1038/nature10676.

[11] H. Wang, D. Yan, Organic heterostructures in organic field-effect transistors, NPG Asia Mater. 2 (2010) 69–78. doi:10.1038/asiamat.2010.44.

[12] G. Horowitz, Organic Field-Effect Transistors, Adv. Mater. 10 (1998) 365–377. doi:10.1002/(SICI)1521-4095(199803)10.

[13] T. Ytterdal, Y. Cheng, T.A. Fjeldly, MOSFET Device Physics and Operation, in: Device Model. Analog RF C. Circuit Des., 2003: pp. 1–45. doi:10.1002/0470863803.ch1.

[14] J.S. Park, J.K. Jeong, Y.G. Mo, H.D. Kim, C.J. Kim, Control of threshold voltage in ZnO-based oxide thin film transistors, Appl. Phys. Lett. 93 (2008) 91–94. doi:10.1063/1.2963978.

[15] H. Moon, D. Im, S. Yoo, Controlling the Threshold Voltage of Organic Thin-Film Transistors by Transition Metal Oxides, Electron Device Lett. IEEE. 34 (2013) 1014. doi:10.1109/LED.2013.2264140.

[16] W. Xu, H. Wang, F. Xie, J. Chen, H. Cao, J. Bin Xu, Facile and Environmentally Friendly Solution-Processed Aluminum Oxide Dielectric for Low-Temperature, High-Performance Oxide Thin-Film Transistors, ACS Appl. Mater. Interfaces. 7 (2015) 5803–5810. doi:10.1021/am508775c.

[17] F. Schwierz, Graphene transistors, Nat. Nanotechnol. 5 (2010) 487–496. doi:10.1038/nnano.2010.89.

[18] C. Avis, J. Jang, High-performance solution processed oxide TFT with aluminum oxide gate dielectric fabricated by a sol–gel method, J. Mater. Chem. 21 (2011) 10649.

doi:10.1039/c1jm12227d.

[19] K. Roy, S. Mukhopadhyay, H. Mahmoodi-Meimand, Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits, Proc. IEEE. 91 (2003) 305–327. doi:10.1109/JPROC.2002.808156.

[20] A. Javey, H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. McIntyre, P. McEuen, M. Lundstrom, H. Dai, High-kappa dielectrics for advanced carbon-nanotube transistors and logic gates., Nat. Mater. 1 (2002) 241–246. doi:10.1038/nmat769.

[21] M.H. Boratto, L.V.A. Scalvi, L. V. Goncharova, G. Fanchini, Effects of Solution History on Sol-Gel Processed Tin-Oxide Thin-Film Transistors, J. Am. Ceram. Soc. 99 (2016) 4000–4006. doi:10.1111/jace.14459.

[22] J. Robertson, High dielectric constant gate oxides for metal oxide Si transistors, Reports Prog. Phys. 69 (2005) 327–396. doi:10.1088/0034-4885/69/2/R02.

Chapter 2

Fundamentals of Experimental Methodology

INTRODUCTION

In this chapter are presented the general concepts of the experiments used to produce and characterize the thin films and electronic devices used in this work. Specific methodology, materials and equipment information, e.g. brand and model, are presented in the chapters where they are applied.

Sample preparations were done mainly by sol-gel spin-coating and dip-coating processes, as well as by resistive evaporation technique. The characterizations were more widely explored through the techniques: X-Ray Diffraction, Rutherford Backscattering Spectrometry (RBS), Ultraviolet-Visible-near-Infrared Transmittance Spectroscopy (UV-Vis-nIR), Atomic Force Microscopy (AFM), Confocal Laser Scanning Microscopy, Scanning Electron Microscopy (SEM), Energy Dispersive X-Ray Spectroscopy (EDX), Electrical Impedance Spectroscopy (EIS), and Current *vs* Voltage (IxV).

1 Sample preparation

1.1 Sol-Gel

Inorganic oxide compounds were synthesized by the sol-gel process, that is based on the hydrolysis and condensation of molecular precursors such as metal alkoxide or hydroxylated metal ions in aqueous solutions. The colloid suspension is in the sol state when the dispersed particles are separated by the continuous phase, the dispersant. The gel state occurs when the particles get closer due to reduction of the dispersant in the suspension [1]. Inorganic polymerization is responsible for the link between particles that produces solid materials through the conversion of monomers into a colloidal solution [2]. A variety of materials can be obtained from this process, such as fibers, xerogel, aerogel, particles and thin films [1]. Figure 2.1 presents the many possibilities of materials obtained through this process. The sol-gel process is used in

this work for obtaining thin films of the semiconductor oxides SnO_2, TiO_2, and the insulating oxide ZrO_2.

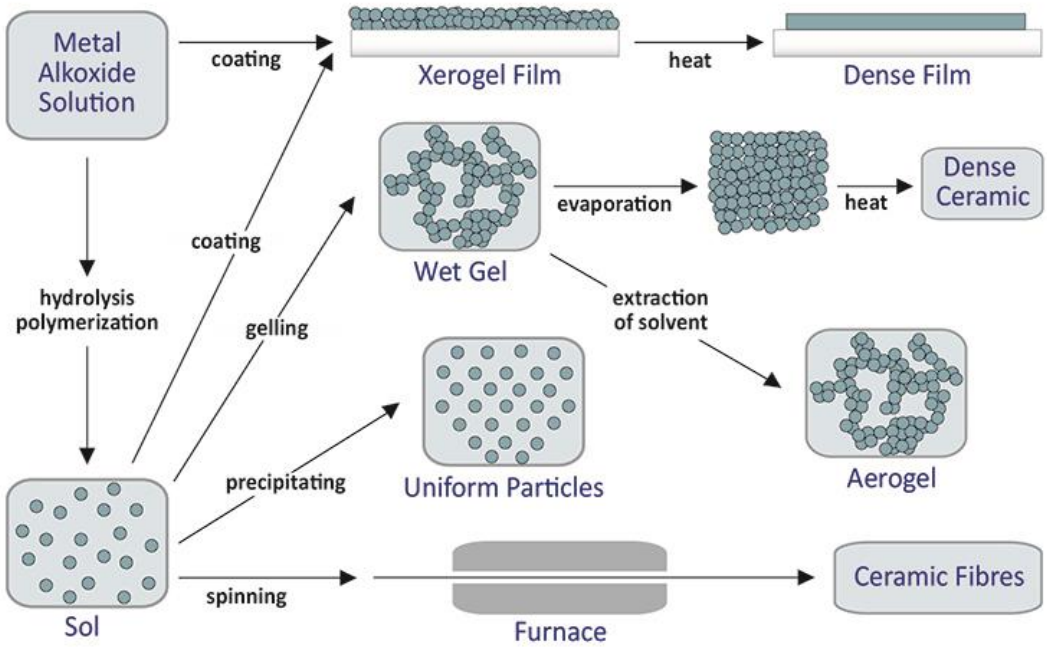

Figure 2.1: Many materials obtained by sol-gel process through different methods. (adapted from https://en.wikipedia.org/wiki/Sol-gel), accessed in 27/11/17.

1.2 Spin and Dip-Coating

Spin and dip-coating are methods of deposition of thin films that use chemical solutions to form the xerogel on a substrate surface. A diagram of the spin-coating deposition technique is presented in figure 2.2a, where the substrate is placed inside a deposition chamber and hold by vacuum. The deposition occurs by dropping the sol-gel suspension on the area where the material shall be deposited, and the equipment starts the rotation, accelerating until reaches the desired speed in order to spread the suspension on the substrate. Then, the film is dried in air before calcination on hotplate or furnace to eliminate the solvents.

A diagram of the dip-coating process is shown in figure 2.2b. It is carried out using an equipment with high control of the immersion and emersion speed of the substrate in the sol-gel suspension placed in a beaker. The emersion process forms the thin film that dries in air after being removed from the suspension. This process is followed by a calcination between deposited layers and, a final thermal annealing in order to eliminate solvents and crystallize the material.

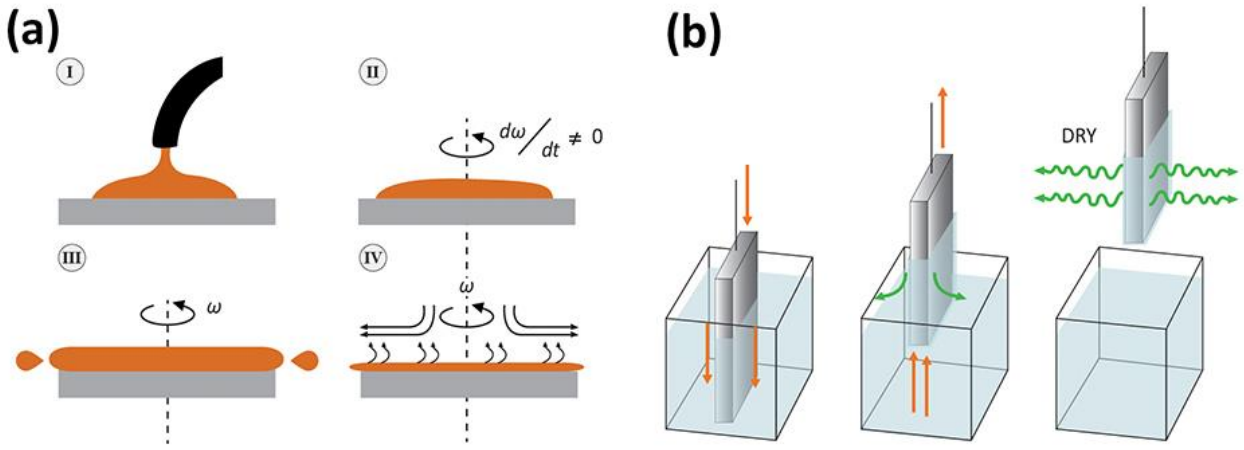

Figure 2.2: (a) Spin-coating and **(b)** dip-coating, both processes of deposition of thin film. ((a) and (b) are adapted from http://large.stanford.edu/courses/2007/ph210/hellstrom1/, accessed in 27/11/17, and [3], respectively.

1.3 Thermal Evaporation

The physical vapor deposition (PVD) is a useful method for deposition of insulating, semiconductor and metal films onto large area substrates. This deposition method can be accomplished in different equipments such as conventional resistive evaporation, electron beam (e-beam), Molecular Beam Epitaxy (MBE) and Pulsed Layer Deposition (PLD). A high vacuum is necessary in all of these equipments in order to minimize the collisions of the evaporated particles with gases in the chamber [4], in order to produce films with higher purity. In this work, the resistive evaporation is used to deposit metallic and semiconductor thin films under pressure of 3×10^{-5} torr.

For the simple thermal evaporation process to occur, it is necessary to use either a twisted-wire coil or a dimpled sheet-metal "boat", both made from refractory metals (e.g. tungsten W, molybdenum Mo, and tantalum Ta). The material used in this work was W. The figure 2.3a presents the "boat". The evaporating material is placed on the "boat" to be heated by Joule effect through currents of about 100 Ampère [4].

The diagram of a thermal evaporation chamber is presented in figure 2.3b. The evaporation starts with the source being heated generating the vapor that reaches the substrate surface placed above the source material, that adsorbs the vapor by fisisorption through Van der Waals bondings with energy around 0.1 eV/atom [4]. The next step is the superficial diffusion, where the atom allocates itself among the surface sites to be incorporated through strong bonding such as covalent (> 1 eV/atom) at the surface. Then, the nucleation of groups of atoms starts to occur, forming the layer of thin film [4]. The evaporation of materials was carried out in

a Boc Edwards Auto 500 evaporation chamber, located at the Electro-Optical Phenomena Laboratory under supervision of Prof. Dr. L. V. A. Scalvi at UNESP, Bauru.

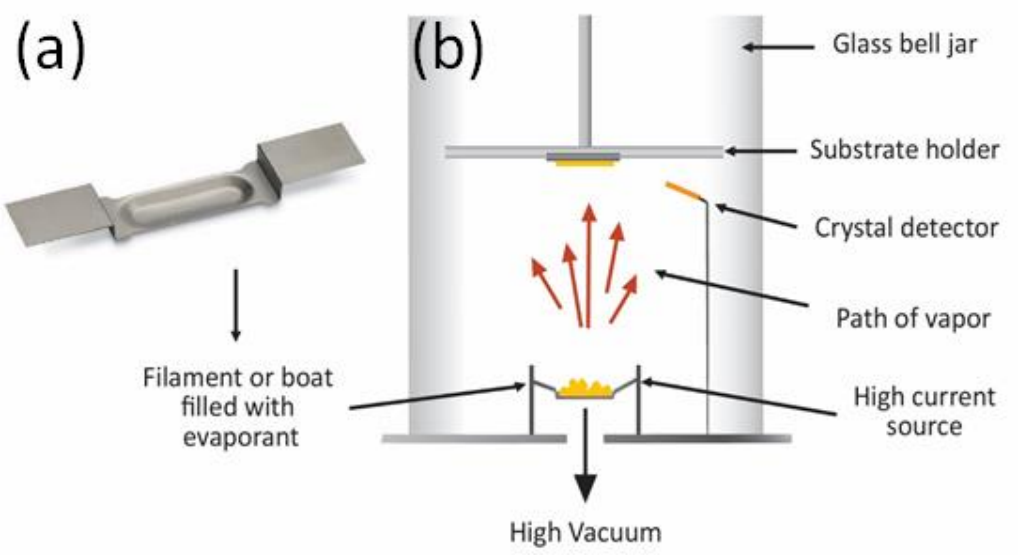

Figure 2.3: (a) Tungsten boat where the evaporating material is placed to be heated. **(b)** Diagram of the evaporation chamber showing the deposition processes of thin films. (adapted from http://www.betelco.com/sb/phd/ch3/c34.html, accessed in 27/11/17)

The Clausius-Clapeyron's equation (2.1) relates the vapor pressure (p_v) generated by the evaporating material as function of the absolute temperature (T) and its latent heat (L_{VAP}) [4]:

$$2.3\ log_{10}\ p_v(T) = \left(\frac{-L_{vap}}{R}\right)\left(\frac{1}{T}\right) + C \qquad (2.1)$$

where R is the gas constant and C is a constant of integration.

A minimum vapor pressure necessary to produce enough particles to achieve the substrate is $p_V > 10^{-2}$ torr [4]. A plot of the $\log_{10} p_V$ *vs* 1/T plot shows a straight line, according to equation 2.1, that shows the temperature required to achieve any vapor pressure of many materials. Such graphs may be verified at appendix B from reference [4].

2 Sample Characterization

2.1 X-Ray Diffraction (XRD)

X-Ray diffraction is an important source of information about structural aspects of crystalline materials since its discover in 1912 [5]. The XRD pattern is unique for each crystalline material, which allows the understanding and recognizing of crystalline structures of materials

[6,7]. Diffractograms of powder and thin film are capable of giving information about interplanar distances and position of the crystal plans through the Bragg's law, and to determine the crystalline structure of the material [6,8,9]. This law explains the diffraction of X-ray beams after collision and interaction with the electrons of the atoms of the material under investigation. Beams scattered are collected by the equipment detector, with constructive and destructive interferences [4], as shown in figure 2.4, and a graph of the X-ray intensity as function of the scattering angle is obtained.

Most of XRD measurements performed in this work were done in Rigaku DMAX at the Multiuser laboratory of UNESP campus Bauru. The equipment is equipped with CuKα beam and Ni filter to attenuate CuKβ radiation, at scan of 2θ/θ for powder mode and 2θ for thin films mode, with X-ray incident angle of 1.5°.

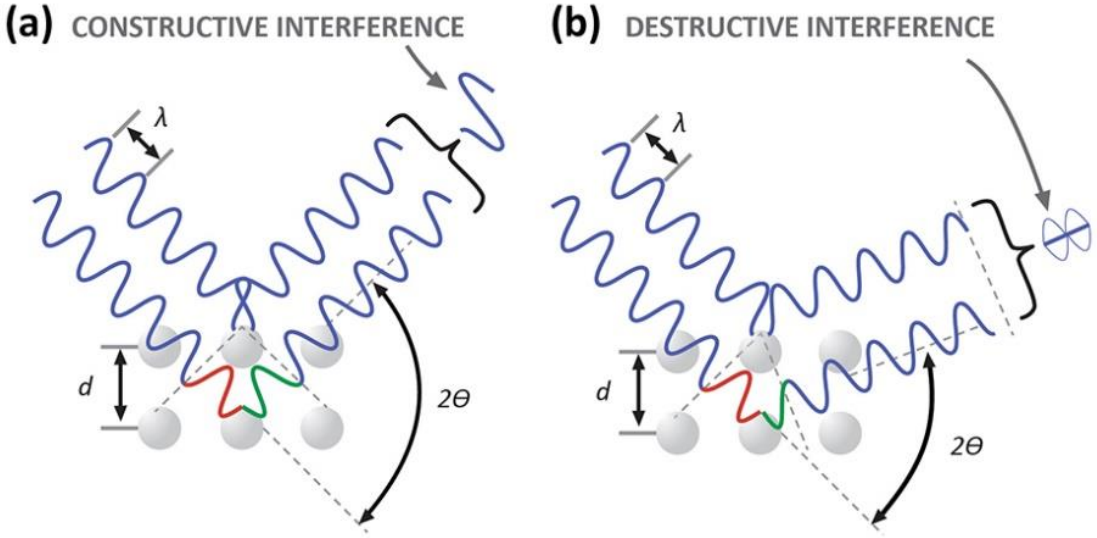

Figure 2.4: X-ray diffraction on a regular array of atoms, with incident angle that results in constructive interference (left diagram) and destructive interference (right diagram). (adapted from https://www.azom.com/article.aspx?ArticleID=3604, accessed in 27/11/2017)

2.2 Rutherford Backscattering Spectrometry (RBS)

The backscattering spectrometry is based on classical scattering in a central-force field. It consists basically in elastic hard-sphere collisions between the high kinetic energy particle ($^4He^{++}$ ion beam, the "projectile") and the stationary particle located on the sample (the "target") [4], as illustrated in figure 2.5a. An accelerator provides a collimated beam of particles that collides on the sample surface and the scattering of the projectile ions is collected by the detector, at certain θ angle, as shown in figure 2.5b.

This elemental-analysis technique is one of the most quantitative among all techniques [4]. High energy ions (MeV) undergo close-impact and scatters after collisions governed by the

well-known Coulomb repulsion between the positively charged nuclei of the target atom and positively charged projectile [10]. The kinematics of the collision and the scattering cross-section are independent of chemical bonding, therefore backscattering measurements are insensitive to electronic configuration or chemical bonding within the target [10]. RBS is commonly used to determine elemental concentrations and their depth profiles within the material, by analyzing the energy spectrum of the backscattered particles ($^4He^{++}$ ions) in experimental results and comparing with simulation ones.

In this work the RBS was performed at the Western University Tandetron Accelerator facility with a 2.5 MeV $^4He^{2+}$ ion beam and detection of backscattered ions at an angle of 170° using a silicon barrier detector in Cornell geometry.

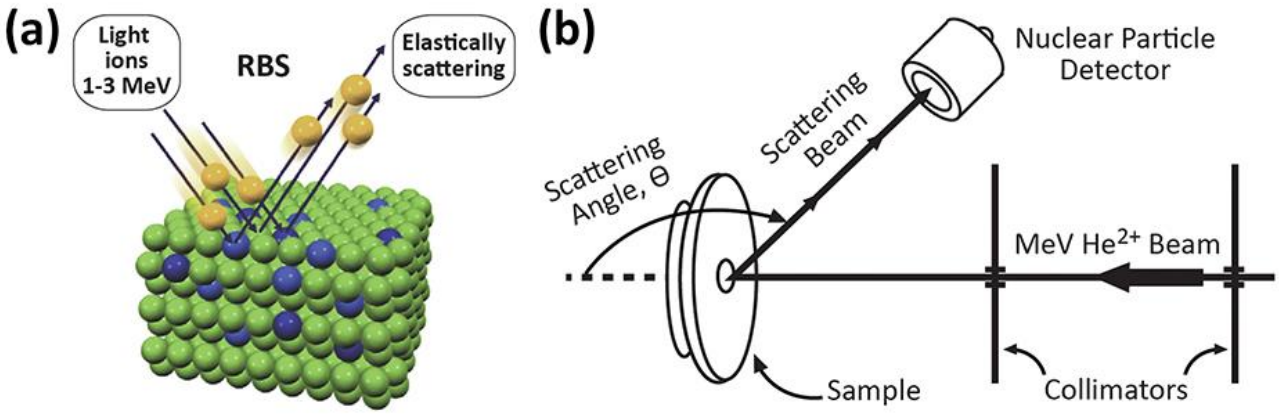

Figure 2.5: (a) The illustration of elastic collision between the beam ("projectile") and the material ("target"). **(b)** Experimental schematic of the RBS spectrometry. High energy collimated ions collide at the sample and the backscattered beam is collected on the detector at a θ angle. ((a) and (b) adapted from https://www.hzdr.de/db/Cms?pOid=29856&pNid=3537 (accessed in 27/11/2017) and [10], respectively).

2.3 Ultraviolet-Visible Transmittance Spectroscopy (UV-Vis)

Spectroscopy on the UV-Vis spectra is a method used to study the optical properties of materials by measuring their transmittance, absorbance and reflectance from the ultraviolet through the visible spectrum up to the near infrared. A parallel beam of monochromatic radiation at initial intensity (I_0) reaches the surface and a fraction of this intensity passes through the films and substrate, figure 2.6b. The beam interacts with the atoms, ions and electrons within the material [11] by absorbing or reflecting part of this electromagnetic energy, decreasing the final intensity (I) of the beam that reaches the sensor. The transmittance is the fraction of the intensity that passes through the sample ($T = [I/I_0] \times 100\%$) [11,12]. All materials present absorption and reflectance in some part of the electromagnetic spectrum, and this absorbed

energy is transformed in vibrations of the atoms in the lattice (phonons) or electronic transitions [13]. The transmittance is related to the optical absorption coefficient (α) of a material through the Beer-Lambert law [14] by the equation $\alpha=\log_{10}(1/T)$.

Figure 2.6a presents a generic plot of transmittance as function of incident angles, different of 90°, to show the transmittance dependence on incident angle. Some incident beams are refracted by the difference in the speed of light in the material and air, and some are reflected on the interfaces. Optical characterizations performed in this work occurred most in a Perkin Elmer system, model Lambda 1050, placed in the Multiuser laboratory under supervision of Prof. J. H. D. Silva at UNESP, campus Bauru.

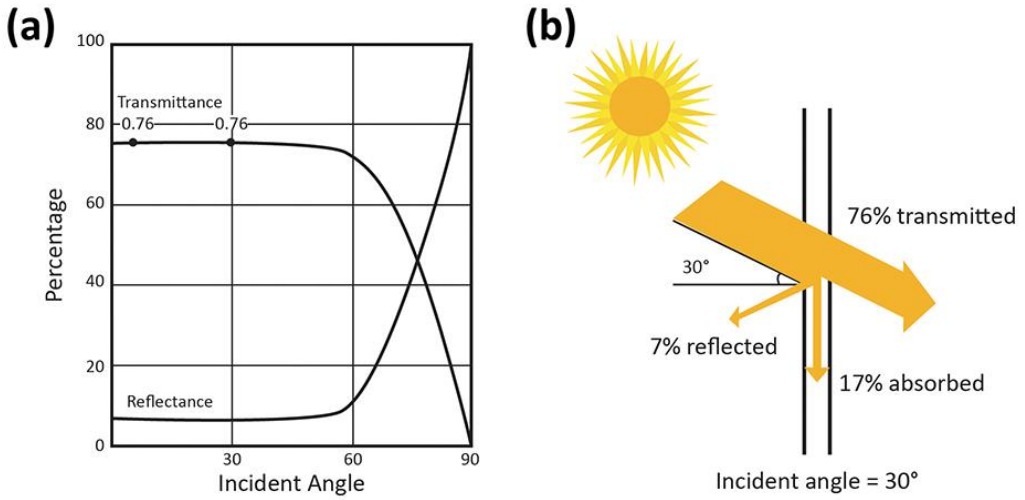

Figure 2.6: (a) Generic transmittance/reflectance as function of the incident angle (related to the normal) of electromagnetic beams on the surface of a material. **(b)** Diagram of the portions of light that are transmitted, absorbed and reflected, in a generic case with incident angle of 30°. (adapted from http://www.commercialwindows.org/transmittance.php, accessed in 27/11/2017).

2.3.1 Optical bandgap calculation

The optical bandgap (*Eg*) of materials can be obtained using the absorption coefficient in Tauc plots [15,16] accordingly to the equation 2.2. This equation has been largely used in literature to estimate the direct/indirect bandgap energy of mono/polycrystalline semiconductors and consists of an approximation, hence it was developed for amorphous materials where the absorption occurs due to band-to-band transitions [17].

$$\alpha h\nu = A\,(h\nu - E_g)^n \qquad (2.2)$$

where the $h\nu$ is the photon energy, A is a proportionality coefficient related to the structure of the nanocrystalline and/or amorphous materials, whereas n depends on the nature of electronic transitions at photon energies sufficiently close to the band gap. Specifically, $n = 2$ for indirect transitions, whereas $n = ½$ for direct transitions, or for non-direct transitions in disordered materials [14].

2.4 Confocal Laser Scanning Microscopy

Confocal microscopy is a non-destructive technique of optical sectioning that allows a 3D reconstruction of the surface of the material, as a topographic surface study [18]. It works similarly to optical microscope, where light is emitted through an aperture in a conjugated plan (confocal) with the sample, and a second aperture is positioned in front of the detector, as shown in figure 2.7. The rays of excitation light reach different focal planes of the sample and only scattered in-focus light rays reach the detector [18].

The Confocal microscopies were performed in a Leica DCM 3D placed at Multiuser Laboratory at UNESP, campus Bauru.

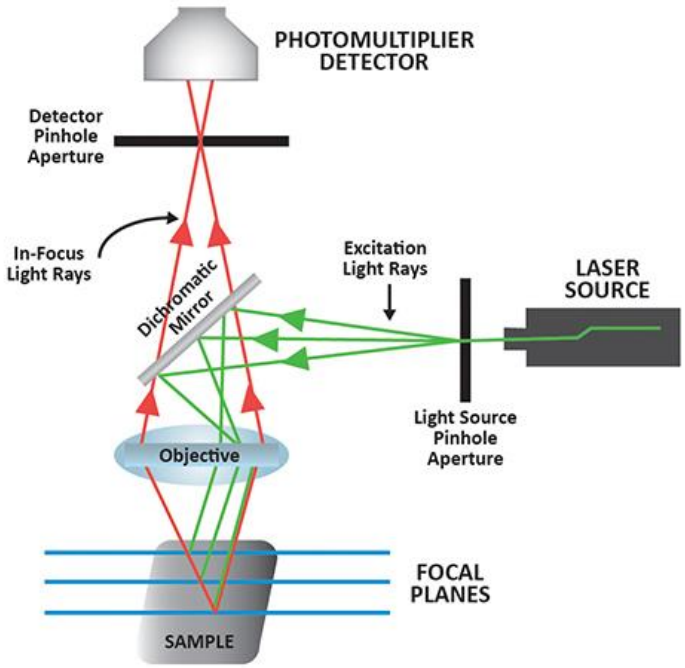

Figure 2.7: Schematic diagram of the confocal microscopy. (adapted from https://www.olympus-lifescience.com/de/microscope-resource/primer/techniques/confocal/confocalintro/, accessed in 27/11/2017)

2.5 Scanning Electron Microscopy (SEM)

SEM is a characterization used to study superficial microstructures with high resolution and large focus compared to optical microscopies. The equipment emits high kinetic electron beam with small diameter that scans determined area of the sample and the scattered electrons

are collected by a detector [19] well synchronized with the beam scan. The collected signal is the result of the interaction of the incident electron beam on the sample surface, that after scattering on the surface reaches the detector with different energies [19,20].

2.6 Energy Dispersive X-Ray Spectroscopy (EDX)

The EDX is used for qualitative compositional analysis through a scanning of a sample surface. This equipment is coupled to a SEM that uses its high kinetic electron beam to ionize the atoms in the sample. The atoms produce electromagnetic radiation, like X-rays, and other particles, as shown in figure 2.8, but only X-rays are collected by the EDX equipment sensor. The characteristic emitted X-rays related to specific atoms in the sample allow the determination of the elements present in the investigated sample region. A quantitative analysis can be done by comparing the peaks intensities of determined X-ray energy in the graph of X-ray intensity as function of X-ray energy [19].

Both SEM and EDX measurements were performed in Zeiss EVO 15 equipped with EDX sensor from Oxford Instruments. The equipment is located at UNESP, campus Bauru.

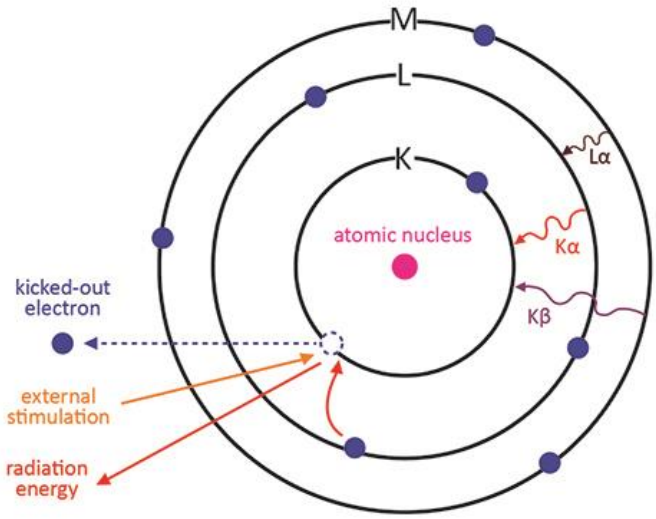

Figure 2.8: Schematic diagram of a EDX characterization. The electron beam collides on the atom and removes electrons from their orbits, that are rapidly replaced by other electrons at higher energy. This replacement causes the emission of electromagnetic radiation. (adapted from https://en.wikipedia.org/wiki/Energy-dispersive_X-ray_spectroscopy, accessed in 27/11/2017).

2.7 Atomic Force Microscopy (AFM)

AFM is a technique capable of manipulate the surface of materials and is also used to study these surfaces through imaging. Due to the high sensibility to surfaces forces, this equipment produces images through the scanning of the surface by measuring the reaction of the

forces between the probe tip and the sample surface. A schematic diagram of the AFM operating system is presented in figure 2.9.

The AFM measurements performed in this work were done at University of Western Ontario in a Witec GmbH, model Alpha 300S operating in non-contact mode, with 325-kHz cantilevers (model HQ-NSC15, Mikro-Masch Inc.).

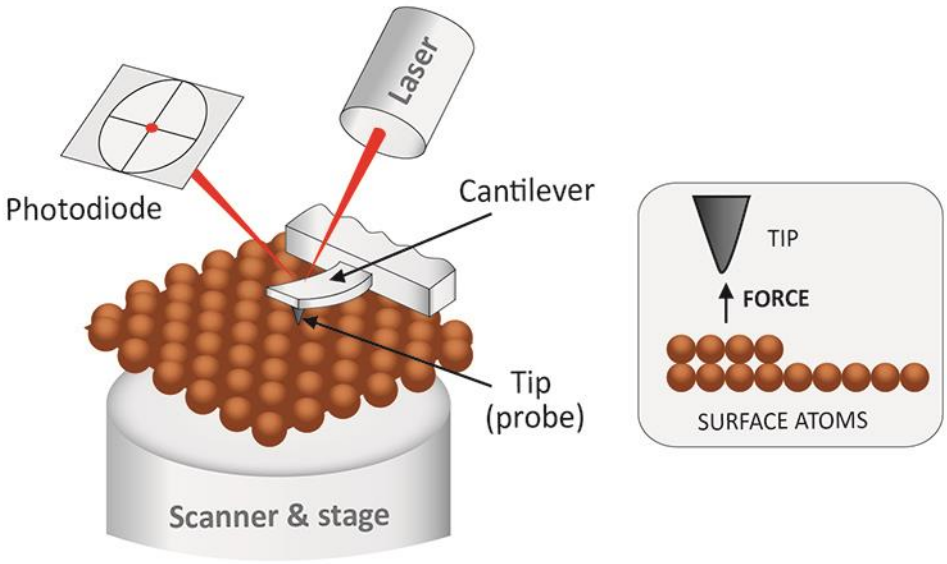

Figure 2.9: Diagram of the AFM technique. (adapted from http://www.farmfak.uu.se/farm/farmfyskem/instrumentation/afm.html and https://www.keysight.com/main/editorial.jspx?ckey=1774141&lc=por&cc=BR), accessed in 27/11/17.

2.8 Electrical Characterization

Electrical measurements such as current as function of the applied voltage and Impedance spectroscopy are very important to determine the electrical properties of materials [21,22].

The current as function of the voltage (I *vs* V) measures the current, that is the rate at which electric charge flows in a material, as function of a potential difference, the voltage, between the electrodes. The I *vs* V curves are the simplest electrical characterization to perform in order to obtain the electric resistance of a material. In this work, the equipment required for this measurement is either the electrometer or the sourcemeter, which may achieve high precision on the applied voltage and the obtained current.

Impedance spectroscopy is the technique that measures the impedance (Z), the opposition that a material or device presents to a current when a time-dependent voltage is applied. It is the extension of the concept of resistance (*R*) to AC circuits. The concept of impedance is necessary in AC circuits due to the effects of the alternating current on inductive

and capacitive elements such as the reactance (X), that is the imaginary part (j) of complex impedance, while the resistance forms the real part, as shown in the following equation $Z=R+j.X$.

Cyclic voltammetry and Impedance Spectrocopy were performed at UNESP, campus Bauru, in a Metrohm AutoLab PGSTAT302 equipment equipped with FRA32M module. The equipment is located at the Laboratory of New Materials and Devices (LNMD) under supervision of Prof. Dr. C. F. O. Graeff.

REFERENCES

[1] L. Ravaro, Influência da acidez da suspensão coloidal para a geração de defeitos pontuais e emissão no infravermelho em SnO2 dopado com Er, Thesis, UNESP, 2013.

[2] J. Livage, F. Beteille, C. Roux, M. Chatry, P. Davidson, Sol - Gel Synthesis of Oxide Materials, Acta Mater. 46 (1998) 743–750.

[3] T.A. Sigueira, J. N. Santos, S.C. Amico, C.F. Malfatti, Avaliação da influência do tratamento superficial nas propriedades mecânicas de camadas de difusão gasosa para PEMFC. (2013).

[4] D.L. Smith, Thin Film Deposition: Principles and Practice, 2nd ed., McGraw-Hill, New York, 1995.

[5] C. Kittel, Introdução à Física do Estado Sólido, 8th ed., LTC, Rio de Janeiro, 2006.

[6] B.D. Cullity, R. Stock, Elements of X-Ray Diffraction, 3rd ed., Prentice Hall, New Jersey, 2001.

[7] D.A. Skoog, F.J. Holler, T.A. Nieman, Princípios de análise instrumental, 5th ed., Bookman, Porto Alegre, 2002.

[8] J.F. Shackelford, Ciência dos Materiais, Pearson Prentice Hall, São Paulo, 2008.

[9] D.R. Askeland, P.P. Phulé, The Science and Engineering of Materials, 4th ed., Thomson, Pacific Grove, 2002.

[10] L.C. Feldman, Fundamentals of surface and thin film analysis, Elsevier Science Publishing Co, New York, 1986.

[11] G. Babu, Crystal Structure and Characterization of a Novel Organic Optical Crystal: 4-Chloro 3-nitrobenzophenone, Cryst. Res. Technol. 44 (2009) 561–566.

[12] W.D. Callister Jr, D.G. Rethwisch, Ciência e Engenharia de Materiais: Uma Introdução, 8th ed., LTC, Rio de Janeiro, 2012.

[13] J.C. dos Santos, Deposição e Caracterização de Filmes Finos de GaAs e de Al2O3 para utilização em transistores, Universidade Estadual Paulista, 2009.

[14] C. Terrier, J.P. Chatelon, J. a. Roger, Electrical and optical properties of Sb:SnO2 thin films obtained by the sol-gel method, Thin Solid Films. 295 (1997) 95–100. doi:10.1016/S0040-6090(96)09324-8.

[15] B.D. Viezbicke, S. Patel, B.E. Davis, D.P. Birnie, Evaluation of the Tauc method for

optical absorption edge determination: ZnO thin films as a model system, Phys. Status Solidi. 11 (2015) n/a-n/a. doi:10.1002/pssb.201552007.

[16] J. Tauc, R. Grigorovici, A. Vancu, Optical properties and electronic structure of amorphous germanium, Phy. stat. sol. 15, 627 (1966).

[17] J.I. Cisneros, Optical characterization of dielectric and semiconductor thin films by use of transmission data., Appl. Opt. 37 (1998) 5262–5270. doi:10.1364/AO.37.005262.

[18] A.R. Clarke, C.N. Eberhardt, Microscopy Techniques for Materials Science, WP, Cambridge, 2002.

[19] B.A. Dedavid, C.I. Gomes, G. Machado, Microscopia Eletrônica de Varredura: Aplicações e Preparação de amostras: Materiais poliméricos, metálicos e semicondutores, EDIPUCRS, Porto Alegre, 2007.

[20] A.M. Jorge Jr, W.J. Botta Filho, Microscopia Eletrônica de Varredura e sua utilização na resolução de problemas industriais, UFSCar, 2003.

[21] S.M. Sze, K.K. Ng, Physics of Semiconductor Devices, 3rd ed., Wiley, 2007.

[22] M.A.L. Pinheiro, Mecanismos de transporte elétrico excitados termicamente em SnO2 dopado com Ce, Universidade Estadual Paulista, 2008.

Chapter 3

SnO_2 based Thin Film Transistors*[1]

INTRODUCTION

This chapter presents a study on the sol-gel processed antimony-doped tin oxide (4 at% Sb:SnO_2) thin film as the semiconductor channel in Field Effect Thin Film Transistors (TFT). An investigation of transistor properties was done to understand the effects of longtime aging on antimony-doped tin oxide (ATO) solutions. The properties of the semiconductor layer and transistors, such as electron transport, mobility, on/off ratios, etc. are presented here in order to understand the non-reproducibility of different sol-gel solutions in same TFT assembly and deposition. The part of this chapter concerning the aging time of tin oxide solutions was published in the Journal of the American Ceramic Society [1] in collaboration with professors G. Fanchini and L.V. Goncharova from University of Western Ontario, Canada.

The deposition of PCBM (Phenyl-C_{61}-butyric acid methyl ester) on top of ATO based TFT devices was performed to investigate the hybrid heterostructure and the influences of the organic layer on the transistor active channel and TFT properties. Both semiconductor layers were obtained by cost-effective solution process and their junction applied in transistors is an original contribution.

Tin oxide (SnO_2) is a n-type inorganic semiconductor material with large bandgap of the order of 3.6 eV [2], high optical transparency in the UV-Vis region, low resistivity, and high thermal stability. These properties represent a promising and alternative low-cost transparent semiconducting material for application in transparent and flexible electronics, such as transistors, solar cells and sensors [1,3–7]. Presley et al. [8] demonstrated the fabrication of transparent TFTs utilizing ultrathin (10-20 nm) channel layers of SnO_2, with field-effect mobility of the order of 0.8 and 2.0 $cm^2/V.s$ in enhancement and depletion mode, respectively, with active layers grown by radio-frequency magnetron sputtering under ultrahigh vacuum. Although superior performance may be desirable for some specific applications and have been achieved with advanced growth techniques [4,7], low-cost growth methods are in even higher demand for

*[1] M. H. Boratto et al, Journal of the American Ceramic Society, 99, 12, 4000, 2016.

depositing transistor-grade-quality SnO_2. SnO_2 TFTs have been obtained at relatively low-cost process by sol-gel spin-coating method [9], but reproducibility and stability of these methods have normally been given little attention. Sol-gel is an attractive and low-cost technique with potential applications for tin oxide transparent and flexible electronics. Colloidal sol-gel methods have been successfully used to produce SnO_2 semiconductor nanocrystals of well-defined crystal structure and size-dependent electronic and thermal properties [10,11]. However, device reproducibility is still a serious issue to be resolved to make them competitive with other SnO_2 thin-film fabrication methods. Precursor solutions used in sol-gel processes are relatively concentrated and the formation of clusters and aggregates may evolve as a function of their aging time. Small fluctuations in the actual fabrication conditions and different aging times of solutions are parameters that may significantly affect the reproducibility of sol-gel-based tin-oxide devices. Small variations in the process parameters may be equally important. For instance, sol-gel processes are normally concluded by thermal annealing of the samples to nucleate solid crystallites in the semiconductor and eliminate undesirable adsorbed oxygen species and impurities originated from the solvents. Small fluctuations in the annealing temperature may lead to significant differences in crystallite size and device properties [12]. In this chapter the study of the Sb:SnO_2 solutions prepared by dialysis sol-gel process is presented, in order to identify the major factors of influence that may determine the non-reproducibility of SnO_2 based TFTs that impacts important properties of the semiconductor channel. Factors that contribute for characteristics of the samples and are considered in this work include: aging of the solution, local inhomogeneity in the thin solid films, and small fluctuations in the annealing temperatures.

The hybrid TFTs were also investigated in this work. The devices were obtained by the addition of the organic PCBM layer on the analyzed ATO TFTs in order to increase the ambipolar characteristics of the transistors. PCBM is a known n-type organic semiconductor with bandgap of about 2.4 eV commonly used as electron acceptor in organic photovoltaic cells [13,14]. Ambipolar devices are semiconductor devices in which both electrons and holes significantly participate in the conduction process through modulation via gate voltage, unlike most Field Effect Transistors (FETs) where the predominant transport occurs by only one type of charge carrier [15,16] that forms either a n-channel or a p-channel. The unipolar conduction occurs due to difficulties in accumulating the minority carrier through strong inversion condition, which is obstructed by traps within the semiconductor as well as at the semiconductor/insulator interface. Even intrinsic semiconductors present asymmetry between hole and electron conduction due to difference of bandwidth of the conduction and valence bands [16]. Factors that contribute to the efficient functioning of ambipolar transistors are the

charge carrier injection and the interface properties. Meijer and coworkers [17] show that ambipolar transport is observed experimentally by reducing the injection barriers by low bandgap semiconductors. Intensive research has been done to find a beneficial strong inversion condition by different strategies [16] to change a n-type FET into an ambipolar or even p-type FET by adjusting the electrode Schottky barrier [18] or doping the semiconductor [19]. Ambipolar charge transport is a desirable property for semiconductors as it enables the fabrication of more compact complementary logic circuits such as CMOS transistors with a single active layer [20]. Besides, it has been extensively used in high-speed circuits, power applications, and have the potential to be part of new devices such as light-emitting transistors [16,20].

Along with other transparent semiconducting oxides (TSO) like In_2O_3, ZnO and TiO_2, tin dioxide is a well-known inorganic n-type semiconductor that is widely tested for various electronic/optoelectronic applications as passive or active components [21]. Performance of p-type oxide materials are mainly limited by the low mobility of holes in the valence band compared to the higher mobility of electrons in the conduction band [21]. Tin monoxide (SnO) has bipolar behavior as consequence of its small bandgap (0.7 eV), small ionization potential (I_P) and large electron affinity (χ) that favors the alignment of both band edges to the source and drain electrodes of the transistors [21]. However, the SnO_2 presents small χ and large I_P that facilitates the n-type and p-type doping, respectively [22], and the ionic character of this semiconductor results in an oxygen-derived valence band (VB) with a dominant 2p character, and a metal-derived conduction band (CB) with a dominant 4s character that results in large bandgap and excellent n-type conduction when donor doped or with intrinsic non-stoichiometry that generates oxygen vacancies [22].

Most of organic semiconductor films display unipolar charge transport, and the majority of them are p-type, where conduction is dominated by holes [20]. However, the Phenyl-C_{61}-butyric acid methyl ester (PCBM), that is a soluble variety of fullerene, is a n-type organic semiconductor. This small molecule widely used as an electron acceptor in photovoltaic cells [14,23] has recently been applied in a cooperative combination with SnO_2 and exhibited improvements of all photovoltaic parameters compared to cells using only SnO_2 [23]. Also, a hole doping and electron trapping were detected in graphene by coupling this layer with C_{60}, which reinforces the widespread use of C_{60} derivatives as electron acceptors in organic photovoltaic devices [24]. In that work, authors identified the change in the transport properties of graphene induced by C_{60} through Raman and THz spectroscopies, and showed that the C_{60} thin film act as hole donor and electron acceptor for the graphene layer, presenting a hole doping concentration of 5.6×10^{12} cm^{-2} [24].

The organic-inorganic heterojunction promises hybrid materials with both the superior carrier mobility of inorganic semiconductors and the easy fabrication of organic materials [25] allowing its use in higher speed devices when compared to devices with a-Si or organic semiconductors. The characteristics of multilayer hybrid systems and their performance in devices depend on interfacial electronic interactions and charge transfer. In the context of photonic applications, the response of such hybrid materials to optical excitation and the role of interfacial charge transfer are of particular importance [24].

In the present chapter the ATO/PCBM is investigated on thin film transistors (TFT) and an improvement of the balance of bipolar characteristics is found in these devices. Section 1 of this chapter presents the methodology for obtaining the inorganic and organic semiconductors as well as the assembling of the TFTs. The section 2 focuses on the results and discussions of the SnO_2 and hybrid TFTs.

1 METHODOLOGY

1.1 SnO_2 based devices

The dialysis-based process used to prepare ATO started by dissolving 8.94 g of $SnCl_4 \cdot 5H_2O$ and 230 mg of antimony chloride ($SbCl_3$) in 50 mL of deionized water. Solution of 0.5 M were thus obtained at room temperature by magnetic stirring of these precursors. NH_4OH was subsequently added drop wise until reach pH = 11. Precursors were purchased from Sigma-Aldrich and used without purification. The solution was then transferred to semipermeable cellulose tubes (25 mm diameter, D9777, Sigma-Aldrich) to carry out the dialysis process. After 12 days, the suspension with reduced pH and with 0.05 M of 4 at% Sb:SnO_2 concentration in water was obtained. Two different colloidal suspensions were considered in this study: the first one was stored for 5 years prior to its use for thin-film transistor fabrication, whereas the second one was utilized no more than 2 weeks after preparation. The process conditions, starting materials, and concentrations were the same for both obtained suspensions. Solutions were concentrated up to 0.3 M by slow solvent evaporation at 100°C prior to their use for spin-coating deposition, to promote better adhesion and thin-film deposition on specific substrates. Three different substrates were used for thin-film deposition, characterization, and TFT fabrication: BK7 glass (Corning) and quartz were used for analytical characterization, whereas 10 mm x 10 mm pieces of highly doped n-type Si (100) wafers with 100 nm thick of thermally grown SiO_2 (Silicon Valley Microelectronics) were used for the fabrication of TFTs and electrical

characterization. All substrates were cleaned by four consecutive 15 min ultrasonic baths in detergent mixture, water, acetone, and methanol (in the bath sonicator model 8890, Cole-Parmer Inc.). Substrates were dried using a flow of medical-grade nitrogen prior to thin film depositions by spin-coating (model WS-400BZ-6NPP, Laurell Technology Co.) at 6000 rpm on all substrates. Two different sets of samples were prepared, and each set was annealed at either 450°C or 500°C in air.

For field-effect TFT fabrication, the ATO layer was deposited on the Si/SiO_2 substrate followed by aluminum evaporation, 200 nm thick, as electrodes. Metal contacts were thermally evaporated in chamber at low pressure (6×10^{-4} Pa) through a pre-patterned shadow mask (figure 3.1a and b) resulting in square electrodes of 800 μm x 800 μm distant from each other by 50 μm. The resulting contact arrangement produced a matrix of 4 x 2 electrodes, resulting in an array of four TFT devices on the same chip with 800 μm and 50 μm channel width (W) and length (L), respectively, as shown in figure 3.1c. This matrix of contacts on one single chip enables the investigation of the inhomogeneity effects on the transistors performance, at different locations along the x-axis. The aluminum electrode was chosen for the better alignment with the conduction band of the n-type semiconductors used in this work. The antimony doping on the SnO_2 layer was accomplished in order to optimize the charge injection by increasing the conductivity and reducing charge-trapping effects in the conduction channel of the inorganic layer [19]. It also drives de Fermi level towards the bottom of the conduction band [26].

The TFT structure consists of a metal-insulator-semiconductor (MIS) junction with two electrodes on the semiconductor $Sb:SnO_2$ layer. The Si/SiO_2 substrate works as the metal/insulator layers, where the SiO_2 works as the dielectric layer, while the highly doped n-type Si work as back gate. A droplet of graphite colloid (Pelco, Ted Pella, Inc.) is used on an edge of the gate to connect with the probe station.

Common features of devices with ambipolar conduction are the use of a low-work function metal for the electron-injection electrode and a high-work function metal for the hole-injection electrode. In this work only the Al that presents low-work function (~4.1 eV) was used [1,20].

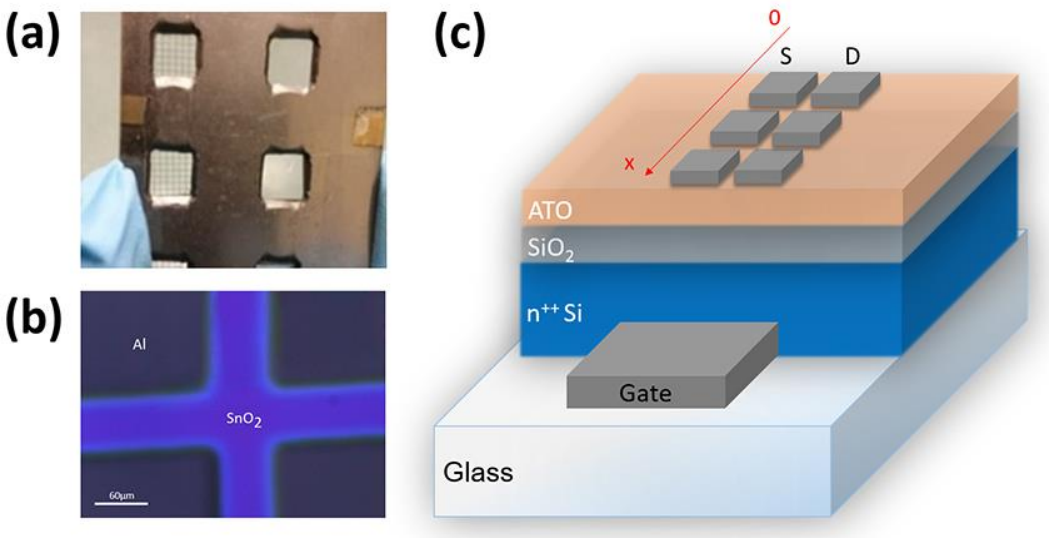

Figure 3.1: (a) Shadow mask for deposition of square shaped metallic electrodes (800 µm x 800 µm). **(b)** Optical image of the semiconducting channel among four different electrodes (corners) deposited on the sample. **(c)** Diagram of the TFT devices with top aluminum source-drain electrodes. The glass substrate is used to support the sample and hold the graphite gate connected to the Si substrate.

Electrical characterization of all devices was performed at room temperature using probes (model S725, Signatone) equipped with two source-meters (model 2400, Keithley), one for source–drain voltage sweep and current measurement, and the second for gate voltage scans. Source-meter control was automated using a National Instruments IEEE 488 interface operated by a custom-built MatlabTM (The MathWorks Inc.) routine. Unless otherwise noted, the values of the transistor performance parameters reported in the following sections refer to the average values of the transistors assembled on the same chip, whereas the uncertainties have been calculated from their standard deviations.

Thin-film transmittance measurements in the ultraviolet visible (UV-Vis) were recorded in the 200 – 600 nm range using an UV-Vis spectrophotometer (model DMS 80, Varian Inc.). The optical band gap of the ATO layer was subsequently determined by the Tauc plot [27,28]. The samples were also investigated by X-Ray diffractometry (XRD, with CPS detector, Inel Inc.) with instrument equipped with a CuKα radiation source operating in film configuration with fixed beam incidence angle of 5°. Sample morphology was characterized by Confocal microscopy (Leica, model DCM-3D), and Atomic Force Microscopy (AFM, model Alpha 300S, Witec GmbH) operating in tapping mode (non-contact) and mounting 325-kHz cantilevers (model HQ-NSC15, Mikro-Masch Inc.). Sample composition was investigated by Rutherford Backscattering Spectrometry (RBS). A 2.5 MeV $^{4}He^{2+}$ ion beam was used for these

measurements and the detection of backscattered ions was carried out at an angle of 170° using a silicon barrier detector in Cornell geometry [29].

1.2 PCBM

Solution of PCBM was obtained by dissolving its powder in chloroform, in a concentration of 1 mg/mL. The mix was dissolved in sonicating bath for 30 minutes and filtered through glass fiber filter of 0.1 μm prior to the deposition. The PCBM deposition occurred on the ATO TFTs after their characterizations. The deposition was performed by sinking part of the samples into a beaker with the filtered solution along with the solvent evaporation. The deposition occurred in room atmosphere and no enclosing was done on the PCBM layer after deposition to protect from oxygen exposure.

2 RESULTS

2.1 SnO_2 based TFTs

Additional analytical characterization of the ATO active layers was performed to gain insight into the differences between field-effect TFTs fabricated from solutions at different aging time, and to understand their electrical characteristics. The crystallinity was obtained using x-ray techniques, while their morphology and composition were obtained through AFM and RBS.

Figure 3.2 presents the comparison of the XRD patterns from ATO layers obtained from fresh and aged solutions. In both cases, the ATO thin films appear to be polycrystalline, with diffraction peaks that can be assigned to SnO_2 rutile tetragonal phase [3] (JCPDS, datasheet 088-0287). The XRD patterns also present contributions from the underlying amorphous SiO_2 layer due to the grazing angle at which the diffractograms are recorded. The mean crystallite size (MCS) of the SnO_2 rutile phase was estimated by means of Scherrer equation [30], by using the diffraction peaks corresponding to (110), (101), and (211) planes, as indicated in figure 3.2. The estimated crystallite size was found to be about the same in all the analyzed samples. The fact that crystallite sizes are at the nanometer-scale level suggests the films are relatively disordered in nature. On the other hand, the little dependence of MCS on the type of the solution indicates that the amount of disorder is similar in all cases and it is not a determining factor for the large differences on the devices characteristics, as will be verified at the end of this section.

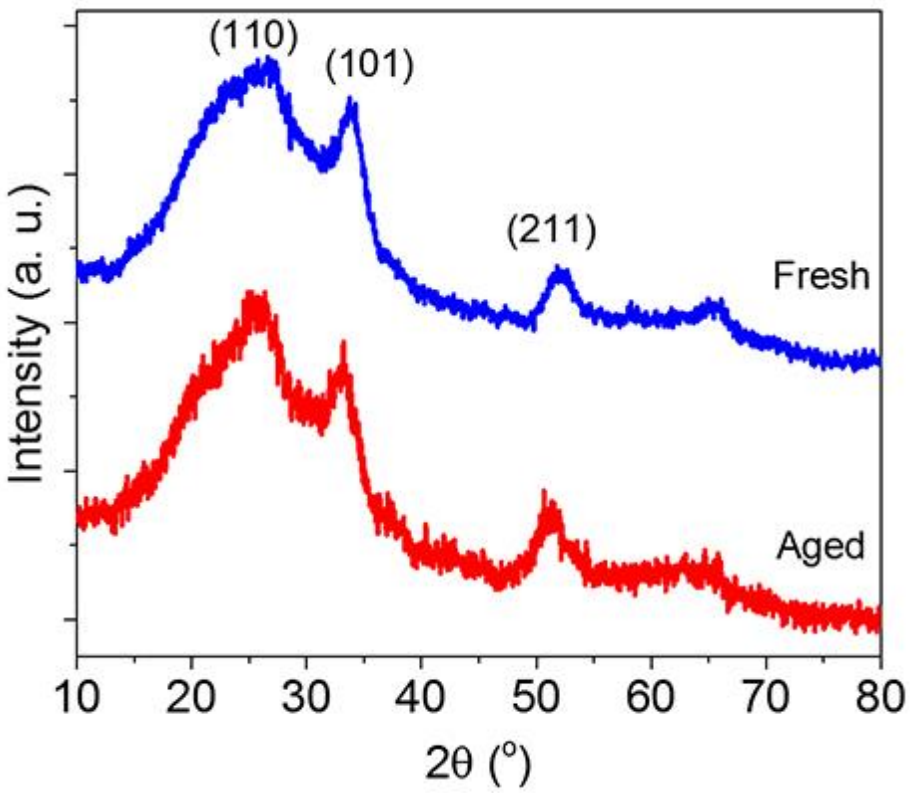

Figure 3.2: XRD of aged and fresh ATO thin film on glass substrate. Aged sample is annealed at 500°C and fresh one is annealed at 450°C. A polycrystalline thin film with SnO_2 rutile tetragonal structure is observed. The high amorphous contribution from the glass substrate is related to the high incident angle of the X-Ray beam.

Figures 3.3a and b compare the micrographs of two films deposited from aged and fresh solutions, respectively. From these images, it is apparent that both films are granular and present particles one order of magnitude larger than the 3 nm crystallite size determined from XRD data [31]. From a qualitative analysis of the AFM images it is convenient to observe that the particles are significantly larger in films made from fresh solution than the observed in films made by aged solution. This phenomenon may occur due to colloidal solution degradation along the aging process.

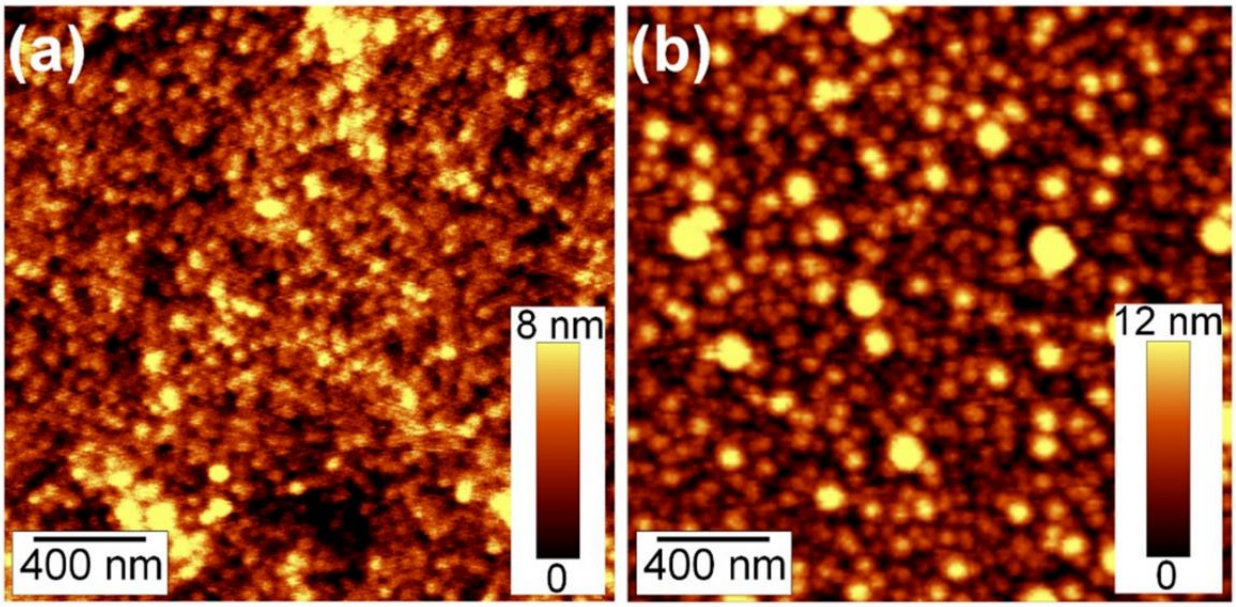

Figure 3.3: AFM topographic image obtained by tapping mode of the **(a)** thin film obtained from aged solution, and **(b)** thin film obtained from fresh solution where larger particles are observed.

To better understand the causes of different electron concentrations and electron mobility in samples made from the two types of solutions, an analysis of the total surface area of each sample must be done. Films obtained from aged solution present larger total surface area due to larger grain boundary area per unit volume. The grain boundaries are populated with the most of Sb ions [32], and the Sb centers in these regions may contribute to the formation of high concentration of defects [3,4,32,33]. This higher density of Sb ions at grain boundaries reduces the doping efficiency and consequently the charge carrier concentration in these samples.

Figure 3.4 shows the experimental and simulated RBS spectra for ATO thin films deposited on silicon substrates. The composition of the films from both samples was 0.04 Sb, 0.96 Sn and 1.94 O, which rules out the possibility that the different charge carrier concentrations is determined and assigned to different Sb contents. Therefore, it is perfectly consistent with RBS data that Sb reconstructs in different environments, consistently with the AFM results. The oxygen content is slightly under stoichiometry in both samples, which may account for the presence of oxygen vacancies at the grain boundaries.

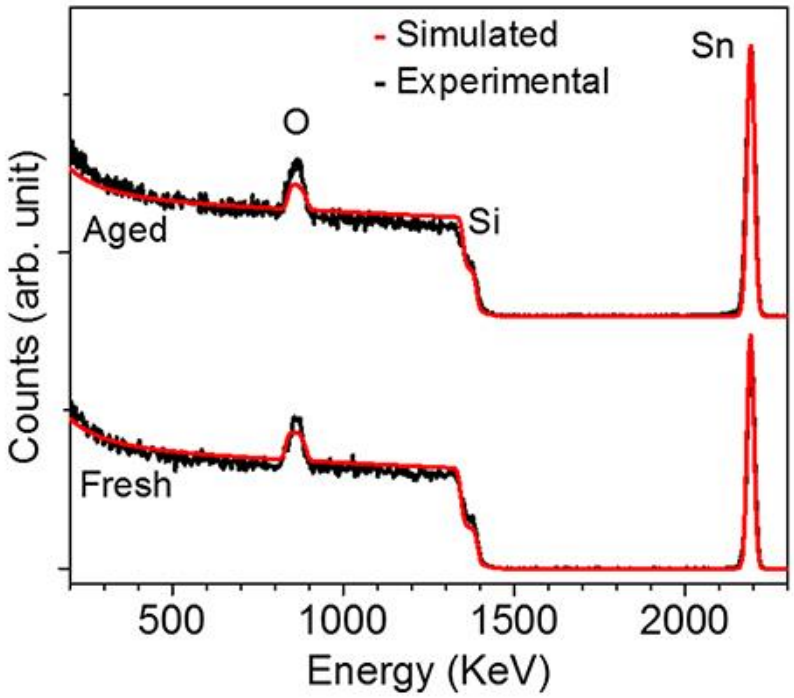

Figure 3.4: Experimental and simulated RBS data for Sb:SnO_2 films obtained from aged and fresh solutions, deposited on Si/SiO_2 substrates. Due to close atomic mass between Sb and Sn, their peaks are largely overlapping.

To acquire additional information about the degree of electron confinement in our active layer, the transmittance of the ATO at photon energy ($h\nu$) from 2.5 to 6.0 eV has been performed and is shown in figure 3.5a. Both films exhibit a transmittance of about 90 % in the entire visible range, which suggests that active layers prepared by this method may be suitable for transparent electronic devices [9,34]. Figures 3.5b and c present the determination of the bandgap energy (Eg) for thin films prepared from aged and fresh solutions, respectively. The optical bandgap of ATO films deposited from aged solution was estimated as Eg = 3.0 eV or Eg = 4.5 eV under the assumptions of indirect or direct transitions, respectively. The corresponding values extracted from ATO obtained from fresh solution were Eg = 3.25 eV and Eg = 4.0 eV. It can be noticed that the direct bandgap values are larger than Eg = 3.6 eV, the bandgap that is reported for crystalline SnO_2, assuming a direct-gap material [4,35–37]. This effect can be assigned to the disordered nature of our samples and electron confinement effects associated with it. A similar effect was observed in electrospun tin-oxide nanofibers with Eg > 4 eV where lateral electron confinement was present [2] and corroborates to the role played by electron confinement in our samples. Although the SnO_2 bandgap is said to be direct, there is also few works that present this semiconductor as an indirect bandgap material [11].

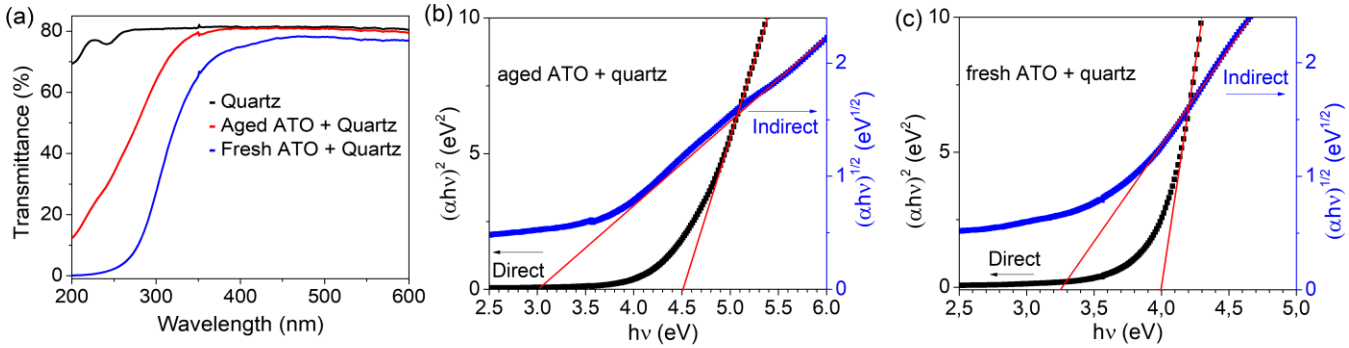

Figure 3.5: (a) Transmittance spectra in the near-ultraviolet and visible range for ATO thin films made from aged and fresh solution on quartz substrates and annealed at 500°C and 450°C, respectively. Allowed direct and indirect band gap transitions were obtained by Tauc plot **(b)** for films from aged, and **(c)** fresh solutions.

Figure 3.6 presents the electrical output characteristics for two different transistor samples. The two transistors have been selected randomly within the matrix presented in figure 3.1c. Both TFTs have an active layer with the thickness of 60 ± 20 nm.

A clear saturation trend can be observed in figure 3.6a for aged ATO devices at high drain (V_D) and low gate voltage (V_G). The channel pinch-off conditions ($V_D \geq V_G - V_T$) [8] are achieved in this sample due to the relatively low threshold voltage (V_T =-2 V). On the other hand, TFTs made from fresh solution with higher V_T (= -19 V) do not exhibit any current saturation and channel pinch-off conditions. Consequently, they require higher gate voltage to turn on the channel and higher negative gate voltages to turn it off. The consequence of high V_T is the low current modulation of the channel that produces low on/off ratio found in this sample [8,9].

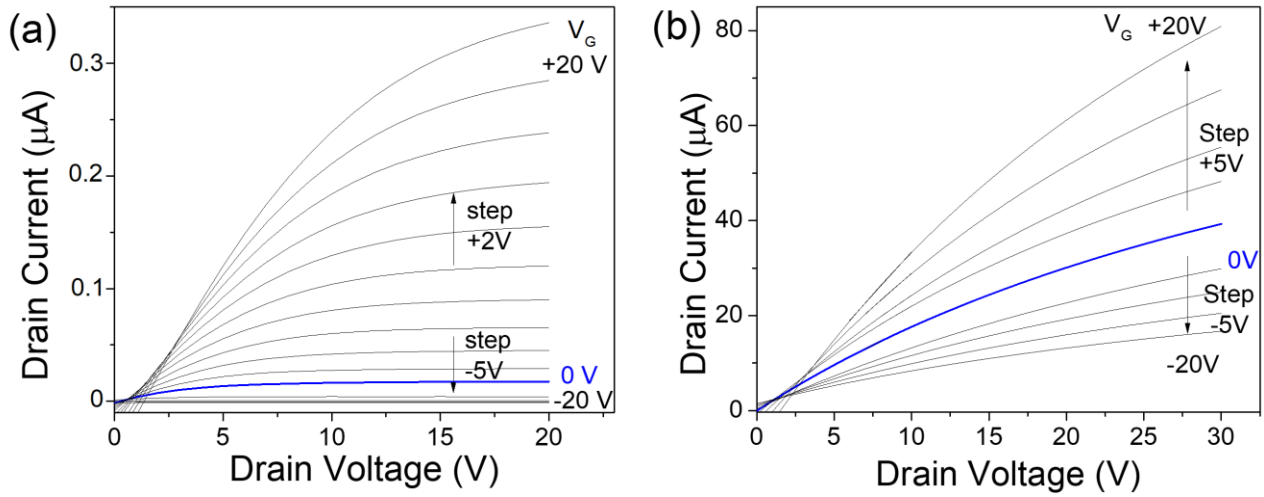

Figure 3.6: Output curves of ATO TFT obtained from **(a)** aged, and **(b)** fresh solution.

Figure 3.6 shows that both devices exhibit an active layer with n-type characteristics, as expected from donors present in the SnO_2 film, such as oxygen vacancies and Sb doping. This is noticeable from the increase in source–drain current (I_D) at increasing positive gate voltages (V_G). Despite the identical fabrication conditions, the two devices exhibit striking dissimilarities in electrical resistivity, about 200 times, which suggests a critical role of solution aging in such dissimilarity. The resistivity is $\varrho = 1.1 \pm 0.2$ Ω·m for films deposited from freshly prepared solution, and it is significantly higher when the aged solution is used: $\varrho = 220 \pm 40$ Ω·m. The latter is relatively high for Sb doped SnO_2 [38–43].

Figure 3.7 shows the transfer characteristics at constant drain voltage $V_D = 7$ V. The threshold voltages found are $V_T = -2.0 \pm 0.6$ V and $V_T = -19 \pm 2$ V for devices obtained from aged and fresh solution, respectively. Negative values of V_T indicate that these devices operate in depletion mode and present considerable current in the absence of gate bias [8,9,44]. This difference of V_T can also be assigned to considerable doping effects from antimony centers at high doping level (4 at.%) that leads to significant concentration of free carriers in devices made from fresh solution. Antimony located at grain boundaries give rise to oxygen vacancies [32,45] that may contribute to higher number of defects which produces smaller grains responsible for trapping free charge carriers in devices obtained from aged solutions. Such traps are responsible for releasing electrons upon applied gate bias. The on/off current ratio found in devices made from aged and fresh solutions are 100 ± 50 and 5 ± 2, respectively. It can be noticed that the uncertainties associated with performance fluctuations of devices assembled on the same chip are considerable (respectively, 50% and 40%), but the influence of the type of solution is even more significant. Specifically, the on/off current is more than 20 times larger after solution aging. The current is better modulated by electric field [8,9] in samples made from aged solution due to larger concentration of trapped carriers that are de-trapped under gate-bias.

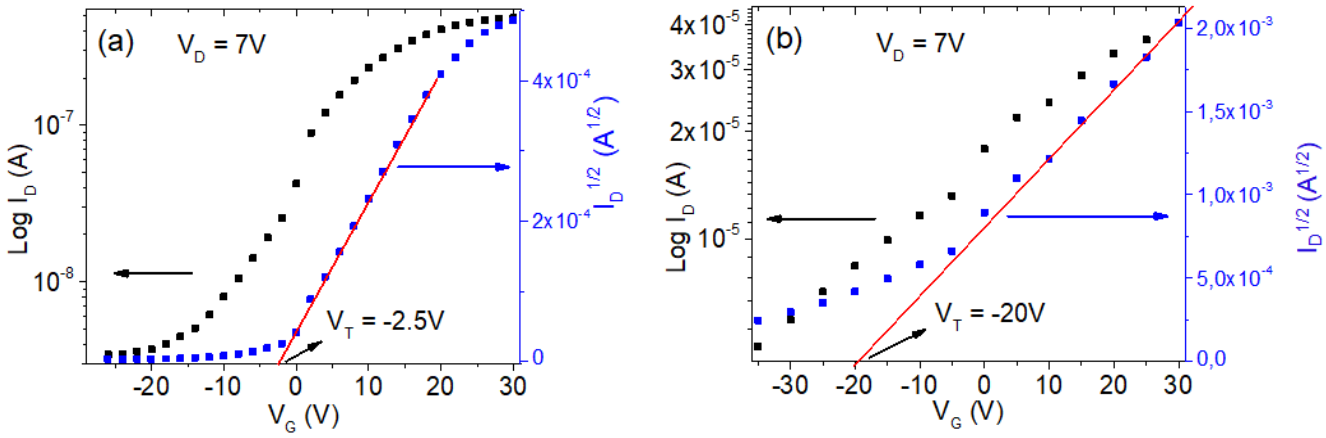

Figure 3.7: Transfer characteristic of one TFT device for each sample, at V_D = 7 V: **(a)** TFT fabricated from aged ATO solution shows on/off current ratio I_{ON}/I_{OFF} = 150 and threshold voltage V_T = -2.5 V. **(b)** TFT fabricated from fresh solution, which shows I_{ON}/I_{OFF} = 5 and V_T = -20 V.

The transconductance of TFTs built from both solutions are also obtained from the transfer curves presented in figure 3.7 through the equation 1.5 presented in chapter 1. The values differ by about two orders of magnitude: (2.9 ± 0.6) x 10^{-8} Ω^{-1} and (2.4 ± 0.3) x 10^{-6} Ω^{-1} for ATO devices prepared from aged and fresh solutions, respectively. As consequence of the different solutions, the different resistivity and transconductances corroborate to the importance of the aging time of the starting solution in the electrical properties of devices. The electron mobility (μ_e) of ATO was determined from the transconductances within the long-channel approximation [44]. It is very low for devices obtained from aged solution (μ_e = (4.6 ± 2) x 10^{-3} $cm^2/V.s$). However, a significantly higher mobility (μ_e = (3.3 ± 2) x 10^{-1} $cm^2/V.s$) is extracted from TFTs with active layers deposited from the fresh solution. The difference is about 70 times higher which suggests that solution aging has pronounced effect on electron mobility due to smaller grains, as seen in figure 3.3, that increases the electron scattering on the larger amount of grain boundaries present in the electron path [5,46]. The electron density (n_d) as function of the thin-film resistivity (ϱ) and mobility was calculated by the constitutive equation 3.1 [33,38]

$$n_d = 1 / (q \varrho \mu_e) \quad (3.1)$$

in which q is the elementary charge. Electron density n_d = (6.7 ± 1.2) x 10^{16} cm^{-3} and n_d = (2.7 ± 1.8) x 10^{17} cm^{-3} were obtained for films obtained by aged and fresh solution, respectively. The charge carrier concentration (n_e) was also calculated from equation 1.2 (in chapter 1) and the

values found are n_e = (4.5 ± 0.9) x 10^{11} cm^{-2} and (4.2 ± 0.4) x 10^{12} cm^{-2} for devices made from aged and fresh sol-gel, respectively. These values show that even though the n_d or n_e are about one order of magnitude higher in fresh solution based-devices the mobility was also increased, which may occur due to reduced number of defects [9,33], or, perhaps, to the donor level closer to the conduction band [9,47] in thin films made from the fresh solution. The gate leakage current is about 10^{-9} A at $V_G = 0$ in both cases and does not increase considerably at high applied V_G, thus, it does not affect the calculations in a significant way [9].

It was also explored the role of a relatively small increase of annealing temperature from 500 °C to 450 °C of active layers made from fresh solutions to investigate the effect of annealing temperature fluctuations on the TFT performance. Moreover, the effects of this variation in the devices properties were determined. A chip with four devices that were thermally annealed at 450 °C present electrical characteristics not dissimilar from their counterparts annealed at 500 °C. The most likely difference is in the n-type carrier concentration that increases about 40 %. This raise of the mean value of n_e at increasing temperature is accompanied by a consistent decrease of about 20 % of the on/off current ratio. The calculated values of field-effect mobility and threshold voltages are also within the standard deviation of the statistical set of data. Therefore, it is inferred from this analysis that small fluctuations in the annealing temperature are not as important as solution aging in determining the performance of sol-gel–processed ATO TFTs.

In summary, from electrical measurements of field-effect transistors, it is possible to evaluate the potential applications of either aged or fresh solution according to the electric characteristics of the resulting ATO thin films. A synthesis of the results obtained from the samples is presented in table 3.1. The properties of devices made from aged solution indicate they are still suitable for applications requiring high on/off ratio and low threshold voltage. On the other hand, devices made from fresh solution show higher mobility at a constant level of doping which indicates that a lower doping level should be desirable to achieve higher on/off current ratio and lower threshold voltage [48]. In general, it is apparent that the aging of the solution affects the TFTs performance, including field-effect mobility, density of charge carrier, on/off current ratio and threshold voltage more significantly than small fluctuations of thermal annealing temperature or local fluctuations of each film.

Table 3.1: Synthesis of the results obtained and discussed in this section.

Property	Aged samples	Fresh samples
Resistivity (Ω.m)	220 ± 40	1.1 ± 0.2
Electron density (cm^{-3})	(6.7 ± 1.2) x 10^{16}	(2.7 ± 1.8) x 10^{17}
Threshold voltage (V)	-2 ± 0.6	-19 ± 2
Transconductance (Ω^{-1})	(3 ± 0.6) x 10^{-8}	(2.4 ± 0.3) x 10^{-6}
Mobility ($cm^2/V.s$)	(4.6 ± 2) x 10^{-3}	(3.3 ± 2) x 10^{-1}
I_{ON}/I_{OFF}	100 ± 50	5 ± 2

2.2 SnO_2/PCBM based transistors

In this section, results concerning the junction of SnO_2 with organic PCBM are shown in order to compare SnO_2 TFT devices, studied and discussed in the previous section, with TFT devices with PCBM deposited. Figures 3.8a and b show a diagram and optical microscope image of the Al electrodes on ATO layer. Confocal microscopy was carried out on samples with PCBM organic layer deposited on the TFT devices to verify the surface homogeneity and PCBM effect on the electrodes and channels, as can be seen in figure 3.8c and d. The organic deposition occurred by sinking part of the TFT devices into a beaker with the fullerene-chloroform mixture. The deposition of PCBM on the Sb:SnO_2 surface occurred along with the solvent evaporation. The microscopy images, figures 3.8c and d, show that after the organic layer deposition the surface becomes non-homogeneous, marked by the presence of clusters of fullerene. Such clusters may appear possibly due to the long-time deposition, of about few hours, and exposure to room atmosphere. The presence of the clusters on the tin oxide surface may affect the inorganic layer as previously presented by Jnawali and collaborators [24]. Their work demonstrated the absence of relation between thickness of the fullerene and the charge-transfer effect on the C_{60}/graphene interface. Thus, in our samples may occur an overlay of non-homogeneous effects from surface regions without C_{60} clusters and regions where fullerenes are more concentrated. Charge transfer may occur through electron transfer from Sb:SnO_2 that are captured by unoccupied trap states in C_{60} clusters. These defects are associated with the influence of oxygen exposure of the organic layer during the deposition at room atmosphere.

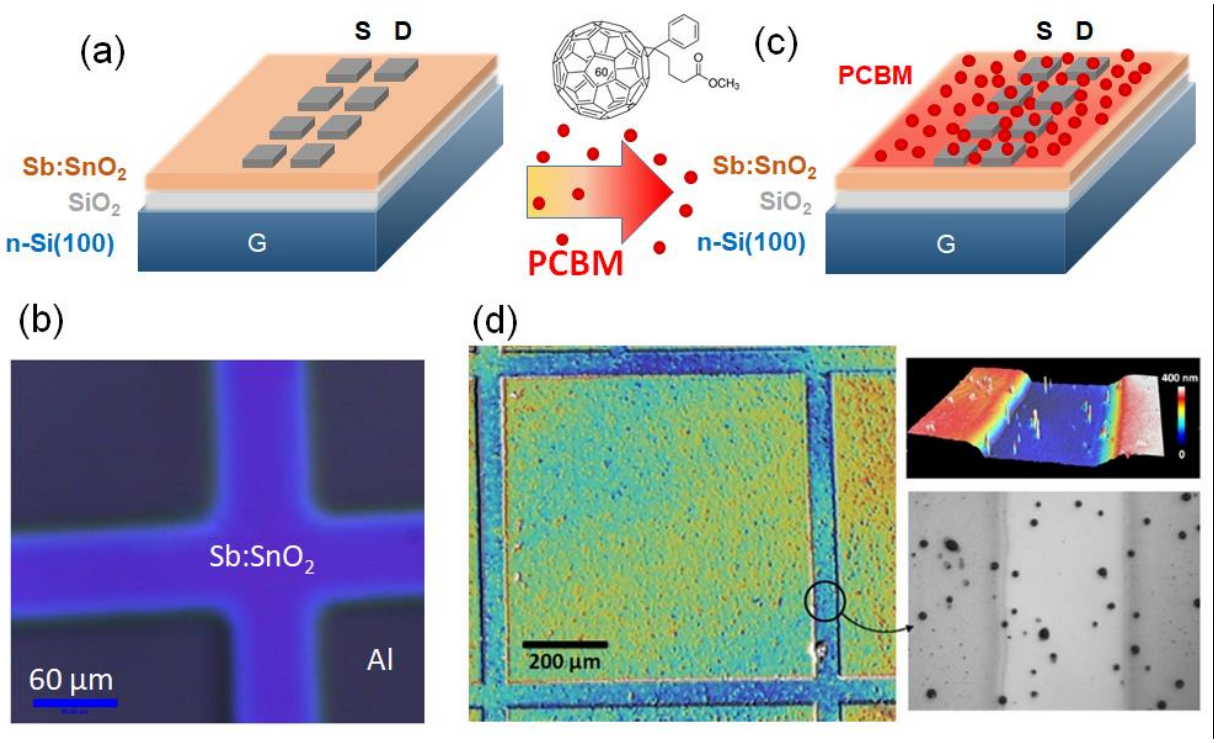

Figure 3.8: (a) FET arrays assembled on $Sb:SnO_2$. **(b)** Optical microscope image of the Al electrodes with channel width of 800 µm and length of 60 µm. **(c)** Schematic of the FETs surface after addition of PCBM. **(d)** Confocal microscopy of the transistor surface after deposition of PCBM. Inset shows an optical image of the channel and its respective confocal image.

The electrical output curves of the TFTs without and with PCBM on top of SnO_2 are shown in figure 3.9a and b, respectively. Black curves represent scans at $V_G > 0$, when the channel is expected to operate (in both panels) in electron accumulation mode. Blue curves are scans at $V_G = 0$. The ATO as well as the ATO/PCBM TFTs operate in accumulation mode upon application of positive gate bias through the increase of I_D. The application of a negative gate bias creates a depletion region in the channel that turns the device off (I_{OFF}). Further increase in negative bias takes the device to strong inversion condition that accumulates holes as charge carriers on the semiconductor/dielectric interface, thus increasing the electric current (red lines) [18]. When compared at positive applied gate voltage, the conduction by electrons is reduced after deposition of the organic layer, whereas, at negative gate bias a strong growth of conduction by holes is observed with the PCBM present on the devices. These results show the inorganic as well as the hybrid layer form a predominant n-type channel in the TFTs with significant enhancement of p-type characteristics after PCBM deposition.

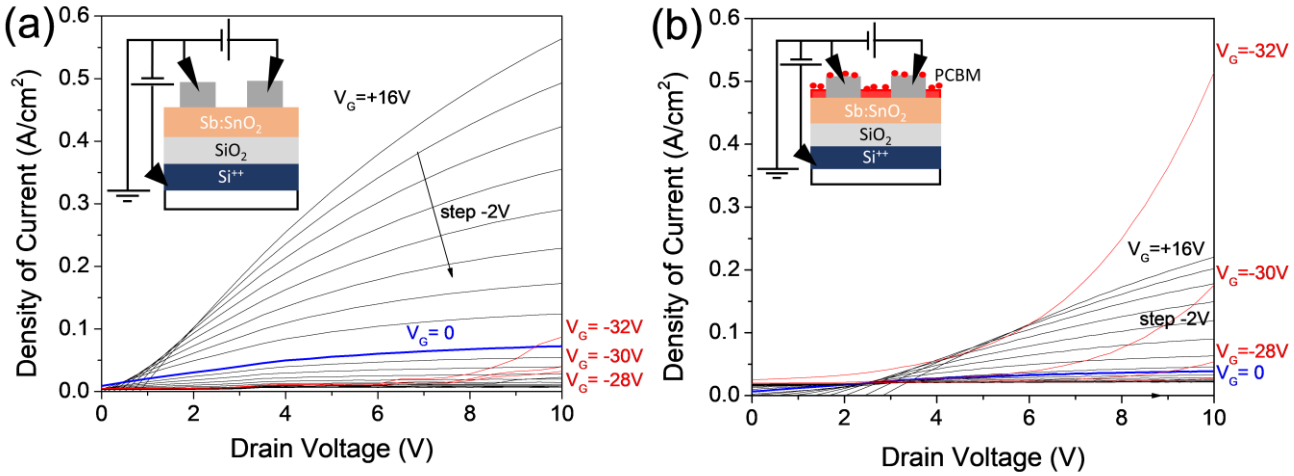

Figure 3.9: (a) Output curves of TFT devices based on Sb:SnO_2 and **(b)** on Sb:SnO_2/PCBM. Inset of both figures show the diagram of the devices and electrical circuits. Positive gate voltages are represented by black lines, $V_G = 0$ by blue ones, and high negative gate bias are represented by red ones.

The transfer characteristics are presented in figure 3.10 to better compare and understand the electrical contribution of the organic layer on the TFTs. The curves were taken at V_D = 10 V. The threshold voltages for electrons ($V_{T,e}$) and holes ($V_{T,h}$) at accumulation and inversion regimes are presented in the figure but also synthesized in table 3.2.

Table 3.2: The values of threshold for different charge carriers. $V_{T,e}$ for electrons, and $V_{T,h}$ for holes.

Sample	$V_{T,e}$ (V)	$V_{T,h}$ (V)
ATO	-12 ± 2	-26 ± 2
ATO/PCBM	-7 ± 1	-22 ± 3

It is noticed that at gate bias larger than threshold voltage for electron $V_G > V_{T,e}$ = -12 V on ATO devices, or $V_G > V_{T,e}$ = -7 V on ATO/PCBM devices the channels are turned on and start the electron accumulation conduction regime. On the other hand, the accumulation of holes, or strong inversion regime, starts at lower threshold voltage for the hybrid devices, $V_G < V_{T,h}$ = -22 V, while for ATO TFT it occurs only at $V_{T,h}$ = -26 V. Prior to PCBM deposition, weak hole current is present in inversion region which is changed into stronger current after PCBM deposition. This reduced threshold voltage for hole accumulation relocates the depletion regime towards positive gate voltages, which represents a more balanced hole-to-electron

concentration. The enhanced balance of electron and hole concentration within the semiconductor affects directly the electrical characteristics of the devices. Among the different characteristics between the two devices investigated, it is possible to verify that the reduced threshold voltages for holes and electrons occur due to significant increase of hole and decrease of electron densities, respectively.

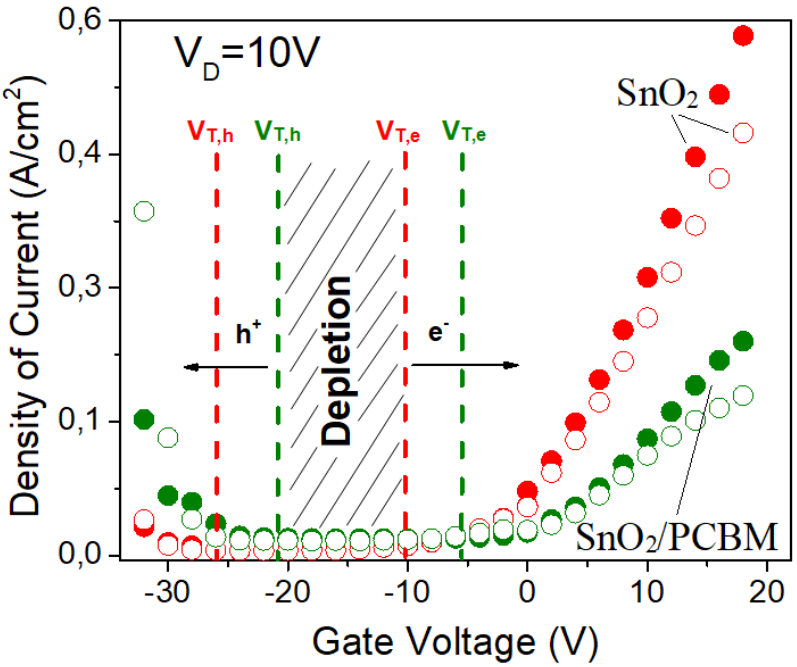

Figure 3.10: Transfer curves of the FET devices at V_D = 10V. Two different devices on same sample (filled and non-filled circles) are presented. Devices with (green) and without (red) PCBM layer. A $V_G > V_{T,e}$ is necessary to start conduction by electrons in accumulation regime, and $V_G > V_{T,h}$ is necessary to start conduction by holes in inversion regime. The depletion layer with no carrier charge moves to positive gate voltages after deposition of the PCBM layer on SnO_2.

As previously presented, it is possible to notice the important role caused by the fullerene changing the ionization potential of the SnO_2 at the ATO/PCBM interface. A downshift of the SnO_2 Fermi energy occurs due to the loss of electrons when in contact and equilibrium with the organic layer, as shown in figure 3.11a and b. The figure presents the interaction between the semiconductors where electrons are transferred from the inorganic to the organic layer. These charges are trapped on defects below the Fermi energy (E_F) of the PCBM that causes a downshift of the Sb:SnO_2 Fermi energy toward the valence band (fig. 3.11b). Creation of gap states from chemical defects and structural disorder on the SnO_2/PCBM interface are related to the reduction of electron density in the conduction band (CB) of the Sb:SnO_2 at positive gate bias [49] along with the capture of electrons by similar states in the acceptor organic layer [24]. After equilibrium, the Sb:SnO_2 valence band (VB) and CB are shifted toward the vacuum energy.

With lower E_{VB} and E_{CB} energies a better alignment occurs between the PCBM HOMO and the Sb:SnO_2 VB that increases the probability of injection of holes from the organic material under gate electric field.

At $V_G < V_{T,h}$, figure 3.11d, the holes are further accumulated in the Sb:SnO_2/SiO_2 interface due to E_F closer to intrinsic Fermi energy (E_{INT}) after equilibrium. The bended E_{INT} crosses the E_F at lower gate voltage and increases the hole concentration [44] that starts the strong inversion regime with electrical conduction by holes. This increase of positive charges available in the channel is responsible for filling traps that enables additional charges to move along the source-drain electric field with higher mobility [25].

Also, the upshifted Sb:SnO_2 VB allows better line up with the positive drain electrode, which improves the injection of holes from this electrode into the inorganic VB. The hole injection can be improved in order to enhance even more the ambipolar characteristic of the PCBM/Sb:SnO_2 FETs by reducing the Schottky barrier between the drain-electrode and the Sb:SnO_2 VB through the deposition of a metal electrode with higher work function [17,50], which would require lower applied V_G to bend the valence band and increase hole injection.

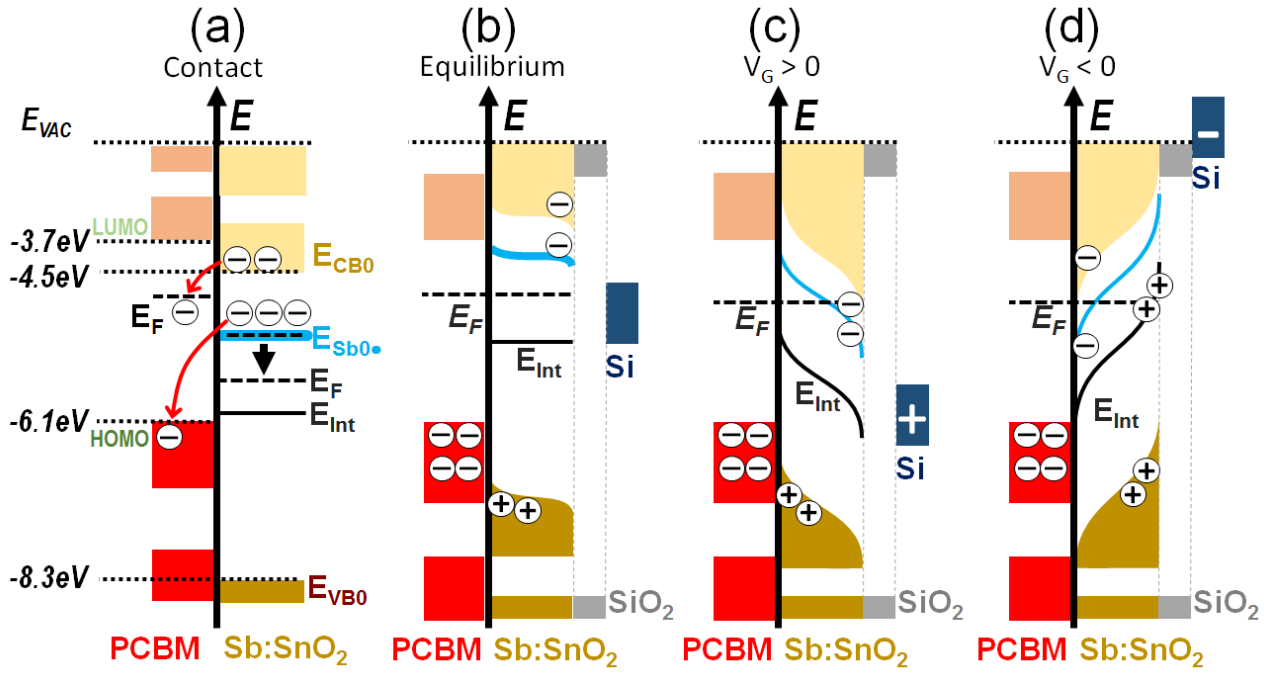

Figure 3.11: (a) Band diagrams of Sb:SnO_2 FETs in contact with PCBM layer. The Sb:SnO_2 valence (VB) and conduction bands (CB) are located at E_{VB} = -8.3 eV and E_{CB} = -4.5 eV, respectively. A Sb energy band is located at Fermi level (E_F) below Sb:SnO_2 CB. The PCBM LUMO and HOMO are located at -3.7 eV and -6.1 eV, respectively. After transfer of electrons from Sb:SnO_2 CB and Sb energy to PCBM traps below E_F and LUMO, a downshift of the Sb:SnO_2 E_F occurs before the **(b)** equilibrium is achieved, which leaves the Sb:SnO_2 with reduced density of electrons. **(c)** At $V_G > 0$ the lower concentration of electrons are attracted and form the conducting channel in the Sb:SnO_2/SiO_2 interface. **(d)** At $V_G < 0$ the holes are further accumulated in the Sb:SnO_2/SiO_2 interface due to E_F closer to intrinsic Fermi energy (E_{INT}). The bended E_{INT} crosses the E_F allowing the conduction by holes in the FETs.

The results reported here are in good agreement with PCBM/SnO_2 junction previous reported [23], and also to other works where other semiconductors are coupled with fullerenes. Jnawali and collaborators [24] have found that C_{60} layer deposited on graphene increases the graphene hole density and mobility by causing a downshift of graphene Fermi level by 160 meV. The trapping of electrons occurs by unoccupied trap states in C_{60} associated with the influence of oxygen exposure. Xiao et al [13] also found that the hole mobility and density are increased in organic semiconductor PCDTBT due to downward shift of the Fermi level.

The possibility of existing a film of PCBM on the Sb:SnO_2 surface may contribute to explain the higher inversion conduction present in this sample, where the conduction of holes could occur in the organic film. Although this may be a possibility to explain the higher ambipolar behavior on the PCBM/SnO_2 samples, the organic layer is farther than the inorganic one from the semiconductor/dielectric interface, where the conduction channel is formed due to the high electric field generated in the interface by the potential difference between gate and source electrodes.

Finally, we may summarize the matter presented in this section as a study of Thin Film Transistors with distinction on the influences of the PCBM on Sb:SnO_2 layer, where the organic works as a p-type dopant on the inorganic layer. The hybrid material obtained by this assembly demonstrated a higher ambipolar characteristic through higher inversion conduction at lower threshold voltages for holes. Also, a lower electron accumulation current related to the strong acceptor characteristic of the PCBM were verified in the devices investigated due to presence of defects trapping negative charges on the hybrid interface.

CONCLUSION

An investigation of the effects of long time aging solution on the electrical, optical, and electronic properties of sol-gel processed Sb:SnO_2 applied on TFT devices were presented. The results show that Sb:SnO_2-based transistors can be prepared regardless of the age of the solution, which, however, is important to determine the transistor characteristics. Specifically, higher electron mobility, carrier concentration and transconductance, along with lower sheet resistivity could be achieved from TFTs obtained from fresh solutions due to better Sb-doping efficiency observed in these samples. Degradation of aged solution led to slower nucleation of grains during the annealing process consequently leading to segregation of Sb ions into the grain boundaries. Although the performance of sol-gel–processed ATO TFTs are inferior than those from materials prepared through more expensive methods, the lower free carrier concentrations

achieved in devices made from aged solutions led to higher on/off ratios and lower threshold voltages, which are positive characteristics for TFT applications.

The investigation of the influence of the PCBM layer on ATO TFTs showed that the n-type organic semiconductor PCBM act as p-type dopant on the investigated devices, by capturing electrons and donating holes. Furthermore, even though the data suggests the increase of the hole density on SnO_2/PCBM devices, the hole concentration is not large enough to equilibrate the electrical conduction but contributes to a higher ambipolar characteristic on the active layer, which is desirable for applications in CMOS transistors or light-emitting transistors.

REFERENCES

[1] M.H. Boratto, L.V.A. Scalvi, L. V. Goncharova, G. Fanchini, Effects of Solution History on Sol-Gel Processed Tin-Oxide Thin-Film Transistors, J. Am. Ceram. Soc. 99 (2016) 4000–4006. doi:10.1111/jace.14459.

[2] Y. Wang, I. Ramos, J.J. Santiago-Avíls, Optical bandgap and photoconductance of electrospun tin oxide nanofibers, J. Appl. Phys. 102 (2007). doi:10.1063/1.2800261.

[3] L.P. Ravaro, L.V.A. Scalvi, M.H. Boratto, Improved electrical transport in lightly Er-doped sol–gel spin-coating SnO2 thin films, processed by photolithography, Appl. Phys. A Mater. Sci. Process. 118 (2014) 1419–1427. doi:10.1007/s00339-014-8900-7.

[4] C. Karunakaran, S. Sakthi Raadha, P. Gomathisankar, Microstructures and optical, electrical and photocatalytic properties of sonochemically and hydrothermally synthesized SnO2 nanoparticles, J. Alloys Compd. 549 (2013) 269–275. doi:10.1016/j.jallcom.2012.09.035.

[5] X. Liu, J. Wang, C. Liao, X. Xiao, S. Guo, C. Jiang, Z. Fan, T. Wang, X. Chen, W. Lu, W. Hu, L. Liao, Transparent, high-performance thin-film transistors with an InGaZnO/Aligned-SnO2-nanowire composite and their application in photodetectors, Adv. Mater. 26 (2014) 7399–7404. doi:10.1002/adma.201401732.

[6] Y. Li, W. Yin, R. Deng, R. Chen, J. Chen, Q. Yan, B. Yao, H. Sun, S.-H. Wei, T. Wu, Realizing a SnO2-based ultraviolet light-emitting diode via breaking the dipole-forbidden rule, NPG Asia Mater. 4 (2012) e30. doi:10.1038/am.2012.56.

[7] A. Oprea, E. Moretton, N. Bârsan, W.J. Becker, J. Wöllenstein, U. Weimar, Conduction model of SnO2 thin films based on conductance and Hall effect measurements, J. Appl. Phys. 100 (2006). doi:10.1063/1.2229802.

[8] R.E. Presley, C.L. Munsee, C.-H. Park, D. Hong, J.F. Wager, D. a Keszler, Tin oxide transparent thin-film transistors, J. Phys. D. Appl. Phys. 37 (2004) 2810–2813. doi:10.1088/0022-3727/37/20/006.

[9] G. Huang, L. Duan, G. Dong, D. Zhang, Y. Qiu, High-Mobility Solution-Processed Tin Oxide Thin-Film Transistors with High - κ Alumina Dielectric Working in Enhancement Mode, (2014). doi:10.1021/am5050295.

[10] C. McGinley, H. Borchert, M. Pflughoefft, S. Al Moussalami, A.R.B. de Castro, M. Haase, H. Weller, T. Möller, Dopant atom distribution and spatial confinement of conduction electrons in Sb-doped SnO2 nanoparticles, Phys. Rev. B. 64 (2001) 245312.

doi:10.1103/PhysRevB.64.245312.

[11] E.A. Floriano, L.V. de A. Scalvi, J.R. Sambrano, V. Geraldo, Evaluation of Bulk and Surfaces Absorption Edge Energy of Sol-Gel-Dip-Coating SnO 2 Thin Films, Mater. Res. 13 (2010) 437–443. doi:10.1590/S1516-14392010000400004.

[12] G. Cao, Y. Wang, Nanostructures and Nanomaterials - Synthesis, Properties, and Applications, 2nd ed., World Scientific Publishing, Singapure, 2011.

[13] Y. Xiao, H. Wang, S. Zhou, K. Yan, Z. Guan, S.-W. Tsang, J. Xu, Enhanced Performance of Polymeric Bulk Heterojunction Solar Cells via Molecular Doping with TFSA, ACS Appl. Mater. Interfaces. (2015) 150610093442002. doi:10.1021/acsami.5b02104.

[14] S. Yoo, J. Kum, S. Cho, Tuning the electronic band structure of PCBM by electron irradiation, Nanoscale Res. Lett. 6 (2011) 545. doi:10.1186/1556-276X-6-545.

[15] S.M. Sze, Semiconductor Devices: Physics and Technology, 2006. doi:10.1016/S0026-2692(82)80036-0.

[16] S.Z. Bisri, C. Piliego, J. Gao, M.A. Loi, Outlook and emerging semiconducting materials for ambipolar transistors, Adv. Mater. 26 (2014) 1176–1199. doi:10.1002/adma.201304280.

[17] E.J. Meijer, D.M. de Leeuw, S. Setayesh, E. van Veenendaal, B.H. Huisman, P.W.M. Blom, J.C. Hummelen, U. Scherf, J. Kadam, T.M. Klapwijk, Solution-processed ambipolar organic field-effect transistors and inverters., Nat. Mater. 2 (2003) 678–682. doi:10.1038/nmat978.

[18] M. Radosavljević, M. Freitag, K. V. Thadani, A.T. Johnson, Nonvolatile Molecular Memory Elements Based on Ambipolar Nanotube Field Effect Transistors, Nano Lett. 2 (2002) 761–764. doi:10.1021/nl025584c.

[19] S.-H. Lee, D. Khim, Y. Xu, J. Kim, W.-T. Park, D.-Y. Kim, Y.-Y. Noh, Simultaneous Improvement of Hole and Electron Injection in Organic Field-effect Transistors by Conjugated Polymer-wrapped Carbon Nanotube Interlayers, Sci. Rep. 5 (2015) 10407. doi:10.1038/srep10407.

[20] M. Muccini, A bright future for organic field-effect transistors, Nature Materials, 5 (2006) 605–613. doi:10.1038nmat1699.

[21] K.J. Saji, Y.P. Venkata Subbaiah, K. Tian, A. Tiwari, P-type SnO thin films and SnO/ZnO heterostructures for all-oxide electronic and optoelectronic device applications, Thin Solid Films. 605 (2016) 193–201. doi:10.1016/j.tsf.2015.09.026.

[22] N.F. Quackenbush, J.P. Allen, D.O. Scanlon, S. Sallis, J.A. Hewlett, A.S. Nandur, B. Chen, K.E. Smith, C. Weiland, D.A. Fischer, J.C. Woicik, B.E. White, G.W. Watson, L.F.J. Piper, Origin of the bipolar doping behavior of SnO from X-ray spectroscopy and density functional theory, Chem. Mater. 25 (2013) 3114–3123. doi:10.1021/cm401343a.

[23] W. Ke, D. Zhao, C. Xiao, C. Wang, A. Cimaroli, C. Grice, M. Yang, Z. Li, C.-S. Jiang, M. Al-Jassim, K. Zhu, M. Kanatzidis, G. Fang, Y. Yan, Cooperative tin oxide fullerene electron selective layers for high-performance planar perovskite solar cells, J. Mater. Chem. A. 0 (2016) 1–8. doi:10.1039/C6TA05095F.

[24] G. Jnawali, Y. Rao, J.H. Beck, N. Petrone, I. Kymissis, J. Hone, T.F. Heinz, Observation of Ground- and Excited-State Charge Transfer at the C60/Graphene Interface, ACS Nano. 9 (2015) 7175–7185. doi:10.1021/acsnano.5b01896.

[25] C.R. Kagan, D.B. Mitzi, C.D. Dimitrakopoulos, Organic-Inorganic Hybrid Materials as Semiconducting Channels in Thin-Film Field-Effect Transistors, Science, 286 (1999) 945–

947.

[26] E.A. Floriano, L.V.A. Scalvi, M.J. Saeki, J.R. Sambrano, Preparation of TiO2/SnO2 thin films by sol-gel method and periodic B3LyP simulations, Phys. Chem. A. 118 (2014) 5857–5865. doi:10.1021/jp411764t.

[27] J. Tauc, R. Grigorovici, A. Vancu, Optical properties and electronic structure of amorphous germanium, Phy. stat. sol. 15, 627 (1966).

[28] B.D. Viezbicke, S. Patel, B.E. Davis, D.P. Birnie, Evaluation of the Tauc method for optical absorption edge determination: ZnO thin films as a model system, Phys. Status Solidi. 11 (2015) n/a-n/a. doi:10.1002/pssb.201552007.

[29] M. Mayer, Rutherford Backscattering Spectrometry (RBS), Work. Nucl. Data Sci. Technol. Mater. Anal. (2003) 19–30. doi:10.1016/1359-6454(95)00193-X.

[30] B.D. Cullity, R. Stock, Elements of X-Ray Diffraction, 3rd ed., Prentice Hall, New Jersey, 2001.

[31] Z. Tian, C. Liang, J. Liu, H. Zhang, L. Zhang, Reactive and photocatalytic degradation of various water contaminants by laser ablation-derived SnOx nanoparticles in liquid, J. Mater. Chem. 21 (2011) 18242. doi:10.1039/c1jm12502h.

[32] V. Geraldo, V. Briois, L.V.A. Scalvi, C. V. Santilli, EXAFS investigation on Sb incorporation effects to electrical transport in SnO2 thin films deposited by sol-gel, J. Eur. Ceram. Soc. 27 (2007) 4265–4268. doi:10.1016/j.jeurceramsoc.2007.02.137.

[33] D.H. Zhang, H.L. Ma, Scattering mechanisms of charge carriers in transparent conducting oxide films, Appl. Phys. A Mater. Sci. Process. 62 (1996) 487–492. doi:10.1007/BF01567122.

[34] E.N. Dattoli, Q. Wan, W. Guo, Y. Chen, X. Pan, W. Lu, Fully Transparent Thin-Film Transistor Devices Based on SnO 2 Nanowires, Nano Lett. 7 (2007) 2463–2469. doi:10.1021/nl0712217.

[35] J. Robertson, B. Falabretti, Band offsets of high K gate oxides on III-V semiconductors, J. Appl. Phys. 100 (2006) 0–8. doi:10.1063/1.2213170.

[36] V. Geraldo, L.V.A. Scalvi, P.N. Lisboa-Filho, C. Morilla-Santos, Drude's model calculation rule on electrical transport in Sb-doped SnO2 thin films, deposited via sol-gel, J. Phys. Chem. Solids. 67 (2006) 1410–1415. doi:10.1016/j.jpcs.2006.01.102.

[37] T. Kololuoma, J.T. Rantala, Effect of argon plasma treatment on conductivity of sol-gel fabricated Sb-doped SnO2 thin films, Electron. Lett. 36 (2000) 172–173.

[38] C. Terrier, J.P. Chatelon, J. a. Roger, Electrical and optical properties of Sb:SnO2 thin films obtained by the sol-gel method, Thin Solid Films. 295 (1997) 95–100. doi:10.1016/S0040-6090(96)09324-8.

[39] B. Thangaraju, Structural and electrical studies on highly conducting spray deposited fluorine and antimony doped SnO2 thin films from SnCl2 precursor, Thin Solid Films. 402 (2002) 71–78. doi:10.1016/S0040-6090(01)01667-4.

[40] M.H. Boratto, L.V.A. Scalvi, J.L.B. Maciel Jr, M.J. Saeki, E.A. Floriano, Heterojunction between Al2O3 and SnO2 thin films for application in transparent FET, Mater. Res. 17 (2014) 1420–1426. doi:10.1590/1516-1439.285114.

[41] A. De, Opto-Electrical Study of Sol-Gel Derived Antimony Doped Tin Oxide Films on Glass, Trans. Elect. and electron. Mater. 16 (2015) 5–9.

[42] D. Arijit, Opto-Electrical Study of sol-gel Derived Antimony Doped Tin Oxide Films on

Glass, Trans. Electr. Electron. Mater. 16 (2015).

[43] T.G. Conti, A.J. Chiquito, R.O. da Silva, E. Longo, E.R. Leite, Electrical Properties of Highly Conducting SnO2: Sb Nanocrystals Synthesized using a Nonaqueous Sol-Gel Method, J. Am. Ceram. Soc. 93 (2010).

[44] G. Horowitz, Organic Field-Effect Transistors, Adv. Mater. 10 (1998) 365–377. doi:10.1002/(SICI)1521-4095(199803)10.

[45] J.S. Park, J.K. Jeong, Y.G. Mo, H.D. Kim, C.J. Kim, Control of threshold voltage in ZnO-based oxide thin film transistors, Appl. Phys. Lett. 93 (2008) 91–94. doi:10.1063/1.2963978.

[46] F.S. Kim, X. Guo, M.D. Watson, S.A. Jenekhe, High-mobility ambipolar transistors and high-gain inverters from a donor-acceptor copolymer semiconductor, Adv. Mater. 22 (2010) 478–482. doi:10.1002/adma.200901819.

[47] G. Adamopoulos, S. Thomas, P.H. Wöbkenberg, D.D.C. Bradley, M.A. McLachlan, T.D. Anthopoulos, High-mobility low-voltage ZnO and Li-doped ZnO transistors based on ZrO2 high-k dielectric grown by spray pyrolysis in ambient air, Adv. Mater. 23 (2011) 1894–1898. doi:10.1002/adma.201003935.

[48] L. Xu, Z. Dai, G. Duan, L. Guo, Y. Wang, H. Zhou, Y. Liu, W. Cai, Y. Wang, T. Li, Micro/Nano Gas Sensors: A New Strategy Towards In-Situ Wafer-Level Fabrication of High-Performance Gas Sensing Chips, Sci. Rep. 5 (2015) 10507. doi:10.1038/srep10507.

[49] A. Opitz, A. Wilke, P. Amsalem, M. Oehzelt, R.-P. Blum, J.P. Rabe, T. Mizokuro, U. Hörmann, R. Hansson, E. Moons, N. Koch, Organic heterojunctions: Contact-induced molecular reorientation, interface states, and charge re-distribution, Sci. Rep. 6 (2016) 21291. doi:10.1038/srep21291.

[50] S. Ezugwu, J.A. Paquette, V. Yadav, J.B. Gilroy, G. Fanchini, Design Criteria for Ultrathin Single-Layer Flash Memristors from an Organic Polyradical, Adv. Electron. Mater. (2016) 1600253. doi:10.1002/aelm.201600253.

Chapter 4

ZrO_2 based devices: The non-alkoxide method *

INTRODUCTION

The current chapter presents content recently published in the Ceramics International with the title "Annealing temperature influence on sol-gel processed zirconium oxide thin films for electronic applications".

Zirconium oxide (ZrO_2), also known as zirconia, is a ceramic material characterized by its hardness, high melt point (2700°C) and chemical inertness to acid and base. The zirconia ceramics are usually used as refractory materials in furnaces, laser mirrors, ionic conductors, pigments, and electronic devices [1]. This material occurs most naturally with monoclinic crystalline structure in the mineral baddeleyite. The phase diagram of pure zirconia shows at least three crystalline forms: monoclinic, tetragonal and cubic. The phase transitions, at room pressure, occur from: amorphous to metastable tetragonal at approximately 430°C; metastable tetragonal to monoclinic between 600-800°C; monoclinic to tetragonal between 950-1230 °C and from tetragonal to cubic at approximately 2370°C [1–3].

In order to find a substitute for SiO_2 in metal-oxide-semiconductor (MOS) devices, dielectric oxides with high dielectric constant (k), also called high-k, such as HfO_2, Al_2O_3 and ZrO_2 have been investigated and are suitable to improve the channel modulation and reduction of tunneling current in such devices even with thinner layers [4–6]. Zirconia is an optimal alternative due to its high dielectric constant (k = 18 - 26), wide bandgap (E_g = 4.7 - 7.8 eV), good thermal stability against silicate formation, excellent chemical inertness, and high breakdown field [7–10].

ZrO_2 thin film has become an interesting subject for researches due to their extensive use within a wide variety of technical and high-temperature applications such as catalysts, fuel cell technology and gas sensor applications [7]. Thus far, it has been one of the most promising oxides for functional and structural materials [7]. Along with properties of wide bandgap, high

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refractive index and low absorption ranging from 240 nm to ~8 μm, ZrO_2 based thin film is also suitable for use as active-waveguide sensors and coatings of optical filters in the ultraviolet to infrared spectral region [7,10–12].

ZrO_2 thin films are obtained for application in electronics by costly methods either at high temperatures (> 500°C) [13] or by high vacuum methods, such as reactive sputtering, atomic layer deposition (ALD) [8,11], electron beam evaporation [14], oxidation of Zr film by thermo-oxidation or ultraviolet ozone [10], and pulsed layer deposition. The approach of sol-gel deposition for ZrO_2 thin films offers besides the reduced cost, significant technical/application advantages, such as the simple and fast fabrication process [7]. The preparation of ZrO_2 thin films at low temperature remains challenging and many approaches have been proposed to decrease the process temperature for fabrication of zirconia films on both glass and flexible substrates [13,15–18].

This chapter presents a study of homogeneous, non-porous and stable ZrO_2 obtained by the non-alkoxide method, which is well known for obtainment of porous films [19] and powders. An investigation of the influences of the thermal annealing temperature on the elemental composition is done to better understand these relations with the electrical properties of the zirconia thin films. The films were deposited on substrate, applied in Thin Film Transistors (TFT) and Metal Insulator Metal (MIM) capacitors to verify their properties and evaluate their possible application in electronic devices.

Section 1 of this chapter presents the methodology to obtain the colloidal solution, films and devices assembled. Section 2 presents the characterizations and results related to the films and devices. The dielectric films were deposited on substrates of glass, quartz, Si/SiO_2, and ITO/PEN, whose use depend on specific characterizations.

1 METHODOLOGY

This section describes the methods for obtaining the chemical solution of zirconia by the non-alkoxide method along with the preparation of thin films and devices.

1.1 Preparation of colloidal suspension

The stable ZrO_2 solution was obtained through the method proposed by Chiavacci and coworkers [19], by using zirconyl chloride precursor ($ZrOCl_2 \cdot 8H_2O$) dissolved in hydrochloric acid (HCl) added dropwise to a warm (80 °C) solution of sulfuric acid (H_2SO_4) at 0.21 M, in a

molar ratio of Zr^{4+}:H_2SO_4 of 3:1. The final volume of 500 mL produced at concentration of 0.2 M suffered dialysis against distilled water reaching the colloidal suspension at pH 1.6 and concentration of 0.1 M [17,20]. To increase the viscosity, 100 mL of the solution was concentrated at 98 °C until final volumes (and concentrations) of 25 mL (0.4 M) and 10 mL (1.0 M) are reached. The concentrated solution was used for thin film deposition without any supplementary step.

Zirconia powder was obtained by completely evaporating the solution at 98 °C. The as-obtained material was used for thermal characterization (TGA/DSC) and structural analysis (XRD) to obtain information about phase changes, mass losses and the crystalline structure. Thermal Gravimetric Analysis (TGA) and Differential Scanning Calorimetry (DSC) were carried out using a STA 409 (Netzsch) with a rate of 10 °C/min from 50 °C to 1200 °C in a controlled N_2 atmosphere. The powders annealed at 1000 °C for 1 hour were also investigated through X-Ray Diffraction (XRD) in a Rigaku DMAX with CuKα beam, Ni filter, at scan of 2θ/θ from 10° to 80°.

Different substrates of quartz, glass, indium tin oxide coated polyethylene naphthalate (ITO/PEN) and Si/SiO_2 were used for thin film deposition for specific characterizations. The cleaning of the substrates followed two steps under sonication bath: 1) in a mixture of water and detergent, and 2) in isopropyl alcohol. In different cases, the films were deposited by spin-coating at 3000 rpm for 1 min, and by dip-coating at 100 mm/min with different intermediate and final thermal annealing (TA) procedures. Annealing was performed to eliminate the organic and solvent residues to obtain the ZrO_2 film. Even though most of the literature reports that under thermal annealing higher than 400 °C the amorphous zirconia changes to metastable tetragonal phase (t-ZrO_2), Soo and collaborators [7] show that coated substrates baked under infrared lamp followed by annealing at 450 °C results in amorphous ZrO_2.

Deposition of 4 layers of ZrO_2 on Si/SiO_2 occurred by spin-coating the concentrated zirconia solution (1.0 M) at 3,000 rpm followed by thermal annealing after the deposition of the last layer. These samples were used for Rutherford Backscattering (RBS) and Atomic Force Microscopy (AFM) characterizations to study the films composition and morphology. The AFM analysis was performed in a Witec GmbH model Alpha 300S. RBS result helps the verification of the elimination of solvent residues from the precursor solution in the zirconia film. The RBS measurement was performed at the Western University Tandetron Accelerator facility, using the $^4He^{2+}$ beam with energy of 2.5 MeV and the silicon barrier detector in Cornell geometry at an angle of 170°. The data analysis and simulation were done with SIMNRA software [21].

ZrO_2 thin films deposited on quartz substrate were used for UV-Vis-NIR transmittance that was carried out in a spectrophotometer Varian Inc, model DMS 80 to verify the transparency on the UV-Vis-nIR spectra and the bandgap of the dielectric material. Deposition of zirconia thin films by dip-coating on glass substrates followed by TA at 450 °C for 1 h were also investigated through XRD with scan of 2θ and incident angle of 1.5°.

1.2 Preparation of films and devices

A preliminary study was performed to define the suspension concentration to be used to deposit zirconia thin films. The higher concentration of the sol-gel suspension revealed to produce more uniform films, with less pores. Therefore, the zirconia layers were obtained from suspension with 1 M concentration.

A first deposition of ZrO_2 on Si/SiO_2 was specifically done for Rutherford Backscattering Spectrometry (RBS) characterization to evaluate the film composition as function of the TA temperature, and to check the elimination of solvent residues from the solution. The films were deposited by spin-coating at 3000 rpm, with a total of four layers and TA only after the last one.

The assemble of devices with ZrO_2 film (figure 4.1a) occurred with the deposition of this film on soda-lime glass substrate by dip-coating of four layers, using the solution at concentration of 1 M and thermal annealing at 450°C for 1 hour after the deposition of the last layer. The evaporation of indium electrodes for electrical measurements were performed on top of the dielectric layer. The thickness of the electrodes and channel length are 100 nm and 300 μm, respectively.

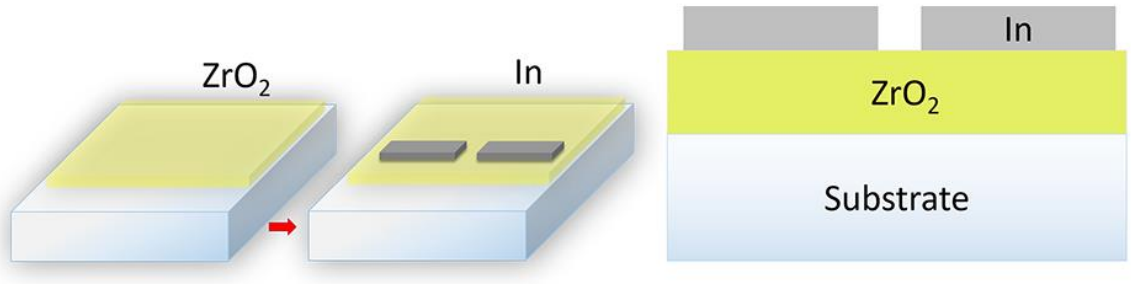


Figure 4.1: Zirconia on glass substrate with channel length of 300 μm for planar electrical characterization.

Thin film transistors (TFT) were also assembled to investigate the field-effect properties of the zirconia layer as dielectric. The TFT was mounted with ZrO_2 deposited by dip-coating on top of 100 nm thick Al (gate) electrode followed by the deposition of SnO_2 as shown in figure 4.2a. The obtaining method of tin oxide sol-gel was previously described in chapter 3. A total of 5 layers deposited by dip-coating at 100 mm/min was obtained. Calcination at 200°C for 10 minutes after each layer and annealing at T = 400°C for 1 hour were performed on the transistor. 100 nm thick Al top electrodes were evaporated on top of the semiconductor as drain and source electrodes. MIM capacitors were obtained by dip-coating 2 layers of ZrO_2 with intermediary and final TA at 450°C for 10 and 60 minutes, respectively. The same deposition occurred also on flexible and transparent ITO/PEN substrates. In these substrates the ITO layer acts as bottom electrode and a top Al electrode is evaporated to finish the device. A schematic diagram of the steps to obtain the employed MIM devices is presented in Fig. 4.2b and c.

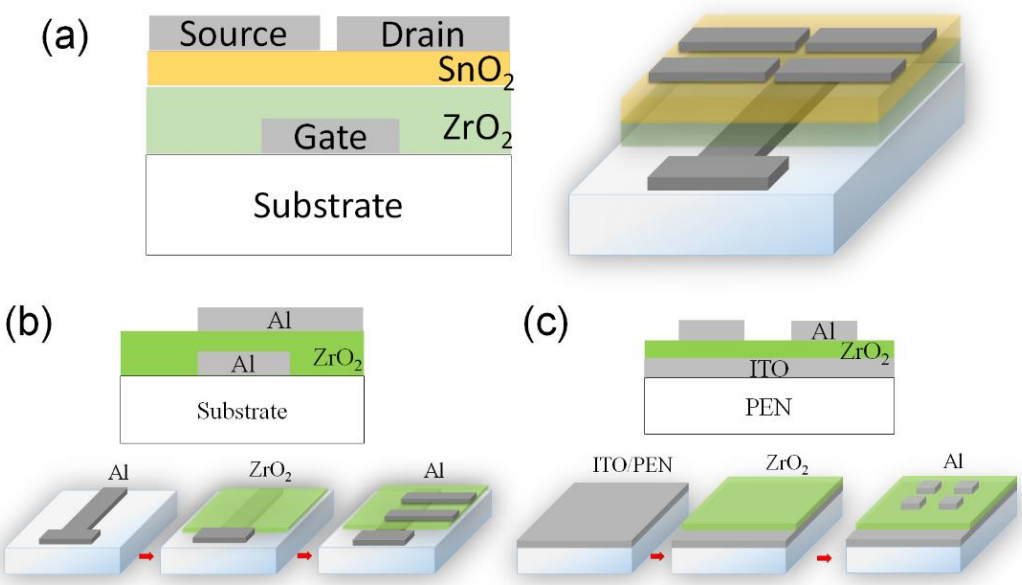


Figure 4.2: (a) The zirconia based TFT with aluminum electrodes and tin oxide as semiconducting layer. **(b)** Obtaining steps of the zirconia thin film-based metal-insulator-metal capacitor on glass substrate, and on **(c)** ITO/PEN flexible substrates. The top square aluminum electrode presents area A = 0.04 cm^2.

2 RESULTS

This section presents the characterizations, results and discussion related to ZrO_2 thin film and devices based on ZrO_2 fabricated by the non-alkoxide method.

The characterizations were obtained by UV-Vis transmittance, Rutherford Backscattering Spectrometry (RBS), Atomic Force Microscopy (AFM), Energy Dispersive X-rays Spectroscopy (EDX), Confocal microscopy, X-Ray Diffraction (XRD), Thermal Gravimetric Analysis (TGA) and Differential Scanning Calorimetry (DSC), and electrical measurements such as IxV curves and Impedance Spectroscopy (IS).

2.1 XRD of film and powder

Zirconia powder thermally annealed at 1000 °C for 1 hour and thin films thermally annealed at 450 °C for 1 hour were analyzed by XRD to investigate the crystallinity of the samples obtained by the non-alkoxide method. The XRD was performed in a Rigaku DMAX with CuK_α beam, at scan of $2\theta/\theta$ for powders and 2θ for films. Ni filter were used in order to eliminate the CuK_β radiation. The incident angle for thin film configuration was 1.5°. Figure 4.3a shows the diffractogram of the thin films with amorphous structure even with TA at 450 °C. On the other hand, the powder thermal annealed at 1000 °C shows high crystallinity with monoclinic structure, figure 4.3b (JCPDS #100-8297).

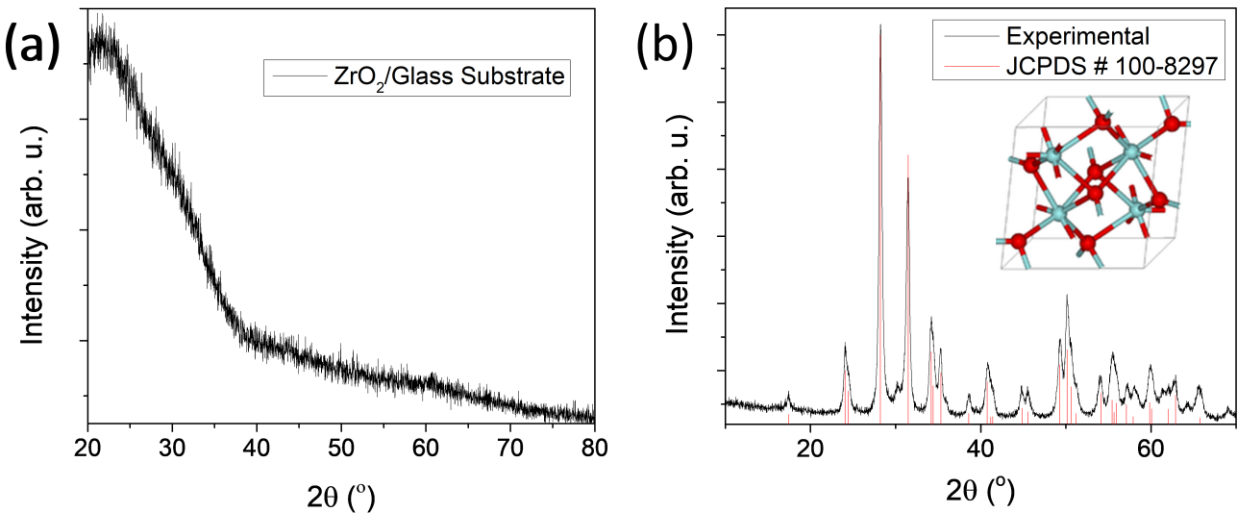


Figure 4.3: (a) Diffractogram of the zirconia thin film after TA at 450°C and **(b)** powder after TA at 1000 °C for 1 hour. Inset of (b): ZrO_2 monoclinic structure with Zr atoms in red, and O atoms in blue.

2.2 Thermal analysis

In order to understand the temperature-induced mass loss occurring during the sample annealing, TGA/DSC measurements were performed on zirconia powder. The results show the release of compounds from the precursor solution and thermal processes (endo/exothermal)

occurring during the material heating. Thermal Gravimetric Analysis (TGA) and Differential Scanning Calorimetry (DSC) was carried out with a rate of 10 °C/min from 50 °C to 1200 °C in a controlled N_2 atmosphere in a STA 409 from Netzsch equipment.

The results are shown in figure 4.4 where it is possible to see a mass loss up to 15% from 100 to 350 °C, probably due to the elimination of adsorbed water and hydroxyl groups (ZrO_2-OH) in the range 150-250 °C, and Cl_2 in the range of 300-400 °C. From 350 to 700 °C another significant mass loss (about 15%) is noticeable probably due to the elimination of SO_4, as also reported by Rizzato et al [20]. Up to 350 °C the density of the solid remains the same through the volume reduction that follows the mass reduction, although the density decreases above 350°C probably as consequence of the increase of porosity due to gaseous species evolution related to Cl_2, ClO_X, S, and SO_X compounds.

The DSC curve shows endothermic peaks at 142 °C and 342 °C that may be related to the temperatures that start to promote the liberation of Cl_2 and SO_4. The endothermic peak at 655 °C is probably related to the phase-transition from metastable tetragonal to monoclinic. This monoclinic structure of the zirconia annealed at 1000 °C is also observed in XRD data (figure 4.3b). An overall mass loss of approximately 35 wt.% is achieved until the end of the temperature ramp [7].

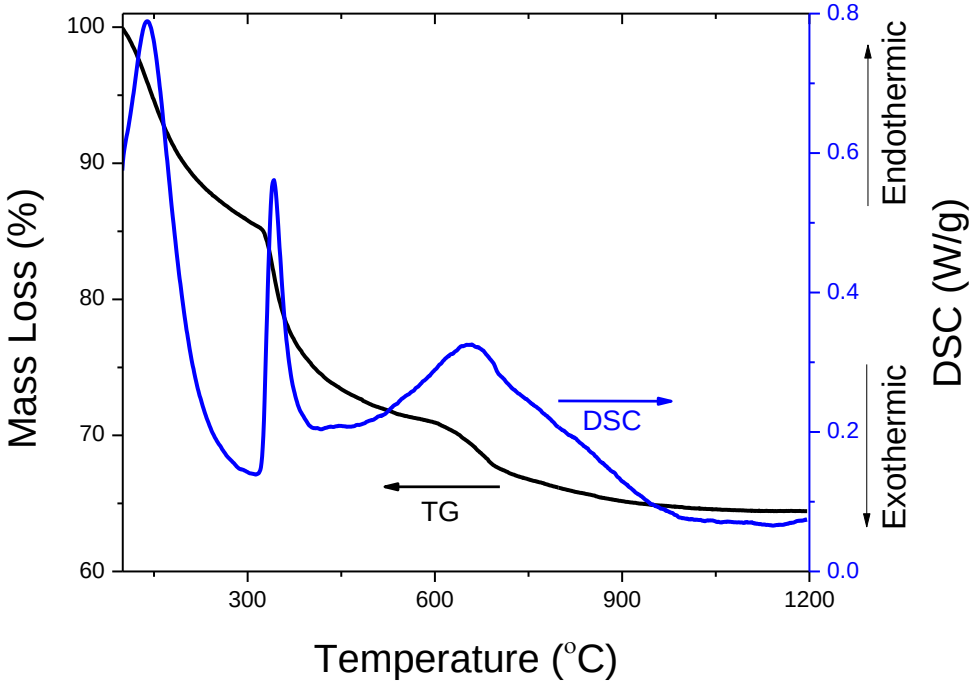


Figure 4.4: TG/DSC curves of the powder of ZrO_2.

2.3 Rutherford Backscattering Spectrometry (RBS)

To verify the surface homogeneity and composition of the thin films obtained from the non-alkoxide method and compare with the results presented by TG/DSC, the suspension 1 M was used to deposit thin films on Si/SiO_2 substrates with a total of 4 layers without intermediate calcination but with final thermal annealing in the temperature range of 250-450°C for 1 hour. The samples were characterized by Rutherford Backscattering Spectrometry (RBS) and the data analysis through simulation was carried out with the help of SIMNRA software [21].

Figure 4.5a shows the RBS experimental and simulated data of 4 layers of ZrO_2 thin film spin-coated and thermal annealed at 450°C after the last layer. The continuous experimental curve represents a homogeneous and regular thin film surface. The composition of the ZrO_2 film shows presence of hafnium (Hf) at concentration of 0.5%. This element is found as impurity in the $ZrOCl_2 \cdot 8H_2O$ precursor used to produce the sol-gel suspension. The residual presence of Cl and S from the precursor solution is due to zirconia film deposition of four layers with thermal annealing only after the last layer. The total removal of Cl_2 and SO_4 at 350 °C and 500 °C [20] are not achieved due to superficial elimination and subsequently trapping of these elements within the first layers. Figure 4.5b shows the dependence of the annealing temperature to eliminate the S and Cl elements. The initial atomic concentration of S and Cl in the films thermally annealed at 250 °C was 7% and 0.8%, respectively. After increase in the annealing temperature (up to 450 °C) the concentration of S reduced to 5.5% and Cl reduced to 0.6%, following a linear reduction as function of the temperature. The total specific reduction of the impurities is 21% for S and 25% for Cl. Once more, the considerable concentration of these elements is due to their incorporation within the first deposited layers with no thermal annealing.

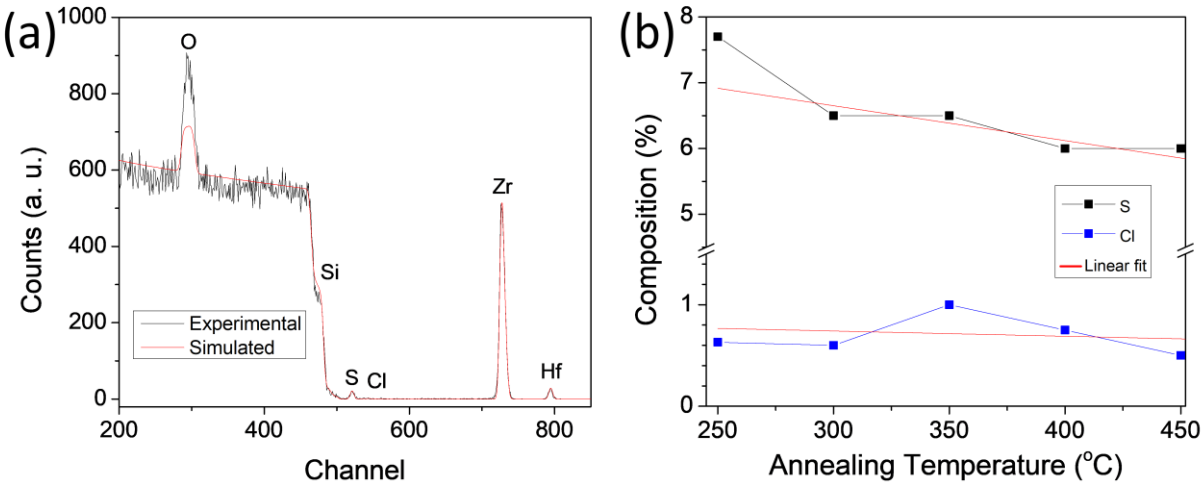


Figure 4.5: (a) RBS experimental and simulated data of the ZrO_2 spin-coated on SiO_2/Si substrate. **(b)** Composition of S and Cl in the ZrO_2 films as function of the annealing temperature.

2.4 Atomic Force Microscopy (AFM)

The zirconia deposited on silicon substrate with TA at 450 °C previously characterized by RBS was also characterized by AFM, as shown in figure 4.6. The image presents a homogeneous and non-porous surface reinforcing the findings of RBS measurements. Figure 4.6b with higher amplification shows that the sample present granular surface with low roughness, as detailed in the cross-section profile (inset).

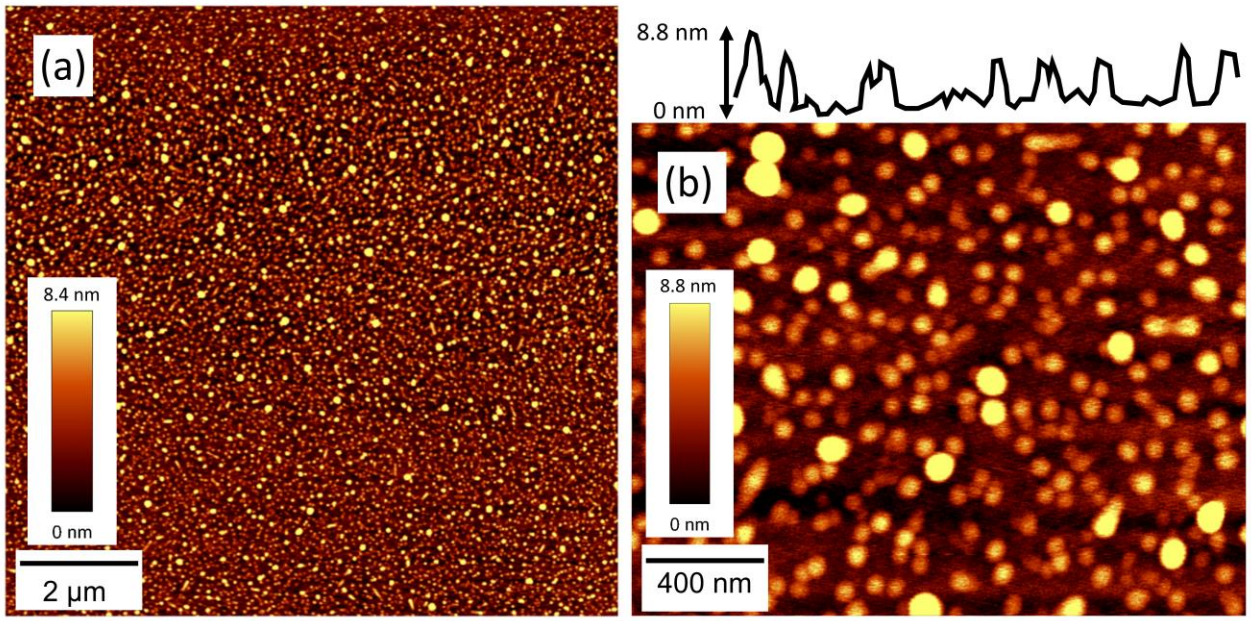


Figure 4.6: (a) Atomic Force Microscopy of the $ZrO_2/Si/SiO_2$ deposited by spin-coating at 3 krpm. **(b)** region that shows similar topography and detail of the grains on the surface. The inset shows the cross-section profile.

2.5 UV-Vis Transmittance

The UV-Vis transmittance was carried out in a UV-Vis spectrophotometer Varian Inc, model DMS 80. The transmittance was performed on the sample with four layers of zirconia film spin-coated on quartz substrate in order to investigate its transparency on the UV-Vis spectra and its optical bandgap. The results of transmittance *vs* wavelength and Tauc plot [22] are shown on figure 4.7. The zirconia film presents high transparency in the visible region spectra and a direct bandgap E_G = 5.8 eV in good agreement with published values [9,23].

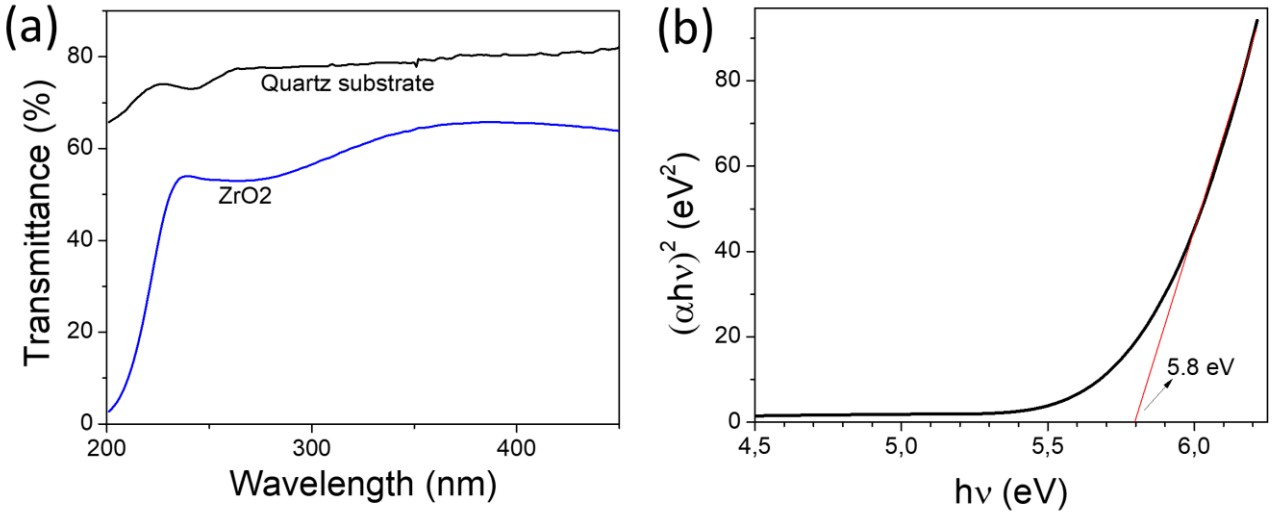


Figure 4.7: (a) Transmittance of the ZrO_2 deposited on quartz substrate, and the **(b)** estimated optical bandgap by Tauc plot.

2.6 Electrical Characterization

After the study on the optical, structural, compositional, and morphological characteristics of the ZrO_2 obtained by the non-alkoxide method, the electrical characterization of ZrO_2 based devices were performed to check whether the presence of impurities within the zirconia films may affect the overall electric characteristics of the dielectric layer. To reduce such possible influences, the zirconia films were deposited with reduced number of layers and thermal annealing after each deposited layer.

Aiming the application of the zirconia films into capacitors, initial investigations occurred with thin film obtained from the solution at concentration 0.4 M. However, the first devices analyzed on MIS ($ITO/ZrO_2/SnO_2$) and MIM ($Al/ZrO_2/Al$) architectures exhibited no electrical insulation, and after several fail attempts, the solution for resolving this issue was to increase the thickness of the dielectric through either a more concentrated sol-gel suspension or reduce deposition speed. Several tests with slower spin-coating deposition led to inhomogeneous films with no electrical insulation. Thus, the sol-gel solution was concentrated to 1.0 M to obtain a more viscous suspension. The higher concentration was obtained through heating the solution at 100 °C. The films obtained from the new concentrated suspension were applied to MIM and TFT devices with appropriated characteristics that are presented in this section.

Firstly, the zirconia films with two layers and intermediary thermal annealing were evaluated through Energy Dispersive X-Ray Spectroscopy (EDX) to obtain qualitative data to verify the presence/absence of the S and Cl elements in the insulating film. The figure 4.8 shows

the presence of S and Cl in small concentration even with calcination and annealing at 450 °C after deposition of each layer. Other elements such as K, Ca, Na, Mg, Al, and Si are related to the soda-lime glass substrate.

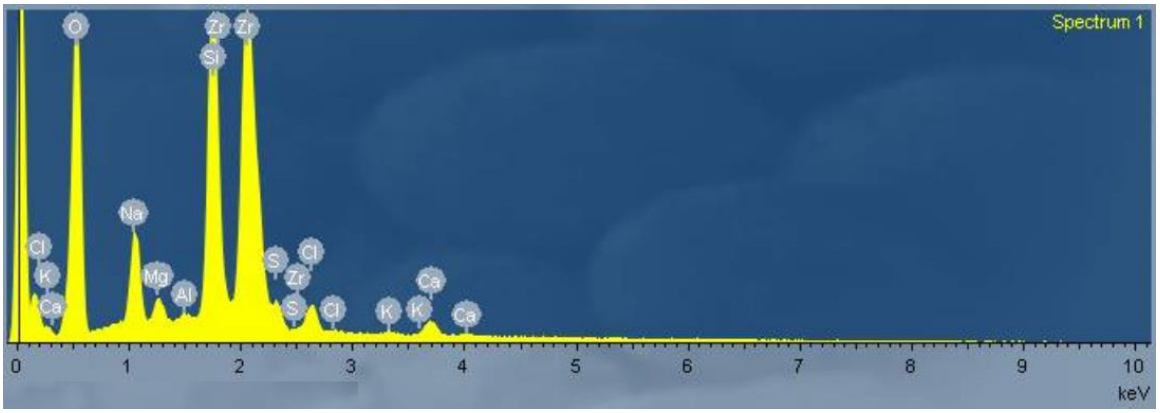


Figure 4.8: EDX obtained on the zirconia film obtained with annealing after each deposited layer.

The topographic characterization of ZrO_2 thin films deposited by dip-coating on glass substrate was performed through confocal microscopy using a Leica DCM 3D microscope. A root mean square roughness of 40 nm and film thickness of about 200 nm was obtained for films deposited through this new solution concentration (Fig. 4.9). This deposition method became the standard deposition for the samples electrically characterized in this section, thus the zirconia thickness presented here is considered in the calculations of the resistivity and dielectric constant of the films.

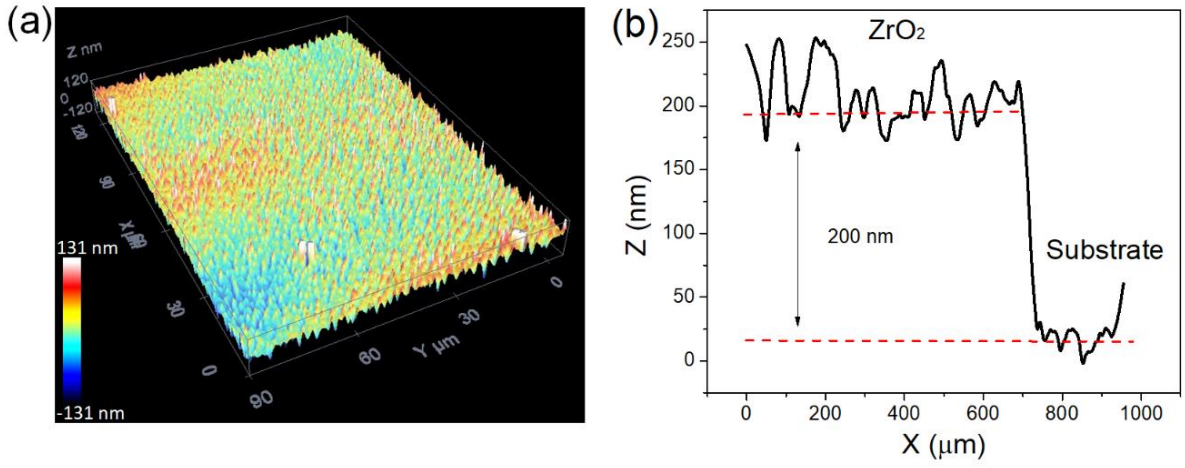


Figure 4.9: (a) Surface topography of a typical ZrO_2 thin film deposited on a glass substrate by dip-coating. **(b)** In a border region, sequential confocal images have been acquired to register the profilometry to obtain the film thickness.

The first devices based on ZrO_2 were assembled on glass substrate with In electrodes and channel length (L) of 300 μm on top of the zirconia layer. The electrical measurement performed with coplanar contacts to obtain the ZrO_2 resistivity occurred at room temperature and pressure. The proposed device was built with two layers of ZrO_2 deposited by dip-coating followed by 10 minutes of calcination and 60 minutes of annealing at 450 °C after the first and second layers, respectively.

Figure 4.10 presents the output of the current as function of the applied voltage where an Ohmic behavior and a resistance R = 7 GΩ were obtained. The film resistivity (ϱ) was calculated by the equation $\rho = R\ A/L$ (presented in chapter 2), where $A = W.t$, W= 3.4 mm, t = 200 nm. The resistivity of 1.6 × 10^4 Ω.m is comparable to values in literature [24] even though the presence of ionized impurities in the film may contribute to higher ionic conductivity within the amorphous material.

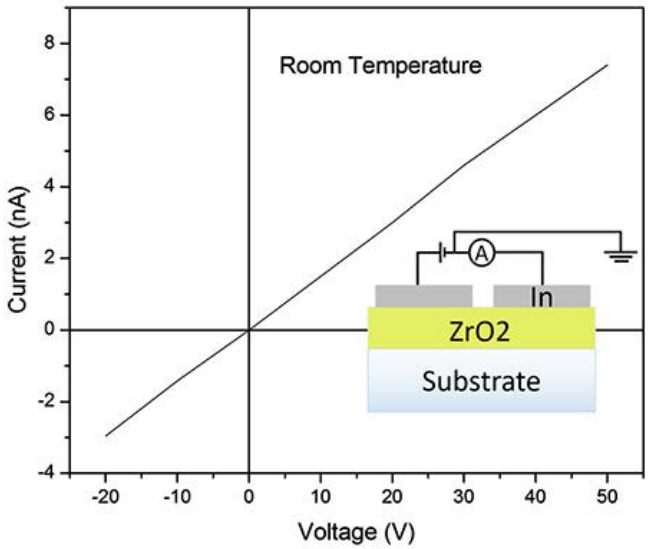


Figure 4.10: Planar electrical characterization of the ZrO_2 film between two electrodes (side by side) with channel length of 300 μm.

The MIM capacitors were assembled as previously described. The electrical measurements of these samples were performed at room temperature through Cyclic Voltammetry (CV) and Impedance Spectrocopy (IS) in a Metrohm AutoLab PGSTAT302 equipped with FRA32M module.

Figure 4.11 presents the results obtained from cyclic voltammetry at several triangular-shape voltage scan rates. It is verified that at faster scan rates the electrical resistance is reduced from R = 5 x 10^8 Ω to R = 1 x 10^7 Ω, at 0.1 and 100 Vs^{-1}, respectively. Moreover, an increase in

capacitive characteristic arises through the hysteresis of the current curve that represents the charge loading in the Al electrodes assisted by the dielectric characteristic of the zirconia film.

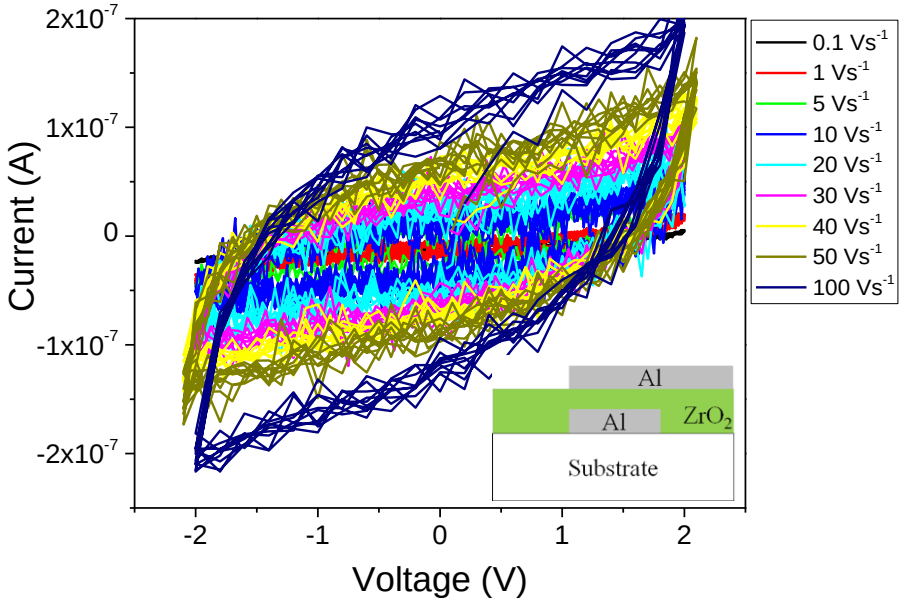


Figure 4.11: Cyclic Voltammetry at voltage scan rate from 100 mVs^{-1} to 100 Vs^{-1} performed on the MIM shown in the inset. A total of 5 cycles was obtained for each curve.

In order to better evaluate the dielectric properties of the zirconia films, electrical impedance of the MIM devices were performed. The impedance results are presented through the black curve in Fig. 4.12a. The maximum impedance Z = 2 x 10^8 Ω obtained at 0.1 Hz is drastically reduced to Z = 5 x 10^2 Ω at 1 MHz. The resistivity (ρ) was calculated considering the electrical resistance at DC voltage (R = 5 x 10^8 Ω) through the equation $\rho = R\,A/L$, where L is the distance between contacts that corresponds to the film thickness L = 200 nm, and A = 0.04 cm^2 is the cross-section area between contacts. The high resistivity ρ = 9.9 x 10^9 Ω.m was found and is within reported values [24].

The presence of capacitive characteristic in the zirconia thin film present in cyclic voltammetry (figure 4.11) was further investigated through the electrical impedance and leads to results presented in Fig. 4.12a. The current-voltage phase difference (blue curve) shows phase values higher than -60° from 1 Hz through 10^5 Hz, with a maximum at -80°. These results represent a behavior close to a perfect capacitor that present -90° phase. The Nyquist plot present in figure 4.12b was performed with a R_P = 9.9 x 10^5 Ω commercial resistor in a parallel configuration with the zirconia based MIM device working as a capacitor in the circuit, more details in the inset of the figure. The result shows the capacitor presents a relatively high specific

capacitance of about 1.7 x 10^{-8} F/cm^2. An average value of capacitance (C_M) was taken from different samples that resulted in C_M = 3.7 x 10^{-8} F/cm^2. The dielectric constant (k) of the zirconia within the capacitor was then obtained k = 8.5. The relative low dielectric constant compared to values reported for zirconia (k = 18 to 23) [7,10] may be related to the presence of impurities in the dielectric layer that may weaken the dipole formation. Although this result is not the state-of-the-art, it is still greater than SiO_2 dielectric constant (k = 3.9) [4,10] which is a positive characteristic and indicates a potential application of this ZrO_2 deposited by sol-gel for replacement of the silicon oxide.

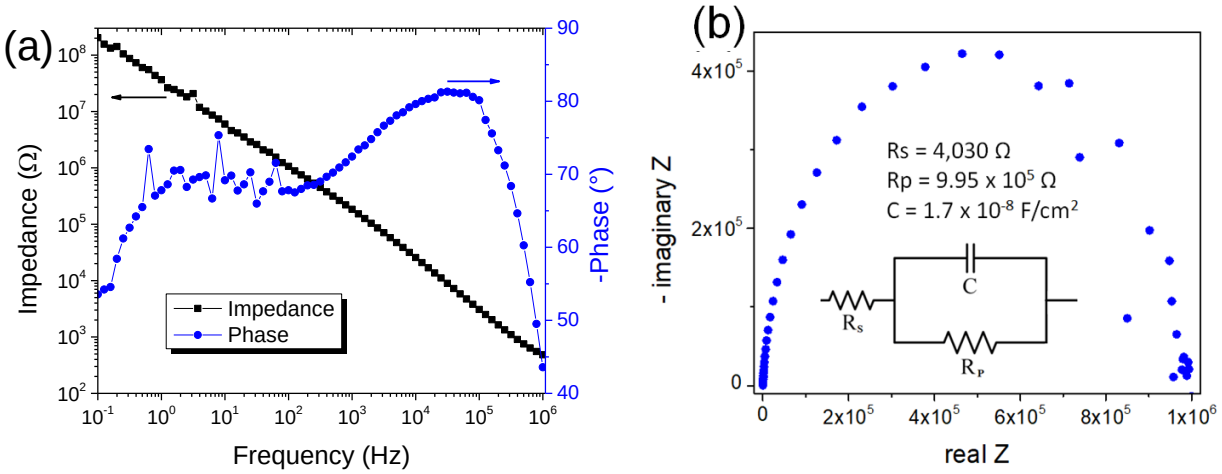


Figure 4.12: (a) Bode plot with Impedance (Z) and Phase as function of frequency**. (b)** Nyquist plot of the ZrO_2 based MIM device in parallel with a R_P = 9.9 x 10^5 Ω commercial resistor.

ZrO_2 thin films were also obtained at low temperature (T = 100 °C) on ITO coated polyethylene naphthalate (PEN) polymeric substrates (ZrO_2/ITO/PEN), as shown in inset of figure 4.13a. The same deposition method was applied in these samples, although the calcination and final thermal annealing were performed at 100 °C for 20 and 60 minutes, respectively. Electrical characteristics of these MIM devices were also evaluated to verify the thermal annealing and ITO electrode effects in such devices. As seen in TG/DSC and RBS results on figures 4.4 and 4.5, samples with lower thermal annealing temperature tends to present higher concentration of S and Cl elements that may impact considerably the dielectric performance and capacitance of these devices.

Bode and capacitance plots are presented in Fig. 4.13a and b. Even though the annealing temperature is much smaller, the samples still present impedance as high as Z = 2 x 10^8 Ω at low frequencies which is similar to values found for samples with higher annealing temperature between Al electrodes. However, the current-voltage phase difference presents higher variation

in these samples. The values of capacitance obtained fluctuates between C = 3 x 10^{-10} F/cm^2 and C = 3 x 10^{-9} F/cm^2, at frequencies of 10^6 and 10^1 Hz, respectively.

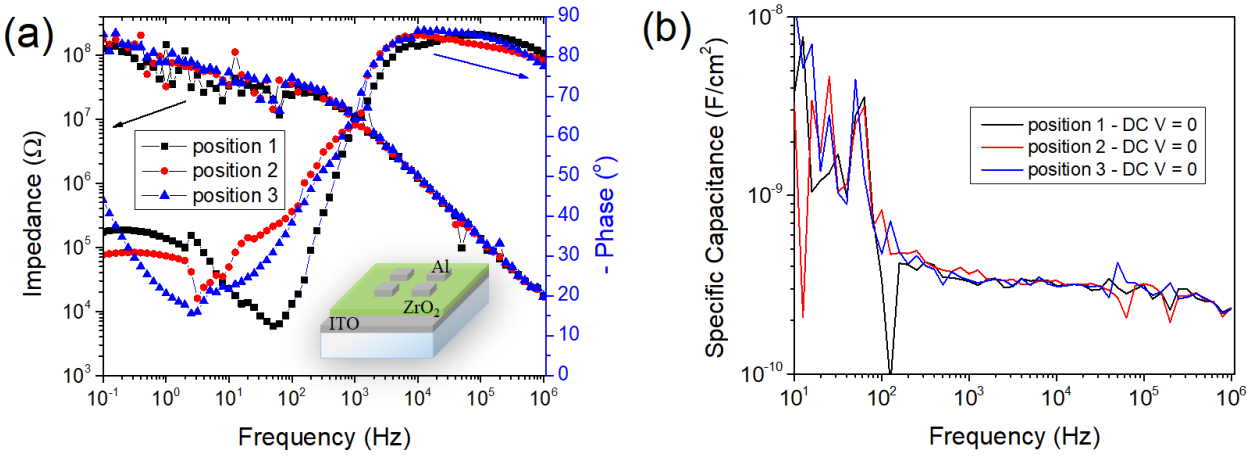


Figure 4.13: (a) Bode plot of Impedance vs frequency (left axis) and phase vs frequency (right axis). Inset: ZrO_2 based MIM devices on flexible substrate with square Al electrodes (A = 0.04 cm^2). **(b)** Specific capacitance as function of frequency at different top electrodes on the sample.

The ZrO_2/ITO/PEN devices present more resistive characteristic than devices deposited on glass substrate, which is observed through the phases closer to 0° at low frequencies (< 10^3 Hz). That difference may be related to higher concentration of ionic components and its consequently higher disorder within the zirconia layer annealed at 100 °C. This condition also may be the responsible for the lower maximum capacitance (3 x 10^{-9} F/cm^2) found for these devices. The resistive characteristic preserves the high impedance at higher frequencies, i.e. the impedance of samples annealed at 450 °C decreases to Z = 10^6 Ω at 10^2 Hz while the impedance of polymeric samples decreases to Z = 3 x 10^7 Ω, at the same frequency. The higher impedance found in ZrO_2/ITO/PEN may be related to the higher work function (4.7 eV) of the ITO electrode [25] that increases the conduction band discontinuity [26] decreasing the carrier injection and the leakage current.

ZrO_2 based transistors - ZrO_2/SnO_2

Zirconia based MIS devices were preliminarily investigated but presented high leakage current and low channel current modulation which motivated a change on investigation direction concerning ZrO_2/SnO_2 n-type TFTs. Results of electrical characterization of these devices are presented in figure 4.14a. Many devices were built and presented the same results described as

follows. The figure shows the output drain and gate currents of the TFT as function of the applied drain voltage. Unfortunately, the dielectric layer does not control the channel due to high leakage current (I_G) that is responsible for the decrease of drain current (I_D) at higher applied V_G. A possible explanation for this high leakage is the large area (of about 0.4 cm^2) of the bottom gate electrode below the dielectric and semiconductor. The large area is represented by the red box in figure 4.14b. This figure also shows a schematic diagram of the possible leakage current where the processes I, II, and III represent the charges flowing in different regions. Process I represents the drain current from the source to drain electrode. The process II symbolizes the charges following different path, oriented by the gate electric field. Finally, the process III represents the leakage current where the charges are still oriented by the large electric field generated by the gate and penetrates into a defect/pore on the dielectric layer and achieves the gate terminal.

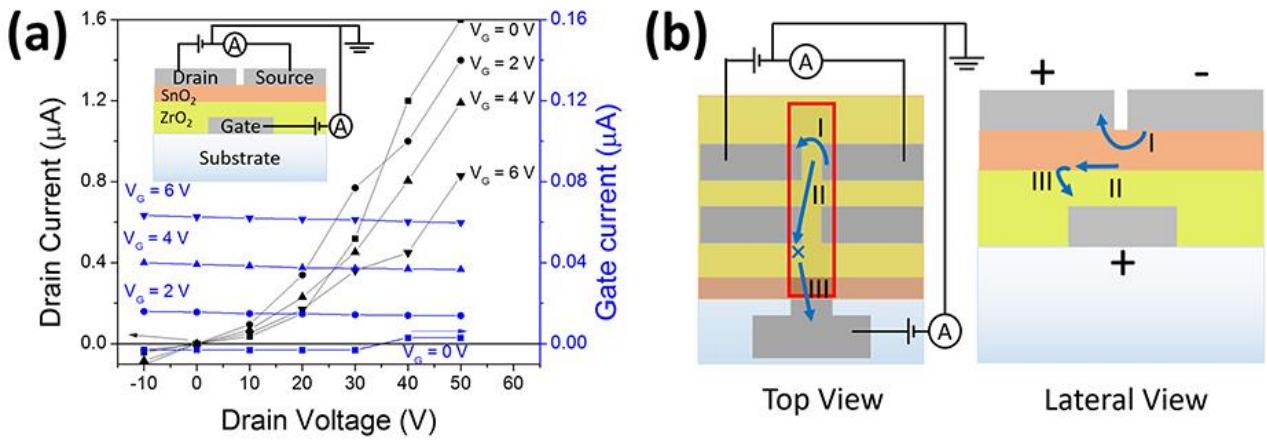


Figure 4.14: (a) Output of Drain and Gate currents of the ZrO_2/Sb:SnO_2 n-type TFT. **(b)** Schematic diagram of the possible leakage mechanism that increases linearly with the gate bias. **I** shows the charges flowing in the channel, **II** shows the charges flowing in the semiconductor layer oriented by the gate electric field, and **III** shows the gate current (I_G) after the charges penetrate a defect on the insulator layer and reach the gate electrode.

The leakage may occur in nano-areas where the dielectric presents pores caused by three different conditions: a non-homogeneous deposition of the zirconia; semiconductor SnO_2 deposited by sol-gel route followed by thermal annealing that possibly causes damages to the dielectric layer on the bottom; and the very low pH (1.5) that in some cases corrodes the bottom gate electrodes. Another possibility is not related to presence of pores but to the small conduction band discontinuity between the SnO_2 and ZrO_2 due to the relatively large bandgap of the semiconductor. In this case, a large contribution of leakage current may occur by gate oxide tunneling (I_{gate}) and injection of hot carriers (I_{HC}).

An alternative to overcome this problem is to reduce the gate dimensions that would reduce the possibility of pores occurrence that causes the high leakage currents. Simultaneously, small bandgap semiconductors obtained by evaporation could be used to avoid eventual damage on the bottom dielectric layer.

CONCLUSION

In this chapter, the investigation of ZrO_2 thin films obtained by non-alkoxide sol-gel method at different annealing temperatures was reported. High transparency and homogeneity, non-porous surface and high bandgap were found in these films. The compositional analysis showed residues of S and Cl elements from the precursor solution that may contribute for the reduced dielectric constant found for the zirconia thin films.

Zirconia based MIM capacitors with thermal annealing at 450 °C and 100 °C showed high and interesting insulating and capacitive characteristics. Although a low dielectric constant was obtained due to impurities, it is still larger than the dielectric constant of SiO_2 which constitute an indicative of possible application of the sol-gel deposited ZrO_2 in electronic devices.

Even though the results obtained through the TFT samples are not ideal, this study is important to verify and understand the application of the dielectric in a stacked architecture where the influence of many parameters may affect the performance of the device.

REFERENCES

[1] D.F. Maia, D.A. Costa, A.C.F.M. Costa, L. Gama, H.L. Lira, Morphological aspects of zirconia from Pechini method, (2000).

[2] A. Kuwabara, T. Tohei, T. Yamamoto, I. Tanaka, Ab initio lattice dynamics and phase transformations of ZrO2, Phys. Rev. B. 71 (2005) 64301.

[3] O.Y. Kurapova, V.G. Konakov, Phase evolution in zirconia based systems, Rev. Adv. Mater. Sci. 36 (2014) 177–190.

[4] M.H. Boratto, L.V.A. Scalvi, Deposition of Al2O3 by resistive evaporation and thermal oxidation of Al to be applied as a transparent FET insulating layer, Ceram. Int. 40 (2014) 3785–3791. doi:10.1016/j.ceramint.2013.09.041.

[5] M.H. Boratto, L.V.A. Scalvi, J.L.B. Maciel Jr, M.J. Saeki, E.A. Floriano, Heterojunction between Al2O3 and SnO2 thin films for application in transparent FET, Mater. Res. 17 (2014) 1420–1426. doi:10.1590/1516-1439.285114.

[6] N. Padmamalini, K. Ambujam, Structural, dielectric and impedance studies on high-k

ZrO2-TiO2 nanocomposite, J. Mater. Sci. Mater. Electron. 28 (2017) 4690–4694. doi:10.1007/s10854-016-6109-6.

[7] M.T. Soo, N. Prastomo, A. Matsuda, G. Kawamura, H. Muto, A.F.M. Noor, Z. Lockman, K.Y. Cheong, Elaboration and characterization of sol-gel derived ZrO 2 thin films treated with hot water, Appl. Surf. Sci. 258 (2012) 5250–5258. doi:10.1016/j.apsusc.2012.02.008.

[8] G. Ye, H. Wang, S. Arulkumaran, G.I. Ng, R. Hofstetter, Y. Li, M.J. Anand, K.S. Ang, Y.K.T. Maung, S.C. Foo, Atomic layer deposition of ZrO2 as gate dielectrics for AlGaN/GaN metal-insulator-semiconductor high electron mobility transistors on silicon, Appl. Phys. Lett. 103 (2013) 2011–2014. doi:10.1063/1.4824445.

[9] D. Xiao, G. He, Z. Sun, J. Lv, P. Jin, C. Zheng, M. Liu, Microstructure, optical and electrical properties of solution-derived peroxo-zirconium oxide gate dielectrics for CMOS application, Ceram. Int. 42 (2015) 759–766. doi:10.1016/j.ceramint.2015.08.177.

[10] Y. Dora, S. Han, D. Klenov, P.J. Hansen, K. No, U.K. Mishra, S. Stemmer, J.S. Speck, ZrO2 gate dielectrics produced by ultraviolet ozone oxidation for GaN and AlGaN/GaN transistors, J. Vac. Sci. Technol. B Microelectron. Nanom. Struct. 24 (2006) 575. doi:10.1116/1.2167991.

[11] A. Javey, H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. McIntyre, P. McEuen, M. Lundstrom, H. Dai, High-kappa dielectrics for advanced carbon-nanotube transistors and logic gates., Nat. Mater. 1 (2002) 241–246. doi:10.1038/nmat769.

[12] D. Panda, T.-Y. Tseng, Growth, dielectric properties, and memory device applications of ZrO2 thin films, Thin Solid Films. 531 (2013) 1–20. doi:10.1016/j.tsf.2013.01.004.

[13] Y. Mi, J. Wang, Z. Yang, Z. Wang, H. Wang, S. Yang, A simple one-step solution deposition process for constructing high-performance amorphous zirconium oxide thin film, RSC Adv. 4 (2014) 6060–6067. doi:10.1039/c3ra46169f.

[14] H. Fukumoto, M. Morita, Y. Osaka, Electrical characteristics of metal-insulator-semiconductor diodes with ZrO2/SiO2 dielectric films, J. Appl. Phys. 65 (1989) 5210–5212. doi:10.1063/1.343155.

[15] C. Avis, J. Jang, High-performance solution processed oxide TFT with aluminum oxide gate dielectric fabricated by a sol–gel method, J. Mater. Chem. 21 (2011) 10649. doi:10.1039/c1jm12227d.

[16] K.K. Banger, Y. Yamashita, K. Mori, R.L. Peterson, T. Leedham, J. Rickard, H. Sirringhaus, Low-temperature, high-performance solution-processed metal oxide thin-film transistors formed by a "sol–gel on chip" process., Nat. Mater. 10 (2011) 45–50. doi:10.1038/nmat2914.

[17] J. Livage, F. Beteille, C. Roux, M. Chatry, P. Davidson, Sol - Gel Synthesis of Oxide Materials, Acta Mater. 46 (1998) 743–750.

[18] J.J. Yu, I.W. Boyd, ZrO2 films deposited by photo-CVD at low temperatures, Appl. Phys. A Mater. Sci. Process. 75 (2002) 489–491. doi:10.1007/s003390201294.

[19] L.A. Chiavacci, S.H. Pulcinelli, C. V. Santilli, V. Briois, Structural and phenomenological characterization of the thermoreversible sol-gel transition of a zirconyl aqueous precursor modified by sulfuric acid, Chem. Mater. 10 (1998) 986–993. doi:10.1021/cm970387d.

[20] A.P. Rizzato, C. V Santilli, S.H. Pulcinelli, X-ray reflectivity of zirconia based sol-gel coatings on borosilicate glasses, J. Non. Cryst. Solids. 247 (1999) 158–163.

[21] M. Mayer, Rutherford Backscattering Spectrometry (RBS), Work. Nucl. Data Sci. Technol. Mater. Anal. (2003) 19–30. doi:10.1016/1359-6454(95)00193-X.

[22] J. Tauc, R. Grigorovici, A. Vancu, Optical properties and electronic structure of amorphous germanium, Phy. stat. sol. 15, 627 (1966).

[23] G. Adamopoulos, S. Thomas, P.H. Wöbkenberg, D.D.C. Bradley, M.A. McLachlan, T.D. Anthopoulos, High-mobility low-voltage ZnO and Li-doped ZnO transistors based on ZrO2 high-k dielectric grown by spray pyrolysis in ambient air, Adv. Mater. 23 (2011) 1894–1898. doi:10.1002/adma.201003935.

[24] S.K. Tadokoro, E.N.S. Muccillo, Zircônia tetragonal policristalina. Parte II: Microestrutura e resistividade elétrica, Cerâmica. 47 (2001).

[25] C. Sun, X. Li, G. Wang, P. Li, W. Zhang, T. Jiu, N. Jiang, J. Fang, Highly efficient inverted polymer solar cells using fullerene derivative modified TiO2 nanorods as the buffer layer, RSC Adv. 4 (2014) 19529. doi:10.1039/c4ra02254h.

[26] K.C. Chiang, C.H. Cheng, K.Y. Jhou, H.C. Pan, C.N. Hsiao, C.P. Chou, S.P. McAlister, A. Chin, H.L. Hwang, Use of a high-work-function Ni electrode to improve the stress reliability of analog SrTiO3 metal-insulator-metal capacitors, IEEE Electron Device Lett. 28 (2007) 694–696. doi:10.1109/LED.2007.900876.

Chapter 5

ZrO_2 based devices: The Pechini method

INTRODUCTION

This chapter presents a study of a second method, Pechini, to obtain homogeneous, non-porous and stable thin films of ZrO_2. Even though this route is well known for obtaining porous films [1] and powders [2,3], an investigation of the influences of the deposition rate and thermal annealing temperatures is done to define the best conditions for deposition of high quality zirconia thin films. The films were deposited on substrates of soda-lime glass or quartz for specific characterizations and applied to capacitors and TFTs in order to investigate their electrical properties. The morphological, optical and electrical properties of the zirconia thin films are investigated in order to apply this insulating layer in future electronic applications, such as in memristors [4,5] and in transistor devices [4].

The section 1 of this chapter presents the methodology to produce the polymeric solution, films and devices. The section 2 presents the characterizations, results and discussions related to the films and devices.

1 METHODOLOGY

The polymeric method that produces crystalline, pure, and stable zirconia powder is used for production of functional ZrO_2 films, and the results are reported in this chapter. Among the several techniques for deposition of ZrO_2 thin film the polymeric precursor method is a cost-effective route with potential to obtain a smooth and non-porous insulating layer. This method consists on the formation of a polymeric resin from polymerization and esterification reaction between a chelate metal cation and poly-hydroxyl alcohol [3,6].

The main purpose of this section is to describe the obtainment of zirconia thin film directly on substrates, to further understand the characteristics that may affect the application of this layer in TFT devices. Even though the use of the Pechini method for fabrication of thin film

is commonly used for ZnO [7] and platinum (Pt) [8], the obtainment of ZrO_2 films by polymeric route is not reported in literature, as far as we know.

1.1 Preparation of colloidal suspension

The obtaining of ZrO_2 polymeric resin was performed in order to produce thin films with a more neutral solution (pH~3.5), less acid than the previous sol-gel solution (pH = 1.5), obtained by the non-alkoxide method, investigated in chapter 4 . This increase of the pH reduces significantly the corrosion caused on the bottom electrode during this oxide deposition.

Zirconium (IV) butoxide ($Zr(OC_4H_9)_4$) (80 wt% in 1-butanol, purity > 99.99 %), citric acid ($C_6H_8O_7$) (purity 99.5 %), and ethylene glycol ($C_2H_6O_2$) (purity 99.5 %) were used to obtain the resin. Firstly, citric acid was dissolved in distilled water and heated at 70 °C under magnet stirring followed by the addition of zirconium butoxide, in a ratio of metal/acid of 1/2.5, to favor the complexation of the metal with the citric acid, forming the zirconium citrate (chelate). The solution presented clear and slight yellow color after the complete dissolution of the zirconium citrate under stirring. The glycol ethylene was then added in a mass ratio of citric acid/glycol ethylene of 60/40, resulting in the esterification reaction that polymerizes forming an organic matrix through the solution [6]. The final solution for deposition of thin films was dissolved in water (volume 50/50) to obtain a lower concentration and less viscous solution.

1.2 Preparation of films and devices

Previously to any film deposition, the substrates were cleaned in sonicated bath in 2 steps as follow: 15 min in water/detergent followed by washing under distilled water before another 15 min in isopropyl alcohol. Subsequently they were dried with serigraphic blower. For preparation of metal-insulator-metal capacitors (MIM) and thin film transistors (TFT) aluminum contacts were evaporated on the substrate to form the gate (bottom) electrode. The deposition of ZrO_2 thin film on the substrate/electrode occurred by dip-coating the substrate with rate of 100 mm/min for 3 times, which was repeated twice, producing 2 layers of ZrO_2 on top of the Al electrodes. Thermal annealing occurred at 150 °C for 1 hour after each layer. The MIM was finished with the evaporation of the Al top electrode (figure 5.1a).

Figure 5.1b presents the assembly of the TFT device that occurred by depositing the fullerene (C_{60}) as active semiconductor on top of the dielectric by evaporation. The thickness of

approximately 45 nm was achieved by a film growth rate of 0.05 nm/s. Evaporation of Al (source and drain) electrodes was done, completing the TFT device.

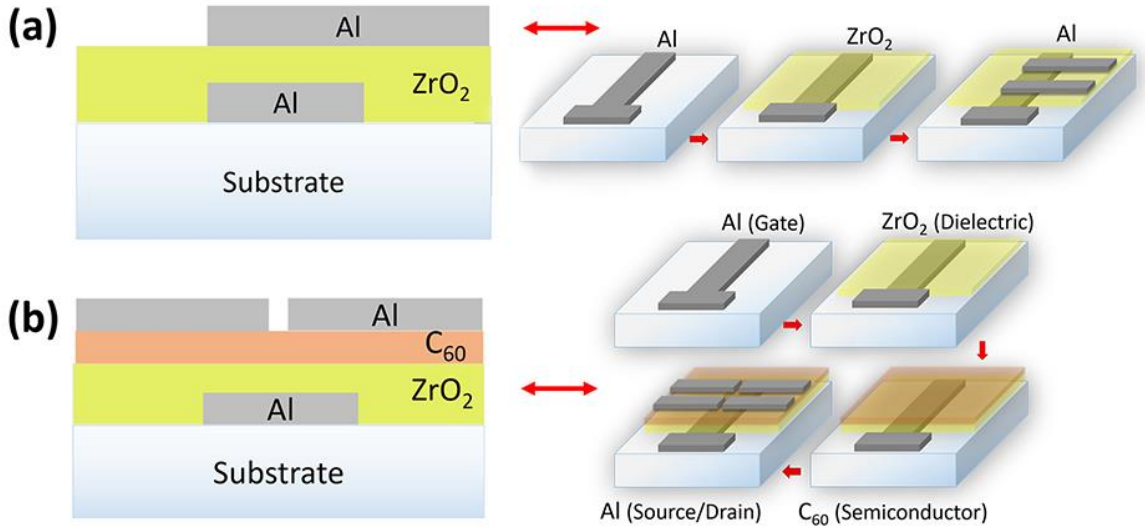


Figure 5.1: (a) Diagram of the MIM capacitors (Al/ZrO_2/Al). **(b)** Diagram of the TFT (Al_{bottom}/ZrO_2/C_{60}/Al_{top}).

Semiconducting polymeric thin films are usually produced by solution routes and deposited by spin coating at low temperature to avoid high temperature processes [9]. Polymers consist of large molecules with long chains of repeating monomers that decomposes during thermal evaporation [10]. However, small molecules with low molecular weight such as C_{60} [11] can be directly deposited under high vacuum conditions, without decomposition at high temperature. These films can easily lead to uniform films with large areas [9], precise controlled thickness, and designed shapes through shadow masks [12,13]. Therefore, the evaporated C_{60} was chosen to be the semiconductor layer to avoid that other chemical suspensions deteriorate the bottom dielectric layer.

A parallel study on the zirconia layer was also carried out to reduce the thickness, cracks and leakages on the ZrO_2 thin films and is presented at the end of this chapter. The study considered the variation of deposition rate from 2 to 70 mm/min of the dip-coating. Also, in order to eliminate more organic components, the films were calcined at 150 °C for 2 hours followed by another annealing with increased temperature up to 250 °C for 1 hour. Both temperatures were achieved at slow heating ramp of 1 °C/min to avoid any cracking on the films.

2 RESULTS

The characterizations, results and discussion related to ZrO_2 thin film and devices obtained by the polymeric method are presented in this section. The characterizations were obtained by UV-Vis transmittance, X-Ray Diffraction (XRD), Thermal Gravimetric Analysis (TGA) and Differential Scanning Calorimetry (DSC), Energy dispersive X-rays Spectroscopy (EDX), Confocal microscopy, Scanning Electron Microscopy (SEM), and electrical measurements such as IxV curves and Impedance Spectroscopy (IS).

2.1 TGA/DSC

The resin of ZrO_2 was evaluated through thermogravimetric analysis (TG) and differential scanning calorimetry (DSC) with temperature up to 500 °C in order to verify the temperatures that occurs the largest loss of mass as well as the high energy changes in the sample. The formation of chemical bonding of cations in the lattice favors the development of a polymeric resin of high viscosity, which is capable of chelate and keep the cations homogeneously distributed. Even when the bondings are broken during calcinations, the high viscosity prevents the cation motion, thus preventing their segregation [14].

Figure 5.2a presents the TG plot of the weight as function of the temperature for the synthesized precursor resin. The derived loss of mass (DTG) shows the temperatures of higher decomposition of the resin. The results obtained indicate the decomposition of the resin involves three processes of loss of mass. The first shows 10.4% of loss between 50°C and 128°C. The second shows decomposition in the interval from 128 °C to 233 °C with loss of mass of about 20.6%, while the third process presented a loss of 58.1% between 233°C and 500°C. The mass loss can be attributed to elimination of organic ligands and water generated by the sterification reaction, decomposition of polyester chain with elimination of CO_2 and H_2O, decomposition of carboxyl bonded to metals and elimination of organic residues with consequent formation of the stable and pure phase metal-oxygen.

The figure 5.2b presents the endothermic and exothermic processes involved in the decomposition of the ZrO_2 resin. The first endothermal band, between 122 °C and 165 °C, occurs due to physical desorption and evaporation of H_2O molecules and ethylene glycol excess generated by the polysterification reaction. The exothermal band between 243 °C and 285 °C involves the energy liberation due to the beginning of decomposition of organic ligands with consequent liberation of CO_2 and H_2O molecules. In the interval of 285 °C and 330 °C the endothermal band is associated to a process of heat absorption. The intense exothermal band at

388°C e 450°C shows maximum of heat released due to final decomposition of the organic ligands that takes to the chemical reactions responsible for formation of crystalline zirconia phases [15,16].

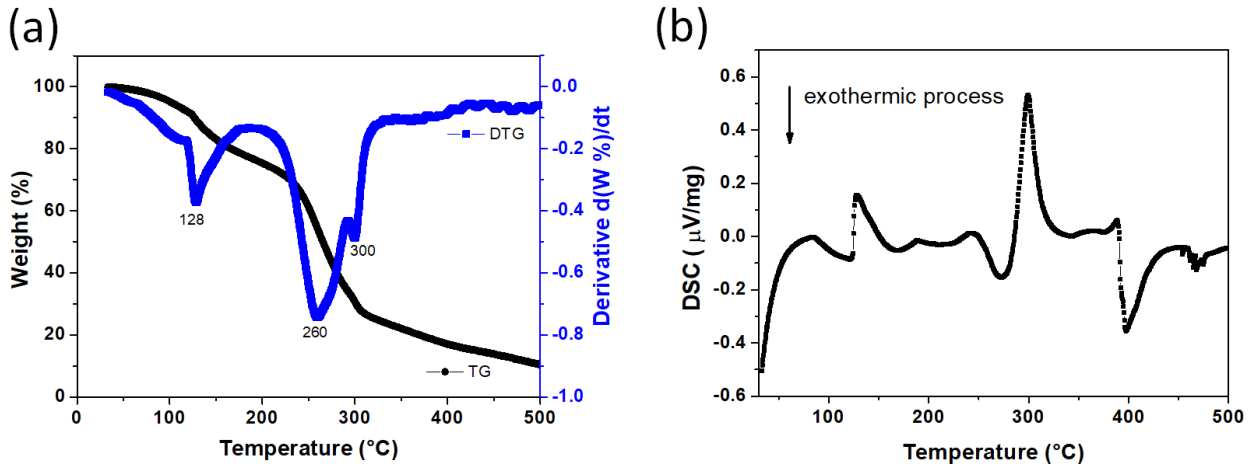


Figure 5.2: (a) TG and DTG curves, and the **(b)** DSC curve of the ZrO_2 resin with thermal annealing from 32 °C to 500 °C.

2.2 Scanning Electron Microscopy

The zirconia films were deposited by the polymeric route on glass substrate by dip-coating 3 times at rate of 100 mm/min with a total of 2 layers and TA at 150 °C for 1hour for each one. The zirconia film polymerizes at this temperature with no crystallinity, even with TA up to 400 °C [2,7].

The ZrO_2/substrate assembly was analyzed by SEM in order to verify the homogeneity of the surface and presence of pores. Figure 5.3 shows the image of the zirconia thin film to verify the surface homogeneity. It can be observed that it presents no exposed pores on the surface.

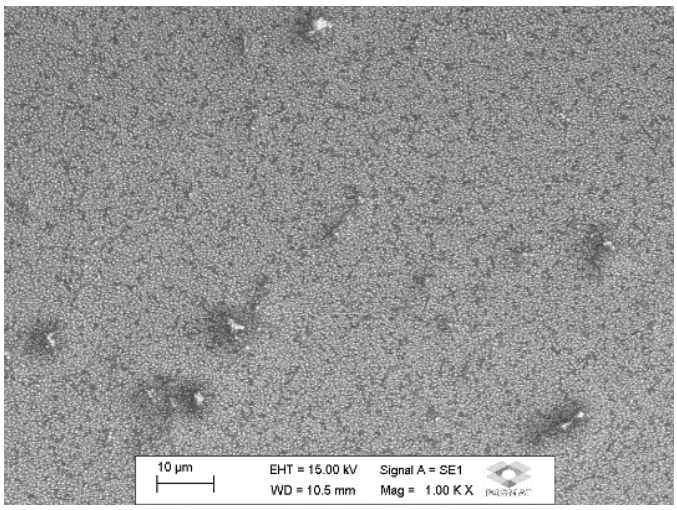


Figure 5.3: (a) SEM of the ZrO_2 film surface deposited on glass substrate.

2.3 UV-Vis Transmittance

ZrO_2 thin film deposited on quartz substrate was submitted to UV-Vis transmittance measurement, to verify the transparency and optical bandgap of the dielectric film. The measurement was performed in a Perkin Elmer Spectrophotometer (model Lambda 1050) at different spots of the sample. The result is presented in figure 5.4. It shows that the zirconia layer is quite transparent and achieves a maximum transparency of about 95% in the wavelength from 260 to 1800 nm. Figure 5.4b shows the direct bandgap obtained through the Tauc plot, with energy E_G = 5.45±0.03 eV, in good agreement with the energy found for the zirconia obtained by non-alkoxide method (E_G = 5.8 eV) presented in chapter 4, and with values reported in literature [17,18].

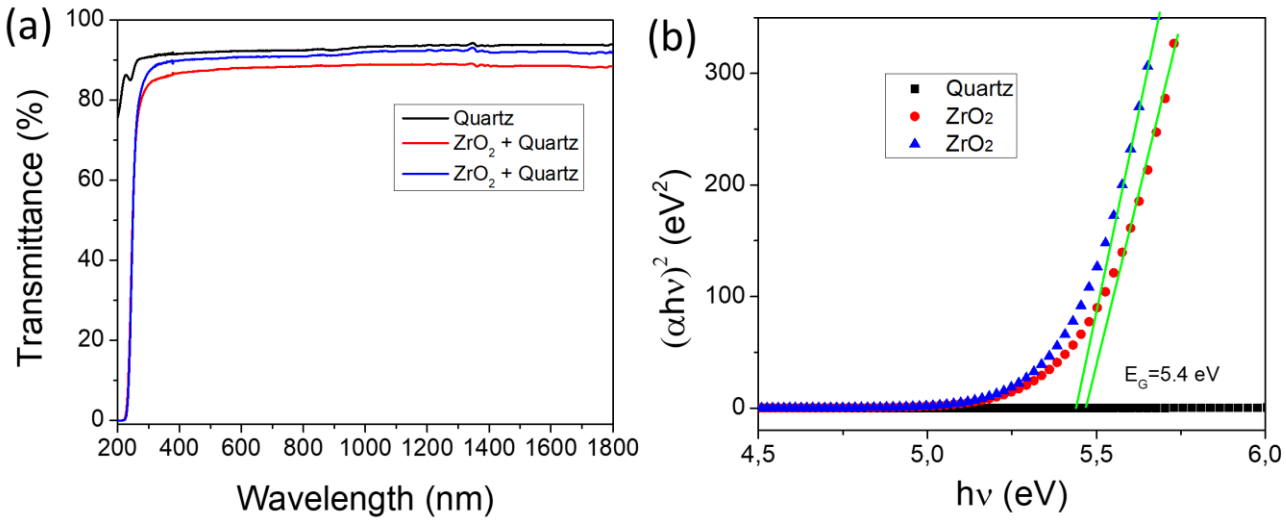


Figure 5.4: (a) Transmittance of zirconia film on quartz substrate in the ultraviolet-visible-near infra-red spectra. **(b)** The bandgap of the zirconia is obtained by the Tauc plot.

MIM capacitors

MIM capacitors were assembled with aluminum electrodes and 2 layers of zirconia deposited by dip-coating at 100 mm/min followed by thermal annealing at 150 °C. The devices were investigated through cyclic voltammetry and Electrical Impedance Spectroscopy (EIS) to understand the dielectric properties of the zirconia layer and their relations for application in TFTs.

2.4 Cyclic Voltammetry

Cyclic voltammetry was carried out on Al/ZrO_2/Al samples at voltage range from -2 V to +2 V and scan rate varying from 0.1 to 1000 V/s, and the results are shown in figure 5.5a. It is possible to notice the capacitive characteristic of the sample through the accumulation of charges that produces a considerable current at zero voltage applied. The current at V = 0 as well as the maximum current (I_{max}) at ±2 V is proportional to the scan rate. The higher current at faster voltage scan rates represents a reduction of electrical resistance in the MIM at higher scan rates.

The hysteresis index (HI) [19] is a parameter that correlates and quantify the resistive/capacitive characteristics of a device with the hysteresis presented in the electrical measurement. The HI was obtained through the equation 5.1:

$$HI = \Delta I/(I_{max} - I_{min}) \tag{5.1}$$

where ΔI is the difference between positive (I_+) and negative currents (I-) at V = 0, and I_{max} and I_{min} are taken at +2 V and -2 V, respectively. HI = 1.0 represents perfect capacitor curves, while HI = 0.0 represents perfect resistors. The results obtained show maximum hysteresis index HI = 0.63 and HI = 0.65 at scan rates (or frequencies) of 10 to 20 V/s (1.25 to 2.5 Hz), which represent a more capacitive characteristic on the samples [20].

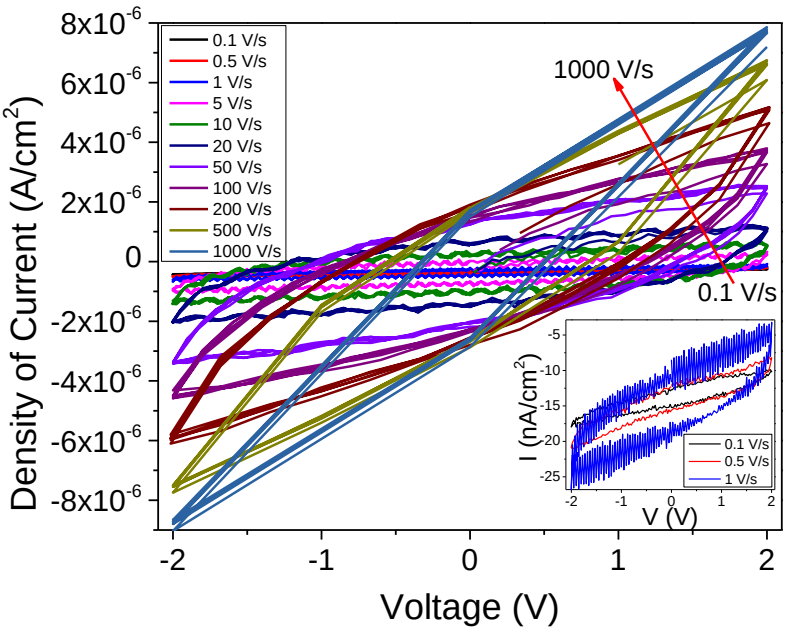


Figure 5.5: (a) Cyclic Voltammetry of the MIM capacitors with voltage scan rate from 0.1 to 1000 V/s. Inset shows the curves for slow scan rates (0.1 to 1V/s).

2.5 Electrical Impedance Spectroscopy (EIS)

The Impedance spectroscopy was carried out on Metrohm AutoLab PGSTAT302 with FRA32M Module operating with AC potential variation of 10 mV. The EIS was carried out on the same MIM devices analyzed through cyclic voltammetry to verify their electrical Impedance and Capacitance as function of the AC frequency. Figure 5.6a shows the Bode plot of current phase *vs* frequency at different DC voltages applied. The result shows a voltage-current phase of -85 ° at zero DC voltage applied at frequencies lower than 10^3 Hz, that means the device is mainly capacitive at this frequency range. The application of DC voltage (from 2 to 4 V) implies on the reduction of phase angle (close to 0 °) turning the device into more resistive characteristic at lower frequencies. It is possible to notice that the -45° phase angle occurs at frequencies (f) from 3 to 4 kHz and the RC constant of time (τ) calculated through the equation $\tau = 1/f$ results in τ = 0.3 ms. Such small constant of time has comparable value with LSG-EC (33 ms) and commercial aluminum electrolytic capacitors (1 ms) [20].

Figure 5.6b shows the Impedance *vs* frequency plot as function of the DC voltage applied. The results present the reduction of the impedance at higher frequencies. At DC V = 0 and 0.1 Hz the impedance presents the highest value Z = 30 MΩ. For higher applied voltages the impedance presents a proportional reduction. The minimum impedance at 0.1 Hz found was Z = 4.7 MΩ at V = 4 V which is only one order lower than the highest values. The reduced impedance at higher DC applied voltage is expected due to some leakage current that reduces the electric resistance of the dielectric film [21].

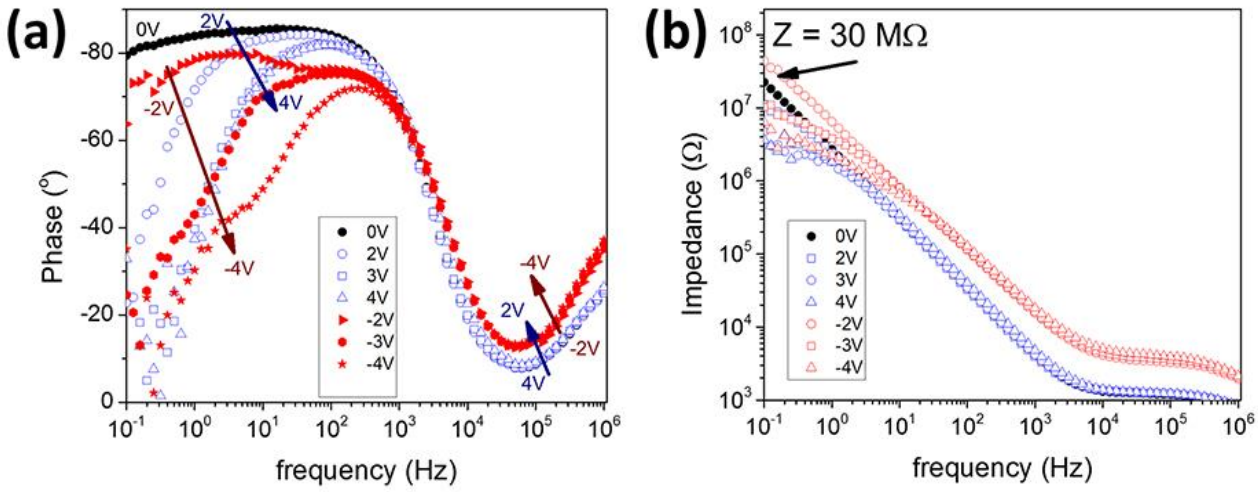


Figure 5.6: Bode plot of the **(a)** Current phase angle *vs* frequency, and **(b)** Impedance *vs* frequency.

The capacitance as function of frequency of the same MIM device prepared from polymeric method is plotted in figure 5.7. The figure shows the capacitance as highly dependent on the operation frequency of the capacitor, presenting the lowest value of 9 x 10^{-10} F/cm^2 at 1 MHz and the highest value at 1 Hz of 1.1 x 10^{-7} F/cm^2.

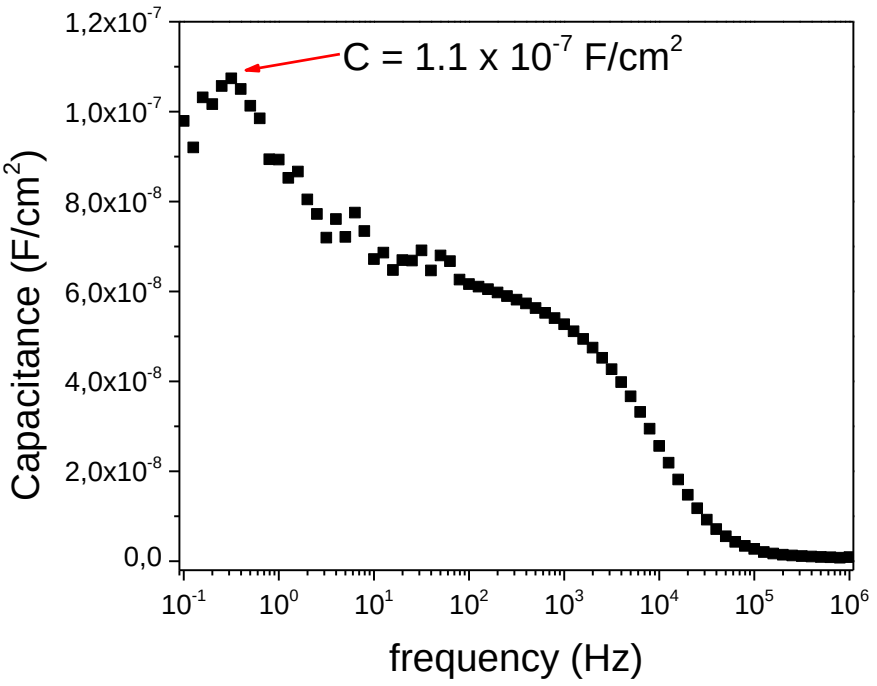


Figure 5.7: Plot of the Capacitance as function of the frequency of operation of the capacitor.

The dielectric constant (k) of the zirconium oxide was obtained through the equation 5.2 [22]:

$$C = \frac{k\,\varepsilon_0\,A}{t} \tag{5.2}$$

where the thickness obtained by confocal microscopy is t = 1200 ± 42 nm, the vacuum permittivity ε_0 = 8.85 x 10^{-12} F/m, and C is taken from the figure 5.7 at different frequencies. The dielectric constant as function of the frequency is shown in table 5.1:

Table 5.1: Values of capacitance as function of frequency, obtained from the figure 5.7, to calculate the dielectric constant, *k* (right column), of the zirconia thin film.

Frequency (Hz)	Capacitance (F/cm^2)	Dielectric constant *k*
1	1.1×10^{-7}	149.2
10^3	5×10^{-8}	109.4
10^6	9×10^{-10}	1.2

The dielectric constant is intrinsically related to the capacitance, and therefore, it is also highly dependent of the operation frequency. The presence of dielectric loss, that is the delay of molecular polarization with respect to the alternating electric field inside the capacitor, at higher frequencies occur in the analyzed samples, which produces films with low *k* at 10^6 Hz, much smaller than the values reported in literature (*k* = 16 to 24) in the same frequency range [23–25]. This loss occurs due to the presence of impurity ions, from the precursor resin, that contributes to increase the dipole and ionic relaxations in the dielectric film.

ZrO_2 based transistors – ZrO_2/C_{60}

2.6 Microscopy: Confocal and Scanning Electron

Thin film transistors (TFT) were assembled as previously shown in figure 5.1b with ZrO_2 and C_{60} working as dielectric and semiconductor layers, respectively, in the $Al/ZrO_2/C_{60}/Al$ configuration. The surface of the fullerene deposited on ZrO_2 was investigated by microscopy to verify the surface homogeneity and porosity. The figures 5.8a (b and c) show different regions of the same sample. These images are from the evaporated fullerene (upper part) on top of the ZrO_2 (bottom part). In the first image the C_{60} is homogeneous and presents no clear porosity, but at the second image the same sample shows some parts with cracks on the surface. The third image, obtained by SEM, shows only the fullerene surface with presence of the same fissures observed in previous image. These fissures on the organic semiconductor layer occur due to the bottom zirconia film that cracks during thermal annealing. A better discussion about such fissures is presented in the next section.

The compositional analysis of the C_{60}/ZrO_2 was done by Energy Dispersive X-Ray Spectroscopy (EDX) and the result is shown in figure 5.8d. A qualitative analysis of the atomic

composition of fullerene and zirconia films presents 2.3 at% Zr, 38.1 at% O, and 59.6 at% C. The results do not show presence of other elements, from non-intentional impurities or glass substrate, probably due to the thick zirconia film. The high concentration of oxygen is due to the inner layer of zirconium oxide along with some possible oxidation of the fullerene surface exposed to air. The carbon concentration is mostly from the C_{60} layer but may have some contribution from the organic solvents within the zirconia annealed at 150 °C.

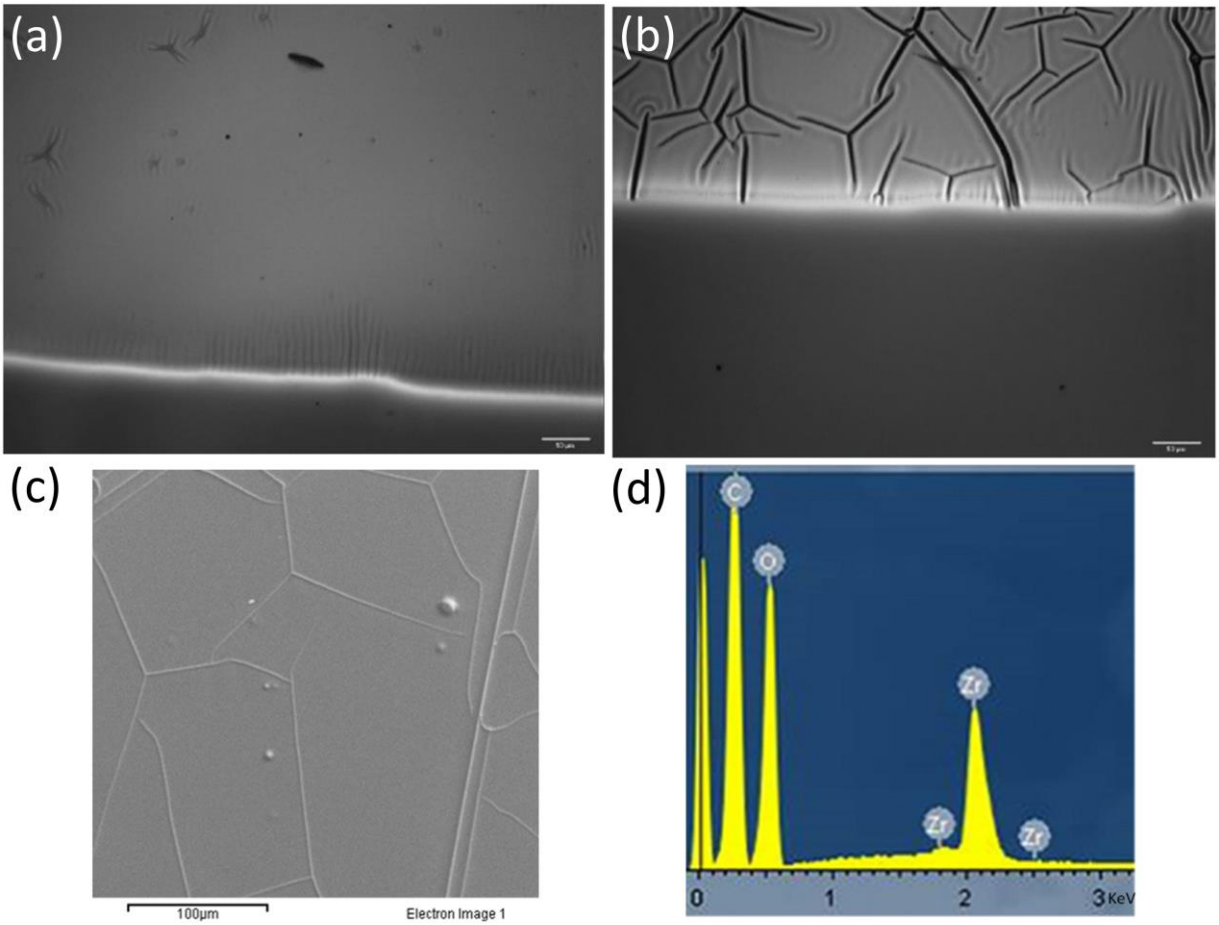


Figure 5.8: Confocal microscopy with 20 x lens shows the **(a)** homogeneous layers of C_{60} evaporated on ZrO_2. **(b)** Different region of the same sample presents some cracks on the semiconductor layer. Scales of 50 µm. **(c)** SEM of the C_{60} surface. 500 times of amplification. Scale of 100 µm. **(d)** EDX composition of the C_{60}/ZrO_2/glass substrate.

The electrical characterization of the C_{60}/ZrO_2 transistors was carried out on two Keithley electrometers. The I *vs* V curves with the output and transfer characteristics of only one TFT is presented in figures 5.9a and b, respectively. The output characteristic of other devices is not considered in this discussion due to the large leakage current obtained. Therefore, this sample represents the only working device that presented lower leakage and considerable current

modulation due to some particularity and absence of fissure close to the semiconducting channel. The leakage present in other devices can also be related to the discussion about the leakage current in the ZrO_2 non-alkoxide transistors, in the previous chapter.

The output curves present modulation of the drain current (I_D) by gate voltage up to V_G = 4 V. The transfer characteristic shows the transistor on and off-states. The off-state occurs at gate voltage lower than the threshold (V_T = 1.1 V) at I_{OFF} = 2.5 x 10^{-8} A, while the on-state occurs at I_{ON} = 7.1 x 10^{-7} A and V_G > 3 V, showing an on/off ratio equal to 28. The transconductance (g_m) and the mobility (μ) of the semiconductor channel were calculated at V_G = 2 V through equations presented in chapter 1. The values of transconductance is g_m = 3.5 x 10^{-7} S and mobility is μ = 0.26 $cm^2/V.s$, showing that the device presents high mobility for an organic semiconductor and comparable to a-Si [26], but lower compared to the outstanding mobility of graphene [27] or of inorganic compounds such as MoS_2 with μ = 200 – 500 $cm^2/V.s$ [28]. The leakage current (I_G curve) is still high and even comparable to I_D due to the fissures on zirconia layers as presented in microscopy images. The leakage is responsible for the low performance of the device and absence of transistor characteristics in other devices. Again, the leakage mechanism that may explain the behavior of these samples is presented in the previous chapter.

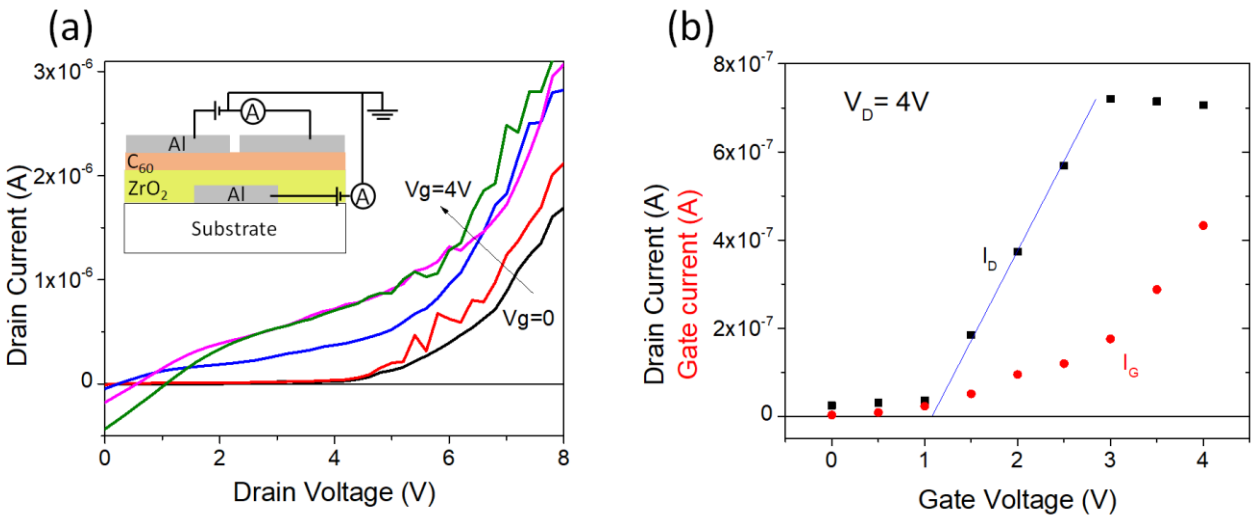


Figure 5.9: (a) Output and **(b)** transfer curves of a ZrO_2/C_{60} TFT .

2.7 Different immersion speed and thermal annealing

In order to reduce the thickness and cracking on the film surface, as observed in previous microscopy images, a study was performed to understand the effects of the film thickness obtained at different deposition rates under higher thermal annealing temperature.

The zirconia films obtained by dip-coating with immersion rate of 100 mm/min and thermal annealing at maximum temperature of 150 °C presented thick films and cracked surface. The low annealing temperature occurred due to beginning of the film deterioration and detachment from the substrate at higher temperatures. To solve this problem, new zirconia films were systematically obtained and investigated in order to get thinner films, which were resistant to higher temperatures. For that reason, the dip-coating rate was varied from 2 mm/min to 70 mm/min.

Figure 5.10 shows the plot of the thickness and surface roughness of the films as function of the deposition speed and thermal annealing. The data were obtained through Confocal microscopy. It is possible to notice that slower deposition leads to thinner films. The thickness shows a tendency to reduce at higher thermal annealing temperature, as verified in the figure.

The surface roughness presented in figure 5.10b shows a close relation with the film thickness. The thicker films remain with low roughness at thermal annealing at 150 °C, which is the case of the samples and devices first analyzed in this chapter. However, when thicker samples are thermal annealed at 250 °C the film starts to crack and detach from the substrates, showing large increases in the surface roughness as can be seen in figures 5.10b. The figure 5.11 presents the confocal and scanning electron microscopies images of the different samples thermal annealed at 250 °C.

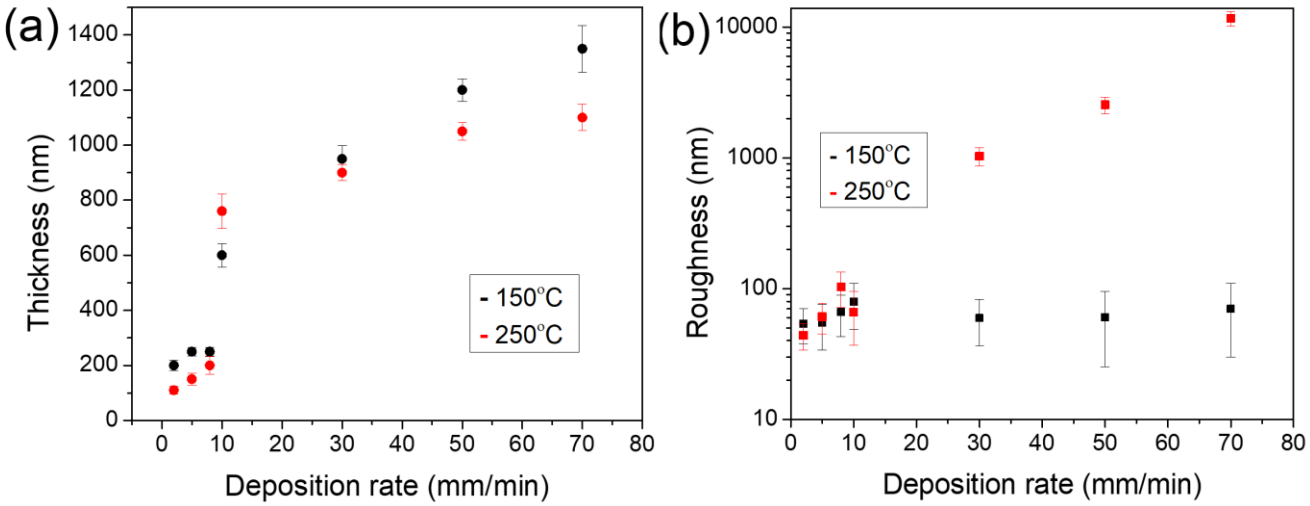
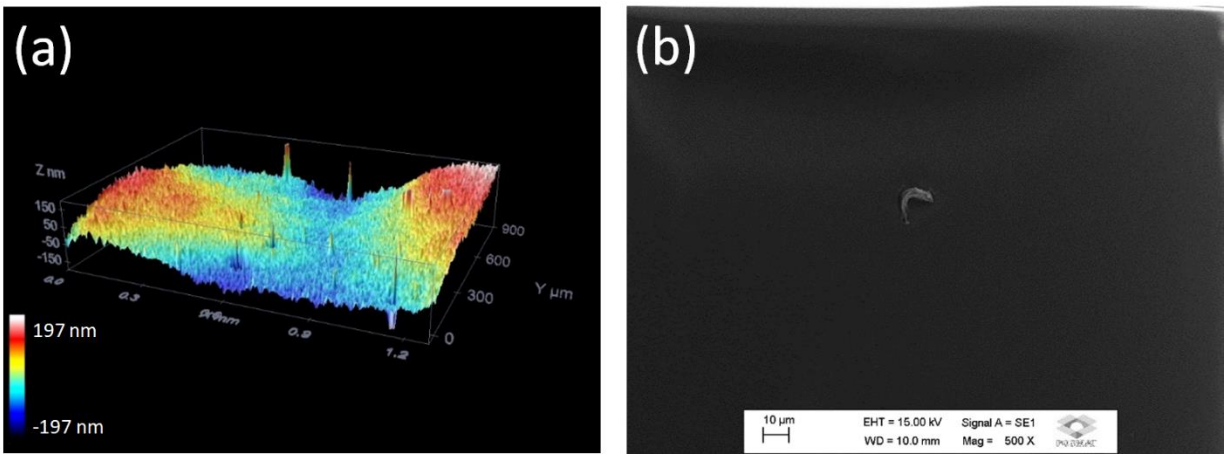


Figure 5.10: (a) Thickness and **(b)** root mean square roughness of the zirconia films as function of the deposition speed and thermal annealing at 150°C for 2 hours, and 250°C for 1 hour.

The images (a) and (b) show the ZrO_2 deposited at 10 mm/min that produced the thinnest film that remained intact, without fissures nor detaching from the substrate. Samples deposited at 30 mm/min (images c and d) show higher roughness and presence of fissures on the surface that is further increased for deposition speed of 50 mm/min (e and f). The thicker zirconia film obtained at 70 mm/min starts to detach from the substrate, as can be seen in images (g) and (h), where the films begins to wind, producing rolled sheets on the surface. The cracks are product of the higher annealing temperature that leads to the elimination of the glycol ethylene from the films.



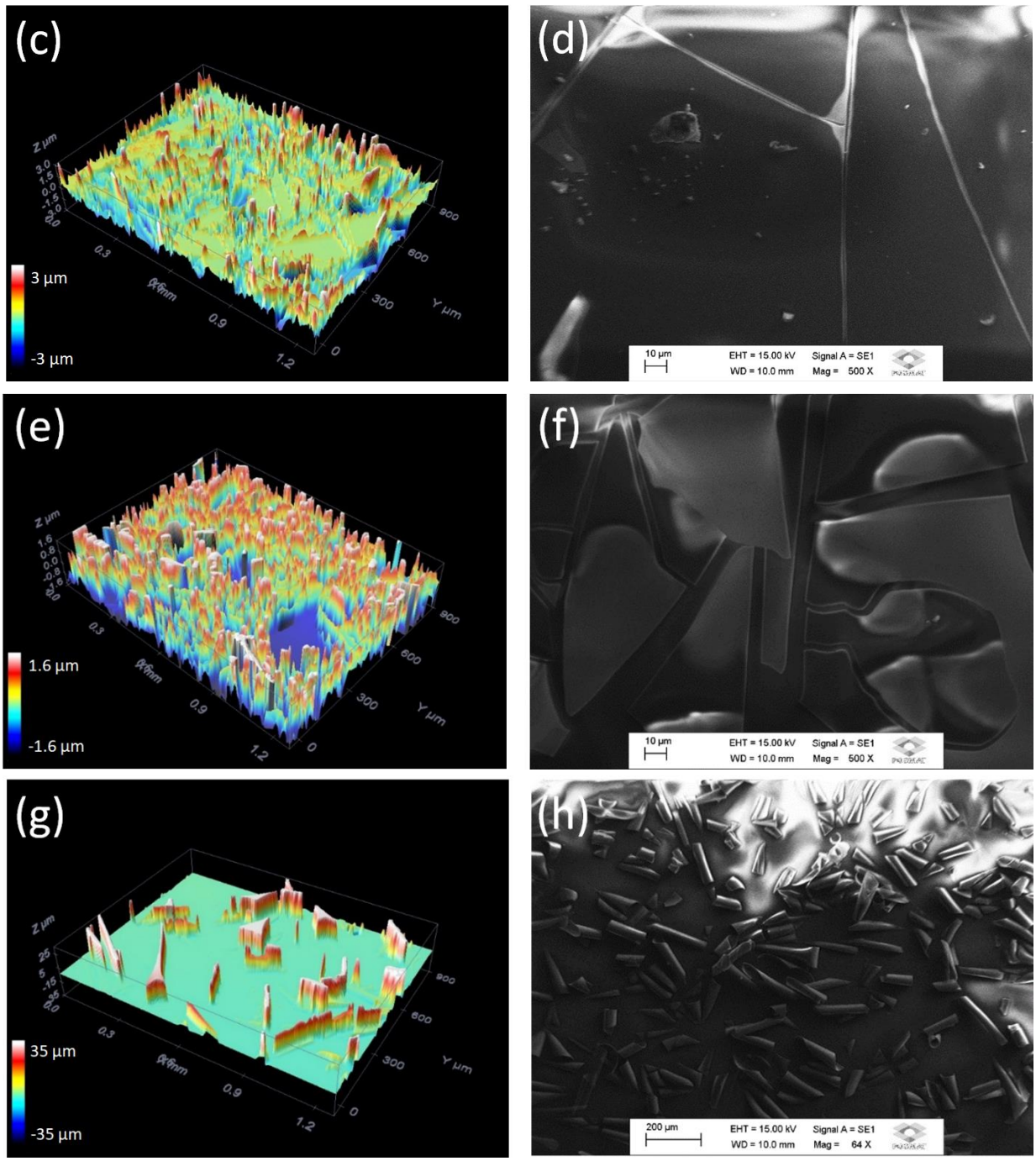


Figure 5.11: Confocal and electron microscopy of the ZrO_2 films on glass substrate after thermal annealing at 250 °C and deposition speed of **(a-b)** 10 mm/min; **(c-d)** 30 mm/min; **(e-f)** 50 mm/min; **(g-h)** 70 mm/min.

The figure 5.12a shows the elemental analysis of the samples to obtain a qualitative analysis of the influence of the thermal annealing at 250 °C on the remained material in samples deposited at different rates. The elements plotted are only oxygen and zircon, totalizing atomic composition of 100%, because they are related to the dielectric oxide film. It is important to

emphasize that the oxygen is abundantly present in the glass substrate. Other elements like Ca, K, Na, and Si, also related to the glass substrate, were removed from this evaluation. It is possible to verify in figure 5.12a that the zircon/oxygen ratio content is reduced for immersion rate higher than 10 mm/min, which can be related to the material detaching from the substrate surface that becomes higher at 50 and 70 mm/min. The low zircon content present in the sample deposited at 10 mm/min may be related to the lower thickness and consequently lower quantity of material on the substrate surface.

The transmittance present in figure 5.12b shows the higher transmittance, of about 90 %, occurs on the sample with lower deposition speed. The high transmittance and interference fringes present in this sample may be related to the thinner, smoother and more homogeneous zirconia film obtained, as previously verified by its low roughness and thickness from figures 5.10a and b. However, the sample deposited at 30 mm/min presents the lower transmittance that is probably associated to the presence of fissures on the film surface that scatters the light, thus reducing the transparency of the film. Finally, the samples deposited at 50 and 70 mm/min present higher transmittance due to the reduction of zirconia film caused by the film detachment from the substrate.

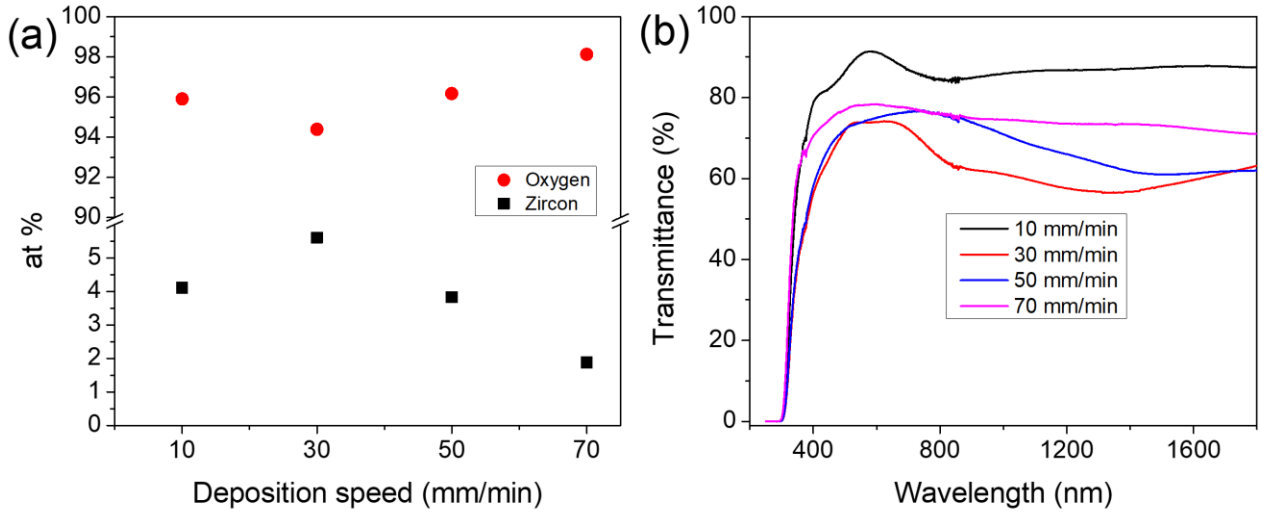


Figure 5.12: (a) Characterization of the zirconia films by EDX to verify the layer composition and the **(b)** UV-Vis-NIR transmittance of the same samples deposited at different speeds.

In summary, it was demonstrated in this section that the zirconia film can be improved aiming high quality electronic applications. The reduction of the immersion rate and increase of annealing temperature led to thinner, smoother, and purer zirconia films. This method is still

under study concerning the application to MIM capacitors, in order to verify the electrical properties of the enhanced zirconia films through electrical characterization.

CONCLUSION

Results related to zirconia thin film deposited by Pechini method is reported in this chapter. Samples and devices obtained with deposition speed of 100 mm/min and annealing up to 150 °C showed high transparency and homogeneity, although some cracking on the dielectric layer reduced the functionality of the evaluated transistors. However, MIM capacitors were better evaluated in order to understand the electric characteristics of the zirconia film. The capacitors showed high capacitance and electrical resistivity, all indispensable characteristics for applications in FETs. Due to the low annealing temperature, residues of carbon from the precursors may have contributed to the reduced dielectric constant obtained in electrical impedance spectroscopy.

The utilization of different deposition rates and higher annealing temperature aims the obtaining of more homogeneous and thinner films with better dielectric characteristics. These films are being applied and investigated in capacitors. The new thinner and smoother ZrO_2 film obtained by Pechini with deposition temperatures up to 250 °C promises good characteristics for application as insulating dielectric in capacitors and FETs, besides the suitability for applications on polymeric flexible substrates.

REFERENCES

[1] J.F. Oliveira, Deposição de filmes de ZrO2 modificados sobre substratos metálicos, Universidade Federal do Rio Grande do Norte, 2010.

[2] A. Majedi, A. Abbasi, F. Davar, Green synthesis of zirconia nanoparticles using the modified Pechini method and characterization of its optical and electrical properties, J. Sol-Gel Sci. Technol. 77 (2016) 542–552. doi:10.1007/s10971-015-3881-3.

[3] D.F. Maia, D.A. Costa, A.C.F.M. Costa, L. Gama, H.L. Lira, Morphological aspects of zirconia from Pechini method, (2000).

[4] D. Panda, T.-Y. Tseng, Growth, dielectric properties, and memory device applications of ZrO2 thin films, Thin Solid Films. 531 (2013) 1–20. doi:10.1016/j.tsf.2013.01.004.

[5] H. Zhang, B. Gao, B. Sun, G. Chen, L. Zeng, L. Liu, X. Liu, J. Lu, R. Han, J. Kang, B. Yu, Ionic doping effect in ZrO2 resistive switching memory, Appl. Phys. Lett. 96 (2010) 123502. doi:10.1063/1.3364130.

[6] R.P. Santos, Estudo comparativo das propriedades de dois sistemas cerâmicos de zircônia/ítria antes e após o processo de sinterização, Universidade Anhanguera de São

Paulo, 2014.

[7] C.A. Amorim, G. Gozzi, D.L. Chinaglia, F.J. dos Santos, L.F. Santos, Synthesis of Transparent Semiconducting Metal-oxides via Polymeric Precursor Route for Application in Thin-film Field-Effect Transistors, MRS Adv. 1 (2016) 489–494. doi:10.1557/adv.2016.224.

[8] R.G. Freitas, R.T.S. Oliveira, M.C. Santos, L.O.S. Bulhões, E.C. Pereira, Preparation of Pt thin film electrodes using the Pechini method, Mater. Lett. 60 (2006) 1906–1910. doi:10.1016/j.matlet.2005.12.050.

[9] F. Pan, S. Gao, C. Chen, C. Song, F. Zeng, Recent progress in resistive random access memories: Materials, switching mechanisms, and performance, Mater. Sci. Eng. R Reports. 83 (2014) 1–59. doi:10.1016/j.mser.2014.06.002.

[10] U. Zschieschang, R. Hofmockel, R. Rödel, U. Kraft, M.J. Kang, K. Takimiya, T. Zaki, F. Letzkus, J. Butschke, H. Richter, J.N. Burghartz, H. Klauk, Megahertz operation of flexible low-voltage organic thin-film transistors, Org. Electron. Physics, Mater. Appl. 14 (2013) 1516–1520. doi:10.1016/j.orgel.2013.03.021.

[11] H. Usta, A. Facchetti, Polymeric and Small-Molecule Semiconductors for Organic Field-Effect Transistors, Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim, 2015. doi:10.1002/9783527679973.ch1.

[12] L. Rossi, Transistores Orgânicos de Efeito de Campo em Arquitetura Vertical, Universidade Federal do Paraná, 2012.

[13] L. Rossi, K.F. Seidel, W.S. MacHado, I.A. Hümmelgen, Low voltage vertical organic field-effect transistor with polyvinyl alcohol as gate insulator, J. Appl. Phys. 110 (2011) 19–24. doi:10.1063/1.3660406.

[14] P.A. LESSING, Mixed-cation oxide powders via polymeric precursors, Am. Ceram. Soc. Bull. 68 (1989) 1002–1007.

[15] A. SOANCA, A. ROMAN, M. MOLDOVAN, I. PERHAITA, L. TUDORAN, M. ROMINU, Study on thermal behaviour, structure and filler morphology of some indirect composite resins, Dig. J. Nanomater. Biostructures. 7 (2012) 1071–1081.

[16] P.H.P. D'ALPINO, R.P. ARAÚJO, A.H.M. GONZÁLEZ, V. DI HIPÓLITO, C.J. VALDUGA, D.I. DOS SANTOS, C.F. GRAEFF, Inorganic characterizations and filler particles morphology of self-adhesive cements, Int. J. Adhes. Adhes. 68 (2016) 62–69.

[17] A. Hojabri, Structural and optical characterization of ZrO 2 thin films grown on silicon and quartz substrates, J. Theor. Appl. Phys. 10 (2016) 219–224. doi:10.1007/s40094-016-0218-8.

[18] D. Xiao, G. He, Z. Sun, J. Lv, P. Jin, C. Zheng, M. Liu, Microstructure, optical and electrical properties of solution-derived peroxo-zirconium oxide gate dielectrics for CMOS application, Ceram. Int. 42 (2015) 759–766. doi:10.1016/j.ceramint.2015.08.177.

[19] M. Kosmulski, P. Próchniak, C. Saneluta, Quantitative assessment of hysteresis in voltammetric curves of electrochemical capacitors, Adsorption. 15 (2009) 172–180. doi:10.1007/s10450-009-9169-6.

[20] M.F. El-Kady, V. Strong, S. Dubin, R.B. Kaner, Science, 335 (2012) 1326–1330.

[21] X. Chen, Y. Wang, J. Zhou, W. Yan, X. Li, J.J. Zhu, Electrochemical impedance

immunosensor based on three-dimensionally ordered macroporous gold film, Anal. Chem. 80 (2008) 2133–2140. doi:10.1021/ac7021376.

[22] G.D. Wilk, R.M. Wallace, J.M. Anthony, High-*k* gate dielectrics: Current status and materials properties considerations, J. Appl. Phys. 89 (2001) 5243–5275. doi:10.1063/1.1361065.

[23] A. Javey, H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. McIntyre, P. McEuen, M. Lundstrom, H. Dai, High-kappa dielectrics for advanced carbon-nanotube transistors and logic gates., Nat. Mater. 1 (2002) 241–246. doi:10.1038/nmat769.

[24] J. Liu, M. Liao, M. Imura, A. Tanaka, H. Iwai, Y. Koide, Low on-resistance diamond field effect transistor with high-k ZrO2 as dielectric., Sci. Rep. 4 (2014) 6395. doi:10.1038/srep06395.

[25] Y. Dora, S. Han, D. Klenov, P.J. Hansen, K. No, U.K. Mishra, S. Stemmer, J.S. Speck, ZrO2 gate dielectrics produced by ultraviolet ozone oxidation for GaN and AlGaN/GaN transistors, J. Vac. Sci. Technol. B Microelectron. Nanom. Struct. 24 (2006) 575. doi:10.1116/1.2167991.

[26] C.R. Kagan, D.B. Mitzi, C.D. Dimitrakopoulos, Organic-Inorganic Hybrid Materials as Semiconducting Channels in Thin-Film Field-Effect Transistors, Science, 286 (1999) 945–947.

[27] L. Liao, Y.-C. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K.L. Wang, Y. Huang, X. Duan, High-speed graphene transistors with a self-aligned nanowire gate, Nature. 467 (2010) 305–8. doi:10.1038/nature09405.

[28] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, A. Kis, Single-layer MoS2 transistors, Nat. Nanotechnol. 6 (2011) 147–50. doi:10.1038/nnano.2010.279.

Chapter 6

SnO_2/TiO_2 based Memristors*[1]

INTRODUCTION

This chapter presents a study of SnO_2/TiO_2 heterostructure obtained by sol-gel, applied to resistive random-access memory (RRAM) devices in order to understand the conduction mechanisms of these semiconductor oxides in these devices. The current chapter was published in the Applied Surface Science as the paper entitled "Memristive behavior of the SnO_2/TiO_2 interface deposited by sol-gel" [1], with collaboration of Prof. C. F. O. Graeff.

The research in the field of advanced electronics is nowadays focused on the study and the application of memristors (memory resistors), a memory storage device. The memristor (MR) is a two-terminal element capable of changing its resistance as a function of the flowing charge *Q*. This special feature makes MR very interesting for several electronics applications such as: unconventional computing, logic and analogic operations [2,3], neural networks, and patterns recognition [4]. Resistive random-access memory (RRAM) belongs to memristor's family and is basically a device with a switchable resistance by rapid voltage pulses (sub-nanosecond) [5]. A special attention from academic community is being given to this device, as shown by the increase number of publications per year and significant progress over the past decade, in order to understand the switching mechanisms behind RRAMs [6,7]. One of the most discussed issues are the improvement of the switching features such as the on/off resistances ratio, the operation speed, and the extreme endurance ($>10^{12}$ cycles) in metal oxides [8].

In a typical configuration, a MR consists of a sandwich structure based on thin layers of a semiconducting or insulating material (e.g. TiO_2) with specific charge-transport characteristics between two electrodes. The first model presented a thin layer of doped TiO_{2-x} grown on undoped TiO_2 [9] with memristive hysteresis behavior under application of an external bias. To understand the carrier-type dependent switching kinetics, much attention has been given by the academic community to NiO_x and TiO_x, p and n-type semiconductors, respectively [10]. Also, the combination of both ionic and electronic solid-state transport phenomena leads to a

*[1] M. H. Boratto et al, Applied Surface Science, v.410, pp. 278-281, 2017.

reproducible resistance-switch [9]. The semiconducting layers for MRs, also called the storage layer, can be fabricated by several methods [6], mainly including atomic layer deposition (ALD) [11], pulsed laser deposition (PLD) [12], magnetron sputtering [13], thermal and plasma oxidation [14,15], and sol–gel chemical route [16]. As already mentioned in previous chapters, the sol–gel is a deposition method that requires considerably less technology and is potentially less expensive in comparison with the above cited techniques. This method is suitable for fabrication of thin oxide layers such as TiO_2 [17,18] and SnO_2 [19-22] as also reported in previous chapters. The interest in using transition metal oxides (e.g. TiO_2, SnO_2, ZrO_2, ZnO) is due to their structural simplicity, low power consumption, fast switching and high integration density [6]. In respect to the electronic potential barrier (Schottky barrier), the work function of the metal electrode has shown no strong effect at the interface with TiO_2 [23]. However, the defects generated by metal deposition and the oxygen vacancies from the oxide govern the electronic barrier at the metal-semiconductor interface [24]. In order to optimize the performance of RRAMs, research on material doping [25], electrodes [26], and interface [27] engineering have been reported. Inorganic RRAMs operating as storage media have a remarkable advantage over organic ones in switching stability, while organic RRAMs have advantage in high-mechanical stability, simple fabrication, and low cost [6].

The inorganic RRAM based on low-cost Sb:SnO_2 and TiO_2 thin films deposited by sol-gel working as storage layer presents nanocrystalline grains of rutile phase for SnO_2 [19] and anatase phase for TiO_2 [18], both intrinsic n-type semiconductors due to their oxygen vacancies and interstitial atoms [28-30], as already discussed in chapter 3, which may contribute to smaller grain size that is usually responsible for creation of electronic barriers at the grain boundaries [23,24]. These materials have comparable electronic bandgap energies (E_G = 3.5 – 4 eV) but optical and electronic properties quite different [31], which are highly dependent on the deposition technique.

1 METHODOLOGY

1.1 Sb:SnO_2 and TiO_2

The obtaining process of the colloidal suspension of antimony doped tin oxide (4 at% Sb : SnO_2) has been previously described in chapter 3.

The sol-gel fabrication of titanium oxide (TiO_2) was carried out by hydrolysis and condensation of titanium (IV) isopropoxide alkoxide using a high molar ratio of water/alkoxide (200/1), isopropanol as co-solvent, HNO_3 as catalyst, and Triton X-100 as surfactant [18,32].

Nitric acid (2.6 mL) was added to a solution of deionized water (185 mL) and isopropanol (57 mL) followed by dropwise addition of titanium (IV) isopropoxide (15 mL) under stirring and heating at 85 °C for four hours. The concentration of this solution was performed by evaporating the solvent and dispersants at 100 °C until reach a volume of 50 mL, which was followed by the addition of the surfactant Triton X-100 under stirring for 30 minutes. This final solution was used for thin film deposition on the devices.

1.2 Device assembly

Prior to any deposition, the glass substrates were cleaned in ultrasonic bath during 15 minutes by three steps with different solutions: mixture of detergent and water, deionized water, and isopropanol. Aluminum contacts (bottom) were deposited on clean substrates by evaporation at a pressure of 10^{-3} Pa. A TiO_2 layer was spin-coated at speed of 2000 rpm for 60 s on top of the as-deposited Al contact followed by layer calcination for 10 minutes at 80 °C. A $Sb:SnO_2$ layer was then deposited following the same spin-coating procedure but with a final thermal annealing at 400 °C for 2 hours. To finish the device assembling, as shown in figure 5.1a, the top Al electrode was evaporated.

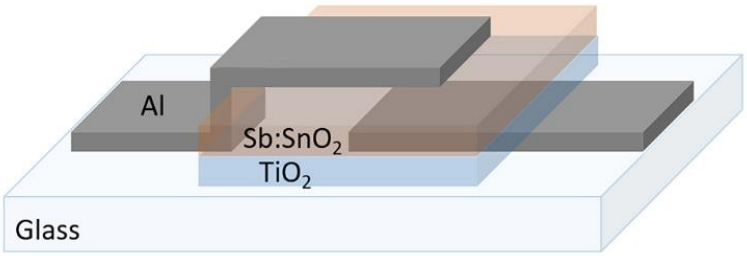


Figure 6.1: Device diagram Al/$Sb:SnO_2$/TiO_2/Al (bottom)/substrate. The overlap area of electrodes is A = 0.04 cm^2.

TiO_2 and $Sb:SnO_2$ thin films were individually deposited on clean glass substrates by the same spin-coating procedure in order to study their structural phase through XRD and optical transmittance with bandgap evaluation by UV-Vis Spectroscopy.

1.3 Characterization

The XRD characterization was performed in a Rigaku model D/MAX 2100, in 2θ mode and incident angle of 1.5°. UV-Vis spectroscopy was performed on a Perkin Elmer system model Lambda 1050, and the bandgap of the two semiconductors were consequently obtained

by the Tauc plot [19]. These characterizations were performed on TiO_2/substrate and Sb:SnO_2/substrate.

A confocal microscopy was performed on the Sb:SnO_2 film on top of the TiO_2 layer to determine their superficial morphology. The Leica model DCM-3D equipment was used for this characterization. The thickness of the SnO_2/TiO_2 layer was also obtained by confocal. Electrical measurements were performed by Current *vs* voltage (I *vs* V) curves, Cyclic Voltammetry (CV) from +5V to -5V at 100 mV/s, and square wave voltages of -5V (set), +5V (reset) and -0.5V (read) in an AUTOLAB PGStat301 equipment.

2 RESULTS

2.1 SnO_2 and TiO_2 Thin Films

Figure 6.2 shows the Tauc plot of the thin films of Sb:SnO_2 and TiO_2 deposited separated on glass substrate, with thermal annealing at 400 °C for 2 hours. The indirect bandgap calculated for the TiO_2 was about 3.5 eV, and the direct one for Sb:SnO_2 was 4.2 eV. The option for considering the direct bandgap nature of the SnO_2 relies in most of works reported in literature. Although matter of controversy, the indirect transition of the SnO_2 was also considered in chapter 3 of this work, that relies on the recent work developed by Floriano and coworkers [33].

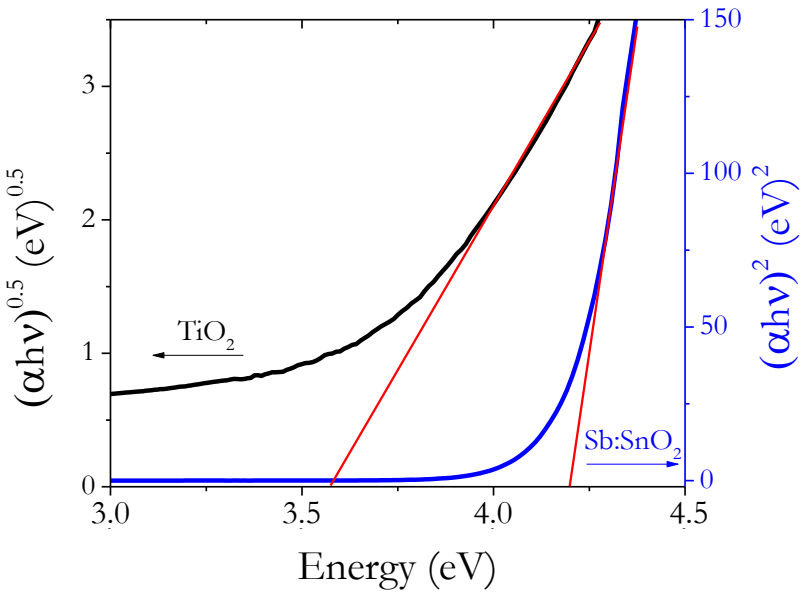


Figure 6.2: Tauc plot of TiO_2 and SnO_2 thin films on glass substrate for bandgap calculation.

Figure 6.3 presents the XRD for the samples previously analyzed by UV-Vis: TiO_2 and SnO_2 thin films deposited on glass substrate. The structure found for these films are anatase (JCPDS #089-4921) and rutile (#088-0287) for TiO_2 and SnO_2, respectively. The $Sb:SnO_2$ and TiO_2 deposited by sol-gel presented rutile [19,22], and anatase [18] nanocrystals as reported in previous works developed by our research group. The crystallite sizes estimated by Scherrer equation for the three most intense peaks in each diffractogram (fig. 6.3) show average values as high as 10 nm and 7 nm for TiO_2 and SnO_2, respectively. The three most intense peaks considered for calculations are related to the plans (101), (200) and (211) for TiO_2, and (110), (101) and (211) for SnO_2.

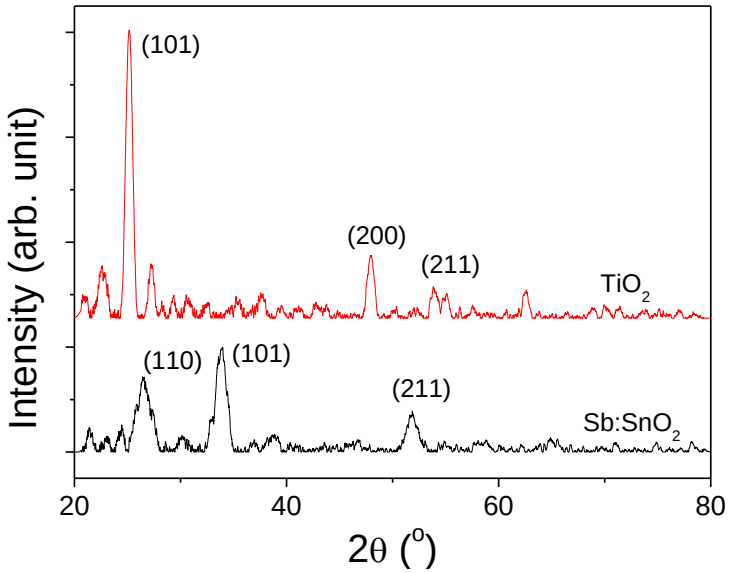


Figure 6.3: Diffractogram of the TiO_2 and $Sb:SnO_2$ films that present anatase and rutile nanocrystalline phases, respectively.

2.2 Memristor devices

Figure 6.4a shows the positions on the sample surface where Confocal microscopy were performed. The region 1 is the border of the two oxide films on the Al bottom electrode, that shows the thickness of the $Sb:SnO_2/TiO_2$ (figure 6.4b). The mean thickness of the storage layer was obtained through several measurements on this region that presents 460 ± 20 nm. The relative thick layer obtained is related to the sol-gel viscosity and spin-coating speed, that unfortunately affects largely the memory switching speed. A thinner layer is favorable to a higher frequency of operation [26]. The region 2 in figure 6.4a is the SnO_2 surface with confocal image

presented in figure 6.4c. The root mean square (rms) roughness of SnO_2 surface is about 108 nm, which represents a considerable roughness on the surface, which may contribute with generation of defects in the SnO_2/Al (top electrode) interface.

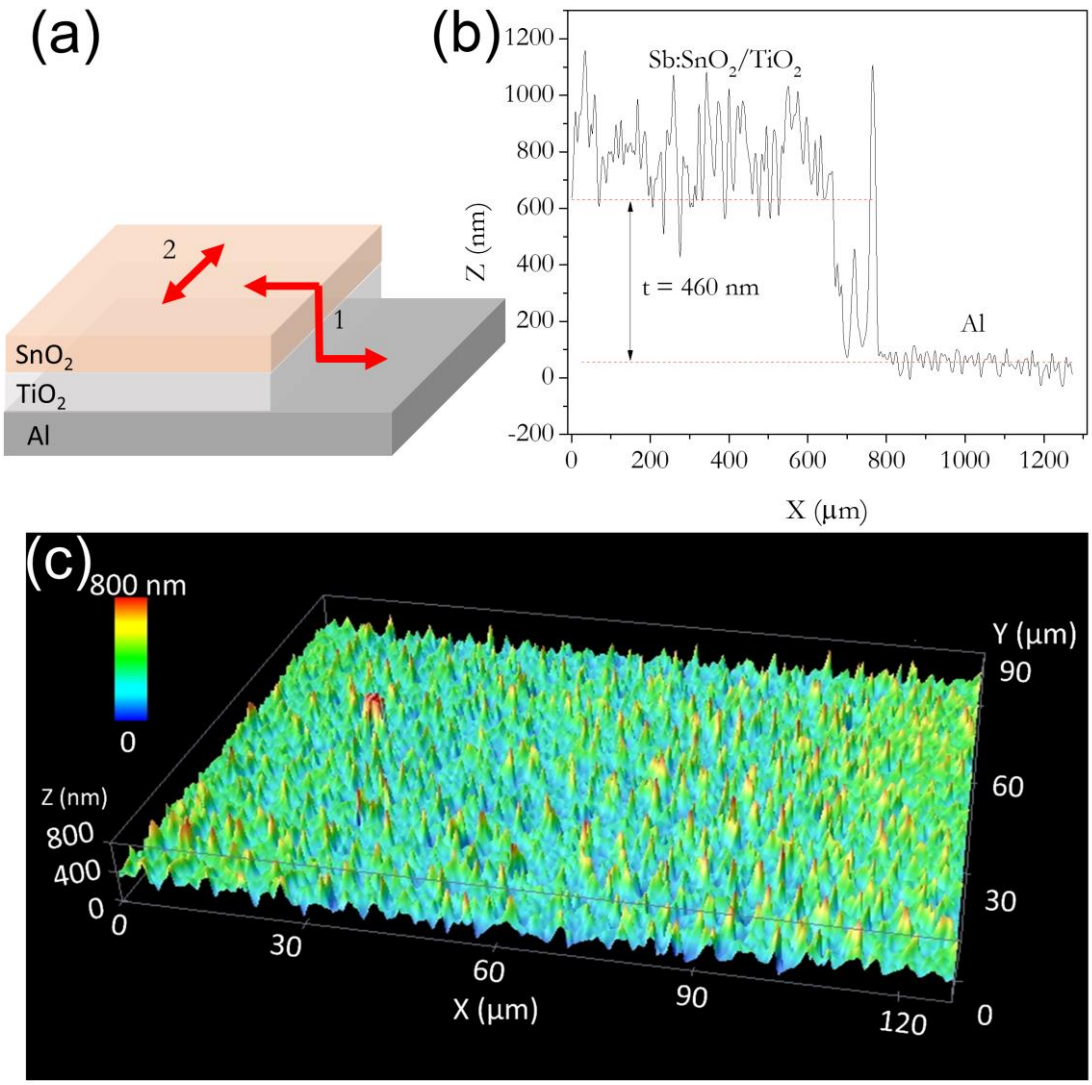


Figure 6.4: (a) Regions on the sample where Confocal Microscopy were performed. **(b)** Cross section confocal image of the Sb:SnO_2/TiO_2 on top of Al electrode (region 1 in image a) that presents the thickness of the oxides t = 460 nm. **(c)** Confocal Microscopy, topographic mode, of the SnO_2 surface (region 2 in image a) prior to Al top electrode deposition.

Figure 6.5a shows the reversible current response of the Sb:SnO_2/TiO_2 devices over 5 successive cycles at a voltage scan of 100 mV/s at room temperature and atmosphere. In order to understand the memristive state transitions between two voltage values (+5V and -5V) a triangular wave function (ramp) has been considered for this measurement, figure 6.5b. Current

flowing through the device retraces almost the same pattern exhibited in the preceding cycle, which confirms a reversible behavior. In figure 6.5a a typical butterfly-shaped plot (in $\log_{10}$I *vs* V plot) is obtained, confirming the memristive feature of the device. This can be confirmed considering the "pinched" shape of the current curves, a sufficient and necessary condition to recognize a device as a memristor [34]. In fact, one can notice that, reading current at a fixed voltage (V_{READ}), it shows different values depending on the position in the cycle. The different current is due to the high resistance state (HRS) and a low resistance state (LRS), which presents low and high current, respectively. Such resistance states are induced by voltage sweep crossing specific voltage values: V_{SET} (-3.0 V) sets the device into LRS, and V_{RESET} (+1.5 V) sets it into HRS. This characteristic of opposite V_{SET} and V_{RESET} polarities means the device operates in bipolar switching, that may be related to trap controlled space charge limited current (SCLC) [6] due to the size of nanocrystallites that represent intrinsic crystal defects in both semiconductors of the storage layer. The device showed non-linear current (non-ohmic behavior) in LRS, typical phenomenon where the electric field rules the device's current [23]. The average on/off current ratio, in LRS/HRS, was 8.3 x 10^2 at V_{READ} = -0.2 V.

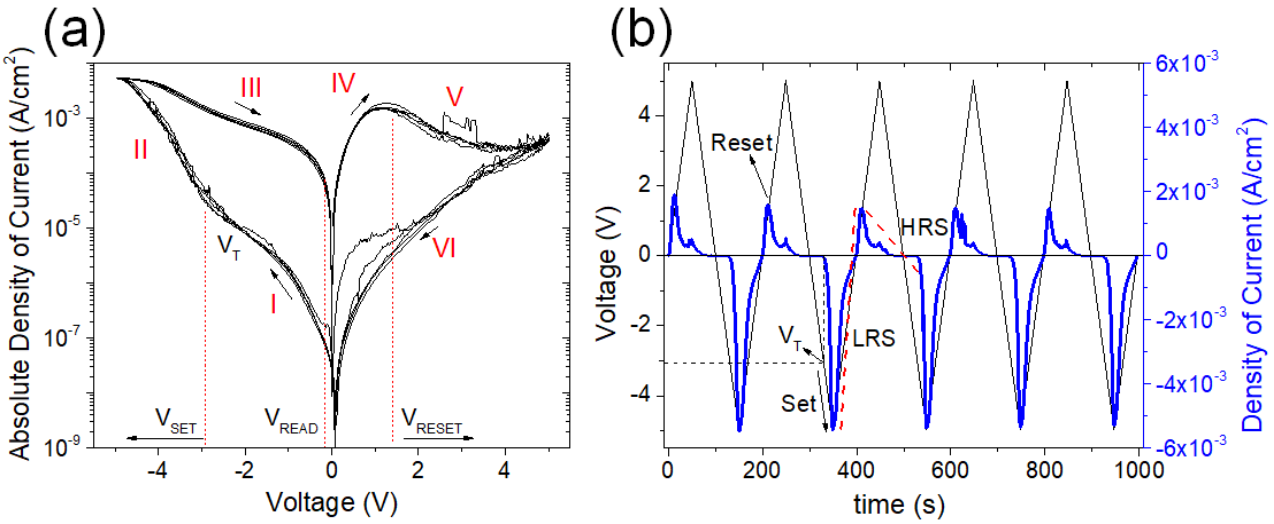


Figure 6.5: (a) Logarithm of current density *vs* Voltage curves for the (top) Al/Sb:SnO_2/TiO_2/Al memristor. Black arrows show the order of the current as function of the applied voltage, with positive bias applied on the top electrode. **(b)** The 5 cycles shown in (a) are plotted as voltage and current as function of time. Black curve represents the triangular sweep voltage applied, and the blue one represents the density of current. The cyclic voltammetry was performed with scan rate of 100 mV/s.

Process (I) in figure 6.5a shows the threshold voltage (V_T = -3.0 V), below which the device is in HRS or off-state. Process (II) shows the device setting into LRS, $|V_{SET}| > |V_T|$, that means the information (resistance value) is stored into the storage layer [10-26]. The reading

operation of on-state (process III) occurs at V_{READ} = -0.2 V. In process IV the device remains in LRS at positive bias and current increases linearly with voltage for values below V_{RESET}, which marks the onset of the reset transition. In this process (V) the resistance starts to increase, leading to a current drop, probably due to the increase of depletion region width in the channel [35]. Furthermore, the oxygen vacancies as well as the interfacial defects that accommodate trap states for electrons emitted from the cathode, are involved in the reset process [24]. Process (VI) shows the device behavior in HRS. Now, reading the information at V_{READ} on off-state, one can notice that the current shows a lower value with respect to that shown in LRS, which means the information (resistance value) was erased from the storage layer (in process V).

The forward bias is applied at the top electrode contacted to the Sb doped SnO_2, and a higher current is found when reverse biased, showing a slight rectification behavior in figure 6.5b, probably due to the n^+-n junction of the $Sb:SnO_2/TiO_2$ storage layer. Multileveled trap states may be found in this device, such as: internal layer traps, semiconductors interfacial traps, and traps at the semiconductor-metal (Al) interfaces [10]. The rectifying phenomena usually appear at these last interfaces as consequence of the Schottky barriers, which are present due to the difference of energies between the electron affinity of the semiconductor and the work function of the metal electrode [6].

Both oxide layers are composed by nanocrystallites, and present defects such as oxygen vacancies within each layer but mainly at their interface. This interfacial oxygen vacancies probably contribute to cations interlayer diffusion. Besides the ionic contribution, electrons trapped in the multiple defects are the predominant carrier charge in the conduction mechanism and switching effect in these samples. The defects act as reservoir of carriers that cause the switching at the interface with less oxygen vacancies [24]. The combination of both ionic and electronic transport results in reproducible resistance-switch [9].

Looking at the transition to LRS (regions I-II in figure 6.5a), one can notice that the initial I *vs* V characteristic of the HRS follows a linear ($I \propto V$) behavior at low voltage (process I), followed by an exponential term at higher voltage ($I \propto V^2$). Such characteristic is typical of insulator with shallow traps [6] and is represented in process II of figure 6.6. At increasing electric field, the injected electrons are pushed toward the conduction band by both Poole-Frenkel field induced emission through tunneling from traps, and Fowler-Nordheim emission from the cathode [23], illustrated in processes *i* and *ii* in figure 6.6, respectively. The de-trapping processes are probably responsible for the HRS/LRS transition [24]. Electrons drawn from multilevel traps (located at Schottky barriers and semiconductor interfaces) leave positive charged ions working as traps. Such effect provides an additional electric field in the oxides layer

which reduces the built-in potential and the depletion width, responsible for creating a conduction path through the channel [10,24,36], setting the junction into LRS, the on-state.

Electrons start tunneling into the Schottky barrier (metal/semiconductor) at positive voltage sweep (figure 6.5a IV-V), establishing a space-charge field opposite to the applied electric field, thus reducing the flowing current [6]. This effect produces a negative derived resistance region in figure 6.5a (region V). Another possible mechanism involves electrons filling trap states within the semiconductors and their interface, process V in figure 6.6. That filling results in neutral-charged occupied trap states [24]. These trapping mechanisms cause the degradation and reduction of the conducting filaments in the channel and resets the heterojunction back into the HRS, off-state, where the potential barriers recover their original state [6].

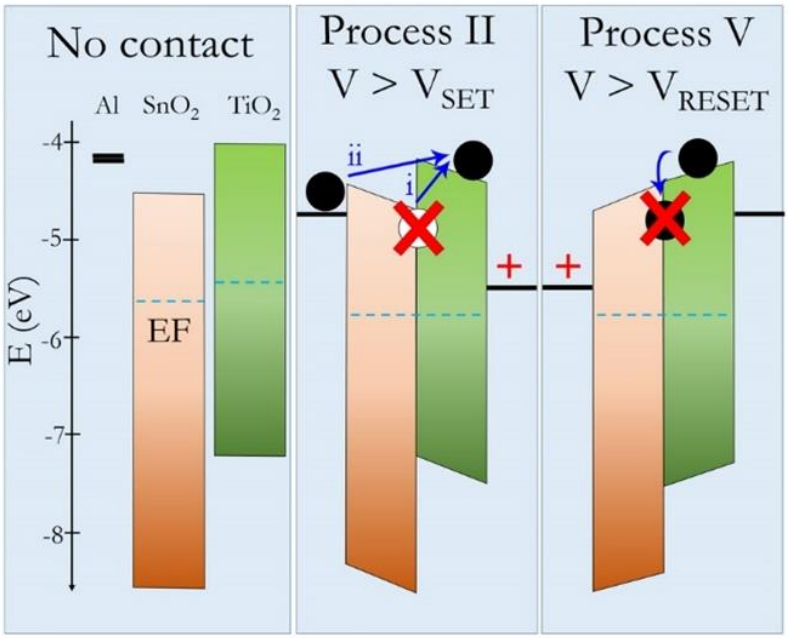


Figure 6.6: Schematic energy diagram of the semiconductors interface, charge trapping, and de-trapping processes related to processes of the figure 6.5. In process II occurs the i) de-trapping by Poole-Frenkel field induced emission, and ii) Fowler-Nordheim emission from cathode. In Process V the trap-states are filled by electrons incoming from the cathode by tunneling.

Figure 6.7a presents the cyclic voltammetry results for scan rates from 100 to 900 mV/s. The curves show a reduction of the memristive behavior of the samples at higher sweep voltage speed through the reduction of the on-state current presented in figure 6.7b. The off-state currents maintain similar values (~2 x 10^{-7}A/cm^2) that represents the maximum electric resistance of the storage layer. The on/off ratio is reduced from 8 x 10^2 to 10^1, a reduction of almost 3 orders of magnitude due to the lower on-state current at faster sweep voltages. It is also possible to notice that the absolute values of V_T increase, from -2.9 to -4.0 V. As previously described, the V_T represents the minimum voltage required to the device to set into on-state. The

faster scan rates reduce the time interval between V_{SET} and V_{MAX}, which reduces the time for de-trapping and injection charge carriers into the channel, reducing the on-state current.

Different charge states of Sb centers in the Sb:SnO_2 layer could have an important role in the switching mechanism of the device. As reported before by Geraldo and collaborators [28], Sb^{5+} ions located at grain boundaries may generate more oxygen vacancies at this region, which produce more defects into the material grain boundary that allow more ionic diffusion. Such effects are noticeable by varying the scan rate. As presented in figure 6.7a, one can notice that the intensity of the anodic peak at +1.5 V decreases at higher scan rates, which suggests a possible ionic contribution driven by diffusion through the film.

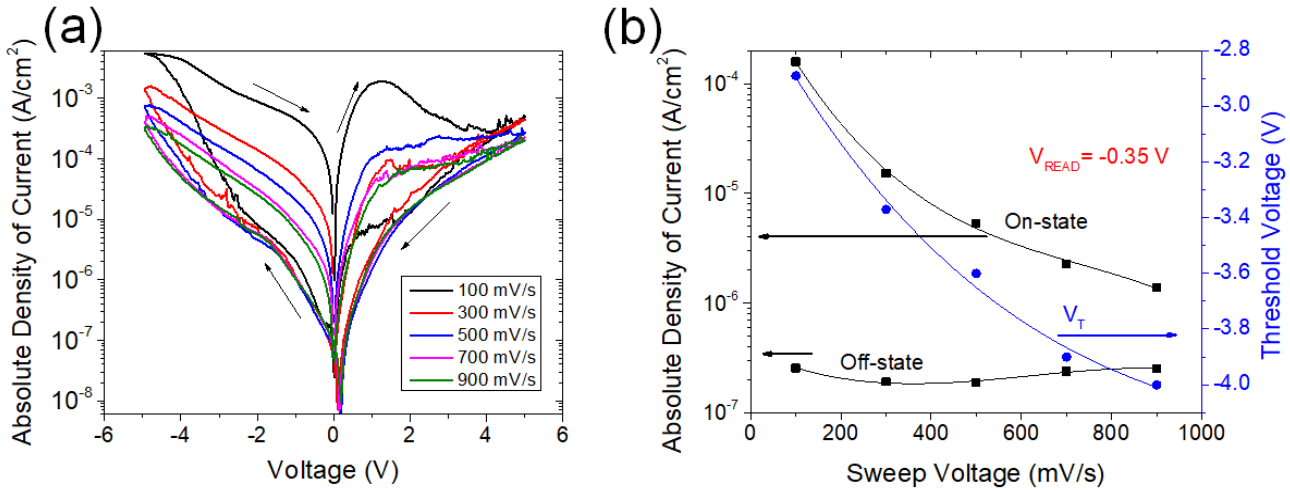


Figure 6.7: (a) Absolute logarithm of current density *vs* voltage curves of the Al/Sb:SnO_2/TiO_2/Al memristor. Black arrows show the order of the current as function of the voltage applied, with forward bias applied on the top electrode. **(b)** The absolute current and threshold voltage obtained from (a) are plotted as function of the sweep voltage speed at V_{MAX} = +5 V and V_{MIN} = -5V.

Square wave voltages with V_{SET} = -5 V, V_{RESET} = +5 V, and V_{READ} = -0.5 V were applied at a frequency of 40 mHz and 50% duty cycle. The set and reset voltages were higher than the obtained from figure 6.5a to ensure the on-off switching. Figures 6.8a and b show the results of 3 and 40 reproducible cycles under square wave voltage sweep, respectively. Figure 6.8a presents only 3 cycles for better conception. The on/off ratio is obtained from the output current at V_{READ} after V_{SET} (on-state) and after V_{RESET} (off-state). The on-state occurs at (3.4 ± 1.2) $x10^{-5}$ A, and the off-state at (3.9 ± 1.1) $x10^{-7}$ A, which produces an on-off ratio of about 9 x 10^{1}. The electrical current fluctuations presented in the figure may be related to different rates of de-trapping and trapping of charge carriers that turn the device into on- and off-state, respectively.

Despite the low frequency, the device shows stability along several operation cycles and promising memristive characteristics that may be improved by optimizing the thickness, doping level, or electrode of the devices.

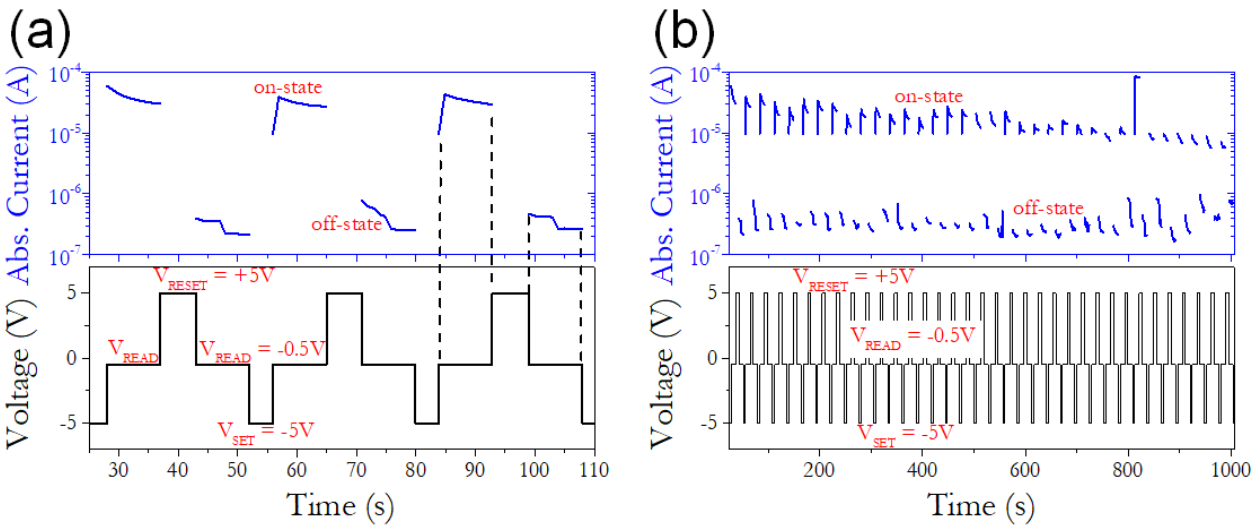


Figure 6.8: Square wave voltage applied and corresponding output current as function of time. **(a)** 3, and **(b)** 40 operation cycles of the Sb:SnO_2/TiO_2-based memristors are presented. V_{SET} and V_{RESET} occur at -5 and +5 V, respectively, and V_{READ} occurs at -0.5 V.

CONCLUSION

In this chapter, it was proposed the use of the Sb:SnO_2/TiO_2 heterostructure deposited by the sol-gel route as active layer of bipolar memristors. The interface of this binary oxide storage layer operates as bipolar switching that is related to the asymmetry in the interfaces which results in a repeatable switching behavior with well-defined switching polarity. The devices have shown repeatable switching at low operating voltages (V_{RESET} ~ 1.5V and V_{SET} ~ -3.0V), as well as a high switching resistance ratio of about 8 x 10^2. This switching mechanism could be explained by charges trapping/de-trapping in the multiple defects of the device interfaces, ruled mainly by the built-in and applied electric fields. Considering the low cost of sol-gel and the encouraging results, this memristor layout should be considered for a more in-depth study focused specifically on its optimization. Particularly, the whole thickness of the device should be reduced and optimized to increase its switching frequency. Furthermore, the effects of ionic diffusion also could be better investigated for future applications.

REFERENCES

[1] M.H. Boratto, R.A. Ramos Jr, M. Congiu, C.F.O. Graeff, L.V.A. Scalvi, Memristive Behavior of the SnO2/TiO2 Interface deposited by sol-gel, Appl. Surf. Sci. 410 (2017) 278–281. doi:10.1016/j.apsusc.2017.03.132.

[2] J. Borghetti, G.S. Snider, P.J. Kuekes, J.J. Yang, D.R. Stewart, R.S. Williams, "Memristive" switches enable "stateful" logic operations via material implication., Nature. 464 (2010) 873–876. doi:10.1038/nature08940.

[3] T. Driscoll, J. Quinn, S. Klein, H.T. Kim, B.J. Kim, Y. V. Pershin, M. Di Ventra, D.N. Basov, Memristive adaptive filters, Appl. Phys. Lett. 97 (2010). doi:10.1063/1.3485060.

[4] M.D. Pickett, G. Medeiros-Ribeiro, R.S. Williams, A scalable neuristor built with Mott memristors., Nat. Mater. 12 (2013) 114–7. doi:10.1038/nmat3510.

[5] H. Akinaga, H. Shima, Resistive random access memory (ReRAM) based on metal oxides, Proc. IEEE. 98 (2010) 2237–2251. doi:10.1109/JPROC.2010.2070830.

[6] F. Pan, S. Gao, C. Chen, C. Song, F. Zeng, Recent progress in resistive random access memories: Materials, switching mechanisms, and performance, Mater. Sci. Eng. R Reports. 83 (2014) 1–59. doi:10.1016/j.mser.2014.06.002.

[7] M. Congiu, L.G.S. Albano, O. Nunes-Neto, C.F.O. Graeff, Printable ReRAM devices based on the non-stoichiometric junction CuS/Cu2−x S, Electron. Lett. 52 (2016) 1871–1873. doi:10.1049/el.2016.2901.

[8] H.S.P. Wong, H.Y. Lee, S. Yu, Y.S. Chen, Y. Wu, P.S. Chen, B. Lee, F.T. Chen, M.J. Tsai, Metal-oxide RRAM, in: Proc. IEEE, 2012: pp. 1951–1970. doi:10.1109/JPROC.2012.2190369.

[9] D.B. Strukov, G.S. Snider, D.R. Stewart, R.S. Williams, The missing memristor found, Nature. 453 (2008) 80–83. doi:10.1038/nature06932.

[10] F. Pan, S. Gao, C. Chen, C. Song, F. Zeng, Recent progress in resistive random access memories: Materials, switching mechanisms, and performance, Mater. Sci. Eng. R Reports. 83 (2014) 1–59. doi:10.1016/j.mser.2014.06.002.

[11] B.J. Choi, D.S. Jeong, S.K. Kim, C. Rohde, S. Choi, J.H. Oh, H.J. Kim, C.S. Hwang, K. Szot, R. Waser, B. Reichenberg, S. Tiedke, Resistive switching mechanism of TiO2 thin films grown by atomic-layer deposition, J. Appl. Phys. 98 (2005) 33715. doi:10.1063/1.2001146.

[12] Z. Yan, Y. Guo, G. Zhang, J.-M. Liu, High-performance programmable memory devices based on co-doped BaTiO3., Adv. Mater. 23 (2011) 1351–5. doi:10.1002/adma.201004306.

[13] C. Chen, C. Song, J. Yang, F. Zeng, F. Pan, Oxygen migration induced resistive switching effect and its thermal stability in W/TaOx/Pt structure, Appl. Phys. Lett. 100 (2012) 253509. doi:10.1063/1.4730601.

[14] G.S. Tang, F. Zeng, C. Chen, S. Gao, H.D. Fu, C. Song, G.Y. Wang, F. Pan, Resistive switching behaviour of a tantalum oxide nanolayer fabricated by plasma oxidation, Phys. Status Solidi - Rapid Res. Lett. 7 (2013) 282–284. doi:10.1002/pssr.201206534.

[15] M.H. Boratto, L.V.A. Scalvi, Deposition of Al2O3 by resistive evaporation and thermal oxidation of Al to be applied as a transparent FET insulating layer, Ceram. Int. 40 (2014) 3785–3791. doi:10.1016/j.ceramint.2013.09.041.

[16] H. Baek, C. Lee, J. Choi, J. Cho, Nonvolatile memory devices prepared from sol-gel derived niobium pentoxide films, Langmuir. 29 (2013) 380–386. doi:10.1021/la303857b.

[17] K.P. Biju, X. Liu, E.M. Bourim, I. Kim, S. Jung, M. Siddik, J. Lee, H. Hwang, Asymmetric bipolar resistive switching in solution-processed Pt/TiO 2 /W devices, J. Phys. D. Appl. Phys. 43 (2010) 495104. doi:10.1088/0022-3727/43/49/495104.

[18] R. De Aguiar Ramos, M.H. Boratto, M.S. Li, L.V.A. Scalvi, Emission properties related to distinct phases of sol-gel dip-coating titanium dioxide, and carrier photo-excitation in different energy ranges, Mater. Res. 20 (2017). doi:10.1590/1980-5373-MR-2016-0675.

[19] M.H. Boratto, L.V.A. Scalvi, L. V. Goncharova, G. Fanchini, Effects of Solution History on Sol-Gel Processed Tin-Oxide Thin-Film Transistors, J. Am. Ceram. Soc. 99 (2016) 4000–4006. doi:10.1111/jace.14459.

[20] M.H. Boratto, L.V.A. Scalvi, J.L.B. Maciel Jr, M.J. Saeki, E.A. Floriano, Heterojunction between Al2O3 and SnO2 thin films for application in transparent FET, Mater. Res. 17 (2014) 1420–1426. doi:10.1590/1516-1439.285114.

[21] L.P. Ravaro, L.V.A. Scalvi, M.H. Boratto, Improved electrical transport in lightly Er-doped sol–gel spin-coating SnO2 thin films, processed by photolithography, Appl. Phys. A Mater. Sci. Process. 118 (2014) 1419–1427. doi:10.1007/s00339-014-8900-7.

[22] T.J. Liu, Z.G. Jin, L.R. Feng, T. Wang, Conducting antimony-doped tin oxide films derived from stannous oxalate by aqueous sol-gel method, Appl. Surf. Sci. 254 (2008) 6547–6553. doi:10.1016/j.apsusc.2008.04.021.

[23] J.J. Yang, D.B. Strukov, D.R. Stewart, Memristive devices for computing., Nat. Nanotechnol. 8 (2013) 13–24. doi:10.1038/nnano.2012.240.

[24] T.D. Dongale, S.S. Shinde, R.K. Kamat, K.Y. Rajpure, Nanostructured TiO2 thin film memristor using hydrothermal process, J. Alloys Compd. 593 (2014) 267–270. doi:10.1016/j.jallcom.2014.01.093.

[25] H. Zhang, B. Gao, B. Sun, G. Chen, L. Zeng, L. Liu, X. Liu, J. Lu, R. Han, J. Kang, B. Yu, Ionic doping effect in ZrO2 resistive switching memory, Appl. Phys. Lett. 96 (2010) 123502. doi:10.1063/1.3364130.

[26] S. Ezugwu, J.A. Paquette, V. Yadav, J.B. Gilroy, G. Fanchini, Design Criteria for Ultrathin Single-Layer Flash Memristors from an Organic Polyradical, Adv. Electron. Mater. (2016) 1600253. doi:10.1002/aelm.201600253.

[27] B. Cho, S. Song, Y. Ji, T. Lee, Electrical characterization of organic resistive memory with interfacial oxide layers formed by O2 plasma treatment, Appl. Phys. Lett. 97 (2010) 63305. doi:10.1063/1.3478840.

[28] V. Geraldo, V. Briois, L.V.A. Scalvi, C. V. Santilli, EXAFS investigation on Sb incorporation effects to electrical transport in SnO2 thin films deposited by sol-gel, J. Eur. Ceram. Soc. 27 (2007) 4265–4268. doi:10.1016/j.jeurceramsoc.2007.02.137.

[29] R.D. Shannon, J.A. Pask, Kinetics of the Anatase-Rutile Transformation, J. Am. Ceram. Soc. 48 (1965) 391–398. doi:10.1111/j.1151-2916.1965.tb14774.x.

[30] C. Terrier, J.P. Chatelon, J. a. Roger, Electrical and optical properties of Sb:SnO2 thin films obtained by the sol-gel method, Thin Solid Films. 295 (1997) 95–100. doi:10.1016/S0040-6090(96)09324-8.

[31] M. Dou, C. Persson, Comparative study of rutile and anatase SnO2 and TiO 2: Band-edge structures, dielectric functions, and polaron effects, J. Appl. Phys. 113 (2013) 83703. doi:10.1063/1.4793273.

[32] G. Oskam, A. Nellore, R.L. Penn, P.C. Searson, The Growth Kinetics of TiO 2 Nanoparticles from Titanium(IV) Alkoxide at High Water/Titanium Ratio, J. Phys. Chem. B. 107 (2003) 1734–1738. doi:10.1021/jp021237f.

[33] E.A. Floriano, L.V.A. Scalvi, M.J. Saeki, J.R. Sambrano, Preparation of TiO2/SnO2 thin films by sol-gel method and periodic B3LyP simulations, Phys. Chem. A. 118 (2014) 5857–5865. doi:10.1021/jp411764t.

[34] L. Chua, If it's pinched it's a memristor, Semicond. Sci. Technol. 29 (2014) 104001. doi:10.1088/0268-1242/29/10/104001.

[35] D. Ielmini, Resistive switching memories based on metal oxides: mechanisms, reliability and scaling, Semicond. Sci. Technol. 31 (2016) 063002–. doi:10.1088/0268-1242/31/6/063002.

[36] S. Prada, M. Rosa, L. Giordano, C. Di Valentin, G. Pacchioni, Density functional theory study of TiO2/Ag interfaces and their role in memristor devices, Phys. Rev. B - Condens. Matter Mater. Phys. 83 (2011) 1–9. doi:10.1103/PhysRevB.83.245314.

General Conclusions

It has been shown in this work the investigation of oxides with semiconducting (SnO_2 and TiO_2) and insulating (ZrO_2) characteristics that can be obtained through cost effective processes. These materials were applied to thin film transistors (TFTs), capacitors and memristors, and were thoroughly characterized concerning their structural, compositional, morphological, and electrical properties. These properties, and their relations with the obtaining processes, help us to understand the processes that may affect the final properties of thin films, and respective devices where they are applied. The main parameters related to final properties of the materials were the different aging-time of suspensions, annealing temperature, and film thickness.

In the study of the semiconductor materials, the combination of Sb:SnO_2 with TiO_2 and PCBM presented different and interesting characteristics. The junction with TiO_2 showed memristive characteristic when applied in memristors, whereas the junction with PCBM showed an increase of bipolar conduction in the PCBM/SnO_2 TFTs, promoted by the organic material.

The study of the dielectric ZrO_2 obtained by different suspensions showed that although a high dielectric loss was perceptive in capacitor devices, probably due to impurity ions remained from the chemical suspension, interesting capacitive and insulating characteristics were obtained from both ZrO_2 materials.

The results presented in this work aim to contribute in a wide area of electronic and semiconductor materials, helping readers and their future works about the conduction, working, and leakage mechanisms of the devices studied in this work. Besides, it must also contribute to the improvement of the knowledge of the investigated oxide semiconductors and insulators obtained through different methods that leads to novel results. Ways to improve the different materials obtained, in order to present comparable results to state-of-the-art materials, are described in their respective sections, and may be summarized through the improvement of annealing procedures, including time and temperatures, solution preparation, active layer thicknesses, and miniaturization of devices.