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InGaAs tunnel FET with sub-nanometer *EOT* and sub-60 mV/dec sub-threshold swing at room temperature

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InGaAs homojunction Tunnel FET devices are demonstrated with sub-60 mV/dec Sub-threshold Swing (SS) measured in DC. A 54 mV/dec SS is achieved at 100 pA/μm over a drain voltage range of 0.2–0.5 V. The SS remains sub-60 mV/dec over 1.5 orders of magnitude of current at room temperature. Trap-Assisted Tunneling (TAT) is found to be negligible in the device evidenced by low temperature dependence of the transfer characteristics. Equivalent Oxide Thickness (EOT) is found to play the major role in achieving sub-60 mV/dec performance. The EOT of the demonstrated devices is 0.8 nm. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4971830]

The interest behind several years of research on tunnel FET (TFET) devices arises from the physics of the operation of this family of devices which is based on Band-To-Band Tunneling (BTBT). BTBT allows for steep switching exceeding the limit of 60 mV/dec at room temperature. In addition, the sub-threshold characteristics of the TFET are potentially temperature independent except for the leakage floor. These characteristics make the TFET an interesting device for low power applications.[1] III–V based TFETs are being studied[2–12] mainly to solve the low drive current issue of TFETs and by far no solutions are found to deliver a reasonable drive current which could compete with the MOSFET performance at a reasonable steep sub-threshold swing (SS). To date only one recent homojunction III–V TFET is demonstrated[13] showing sub-60 mV/dec SS (in DC) while sub-60 mV/dec performance has obtained for heterojunction III–V based TFETs.[7,14] Fast pulsed I–V measurements have shown to suppress SS degrading mechanisms like Trap-Assisted Tunneling (TAT) and result in sub-60 mV/dec SS despite large SS in DC.[4] TFETs based on the combination of Si and III–V are demonstrated with SS as steep as 21 mV/dec but at extremely low (less than 1 pA) currents.[9]

This work reports the sub-60 mV/dec SS performance for a homojunction III–V TFET over a range of 1.5 orders of magnitude of drain current by scaling the equivalent oxide thickness (EOT) down to 0.8 nm.

The device structure is shown in Figure 1(a). The fabrication flow is similar to Ref. 3 and starts with the Metal-Organic Chemical Vapor Deposition (MOCVD) growth of the III–V stack on an InP substrate. The stack consists of a 10 nm InP seed layer, a 90 nm thick unintentionally doped $In_{0.53}Ga_{0.47}As$ layer which serves as the channel material, a 3 nm thick InP etch stop layer and a 50 nm n+ (Si, 1×10^{19} cm^{-3}) $In_{0.53}Ga_{0.47}As$ drain layer. A SiO_2 layer is then deposited as the hard mask and the drain of the device is defined through wet etching. The gate stack is deposited in the next step and consists of a bilayer of Atomic Layer Deposited (ALD) Al_2O_3 (1 nm) and HfO_2 (either 3 nm or 2 nm). The deposition temperature is 300 °C for both oxides. The corresponding EOT for the gate stacks are 1 nm and 0.8 nm respectively considering a relative dielectric constant of 9 for Al_2O_3 and 21 for HfO_2. It should be noted that the sample surface is treated with HCl:H_2O (1:5 volume ratio) for a minute to remove the

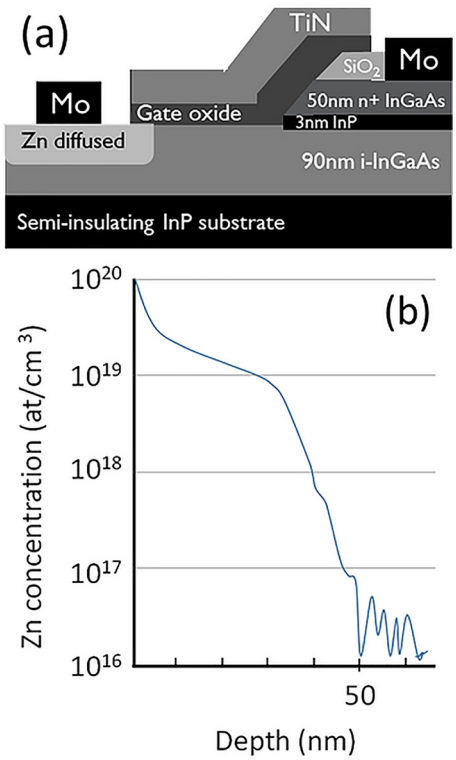

FIG. 1. (a) Device structure. (b) SIMS measurement of the Zn concentration in the source after a diffusion at 500 °C for 1 min. Active doping concentration is around 2×10^{19} cm^{-3} from Hall measurements and the junction depth is around 40 nm.

[a)]Currently at NUS, Singapore.

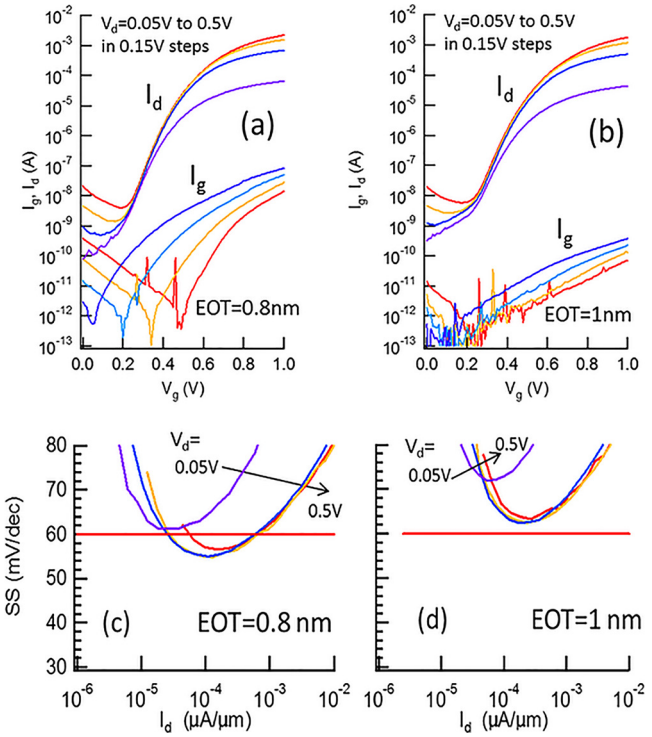

FIG. 2. (a), (b) Transfer characteristics as well as the gate leakage current for both gate stacks showing significantly lower gate leakage current than the drain current. (c), (d) Corresponding SS behaviors show that the device with 0.8 nm EOT demonstrates sub-60 mV/dec over a drain current range of 1.5 order of magnitude with a point minimum of 54 mV/dec. Horizontal line shows the thermal limit at 60 mV/dec. T = 300 K for all plots.

native oxide of InGaAs followed by a water rinse and treatment in aqueous $(NH_4)_2S$:H_2O (1:1 volume ratio) for 3 min which is reported to reduce the Al_2O_3 oxide trap density[15] prior to the gate stack deposition. 100 nm Physical Vapor Deposited (PVD) TiN is then deposited as the gate metal and patterned using SF_6 dry etching. Next, the Al_2O_3/HfO_2 bilayer gate stack is etched in diluted HF and the source of the device is formed by zinc diffusion process[2,3] which is reported first by Ref. 2 to lead to minimal TAT in the TFET characteristics as opposed to implantation. The device fabrication process does not allow for *in situ* doping of the source and so the most promising method of source formation would be diffusion. The diffusion is performed self-aligned to the gate and the gate stack is used as the diffusion mask over the channel area. The Zn diffusion is performed from the gas phase in an MOCVD epi reactor using DEZn (Diethyl zinc) precursor providing Zn dopants and TBAs (Tributyl arsine) providing arsenic overpressure to avoid arsenic outgassing from the InGaAs surface at the diffusion temperature. The diffusion temperature is 500 °C, and the duration of the diffusion is 1 min. It should be noted that this approach is applicable for the processing of scaled FET-based devices like nanowires and avoids the complexity involved in diffusion from spin-on dopants as reported before.[2,3] The process is not only limited to Zn diffusion, and the other dopant species (n-type or p-type) like Be may be diffused using a similar procedure. The Secondary Ion Mass Spectroscopy (SIMS) profile shown in Figure 1(b) suggests a junction depth of about 40 nm, an steepness of about 4.7 nm/dec and a doping concentration of about 2×10^{19} cm^{-3} comparable to the diffusion profiles from spin-on dopants.[2,3] The Mo/Al source/drain contacts are deposited afterwards. The devices receive a 400 °C anneal in forming gas (FOG) for 15 min. Fabricated devices have a gate length of 6–8 μm and a width of 400 μm.

Figures 2(a) and 2(b) show the room temperature transfer characteristics as well as the gate leakage current on the same plot for both gate stacks. The gate leakage (I_g) is significantly lower than the drain current (I_d) at any given gate voltage (V_g) and drain voltage (V_d) and as such, the SS can be extracted reliably from the drain current. The gate leakage increases with two orders of magnitude when scaling the EOT from 1 nm to 0.8 nm.

The corresponding SS behaviors extracted from the room temperature transfer characteristics of the devices are also shown in Figures 2(c) and 2(d). For the device with 1 nm EOT, SS shows a minimum of 62 mV/dec while for the device with 0.8 nm EOT, a sub-60 mV/dec SS can be seen over a drain current range of 1.5 orders of magnitude (30×) with a minimum of 54 mV/dec at 100 pA/μm. I_{60}, the maximum current at which SS is still sub-60 mV/dec, is 740 pA/μm. The SS behavior is V_d dependent since the off-state current level increases with V_d and hinders the steep portion of the characteristics. A large number of the measured devices (>70%) show sub-60 performance over a significantly wide drain current range.

Output characteristics of both devices are shown in Figures 3(a) and 3(b). Figure 3(c) is the comparison of the transconductance of both devices at $V_d = 0.5$V. The 0.8 nm EOT device slightly outperforms the 1 nm EOT device in

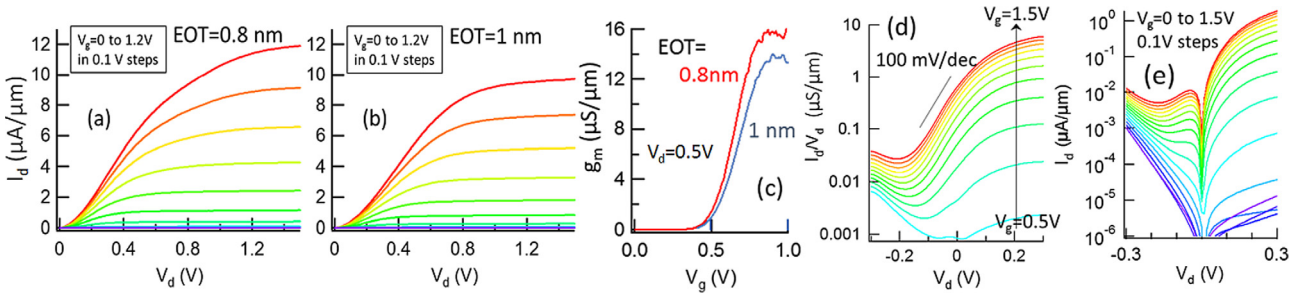

FIG. 3. (a), (b) Output characteristics for both gate stacks. Decent saturation characteristics are observed in both cases. (c) Comparison of the transconductance of both devices. The difference in on-state performance is not significant as EOT scales by 0.2 nm as evidenced from the transconductance comparison. (d) The drain conductance slope plot for the EOT = 0.8 nm device. Such characteristics are reported[16,17] to be a measure of how steep the TFET may achieve. In strong on-state, the TFET operates as an Esaki diode. Conductance slope is 100 mV/dec. (e) NDR was observed as V_g increases, and the channel inversion charge forms. The plot is for the EOT = 0.8 nm. Similar behavior observed for the EOT = 1 nm (not shown). T = 300 K for all plots.

terms of the on-state performance. The conductance slope[16,17] plot where the I_d/V_d is plotted against V_d for various V_g values is shown in Figure 3(d). In strong on-state (large V_g bias) the TFET operates as an Esaki-diode and the conductance slope method should therefore be applicable. For the sub-60 mV/dec performing TFET, the conductance slope is 100 mV/dec when biased as an Esaki diode. The Negative Differential Resistance (NDR) behavior was observed for both devices with different EOTs as shown in Figure 3(e) for the case of EOT = 0.8 nm. As V_g increases beyond the threshold voltage, the inversion charge forms in the channel, and the tunneling junction becomes operational (similar to an Esaki junction) thereby the NDR emerges. With higher V_g, the device moves to stronger inversion regime, and the tunneling current increases further.

Analysis of the multi frequency Capacitance-Voltage (C-V) behavior for both gate stacks shows a similar interface quality for both of them. The C-V was directly measured on the actual TFET devices. The extracted interface state density from the conductance technique is $\sim 2 \times 10^{12}\ cm^{-2} eV^{-1}$ at the midgap for both devices. The Capacitance Equivalent Thickness (CET) difference as suggested from the C-V characteristics matches the expected EOT difference of 0.2 nm. The extracted CET is ~1.3 nm and ~1.5 nm for the devices with 0.8 nm and 1 nm EOT respectively.

Figure 4(a) shows the temperature dependent transfer characteristics in the measurement temperature range of 50 K to 300 K for the device with 0.8 nm EOT. As the temperature drops, the leakage floor reduces, and steeper portion of the I_d-V_g behavior is revealed. TAT in the device is not significant as the SS above the leakage floor is not a strong function of temperature. The corresponding extracted activation energy is plotted in Figure 4(b) as a function of V_g-V_{th}. Threshold voltage (V_{th}) was extracted from the transconductance derivative peak.[18] V_{th} correction is performed since the threshold voltage shifts as a function of measurement temperature as observed in Figure 4(a) due to factors like bandgap narrowing. Each point of the plot is obtained from the slope of the linear fit to $Ln(I_d)$ as a function of 1/kT as shown in the inset. As plotted in the inset for an example V_g point, two regimes are identified in the temperature dependent behavior with two different activation energies: The activation energy is low at the lower temperature range of 50–150 K while it is high at the higher temperature range of 200–300 K. It is believed that the lower temperature operation in the off-state is more dominant with a tunneling process (TAT and/or BTBT) at the opposite junction at the drain side (pTFET operation mode) and as the temperature increases, the Shockley-Read-Hall (SRH) process starts to contribute as well thereby increasing the activation energy.

Semi-classical simulations (with carefully calibrated BTBT models[19]) of the impact of EOT scaling on the SS behavior are plotted against experimental results in Figure 5. A reasonable agreement is observed between the experiment and predictions. Note that the simulations do not include mechanisms which limit the off-state current and as such, the SS will further reduce with the current.

Figure 6 is the benchmark of the DC sub-60 performance of the III–V based TFET devices reported so far (T = 300 K). For a proper benchmarking of the sub-60

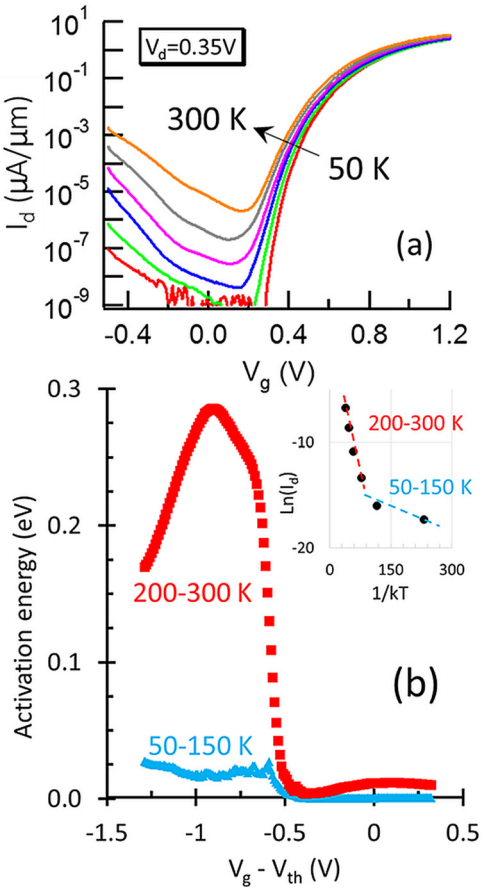

FIG. 4. (a) Temperature dependent transfer characteristic at temperatures from 50 K to 300 K in 50 K steps for the device with 0.8 nm EOT. As the temperature drops, the leakage floor reduces and the steeper portion of the I_d-V_g behavior is revealed. TAT in the device is not significant as the SS above the leakage floor is not a strong function of temperature. (b) Drain current activation energy extracted from the temperature dependent I_d-(V_g-V_{th}) behavior. Inset shows two regimes are identified in the temperature dependent behavior with two different activation energies. In the off-state, the activation energy is low at the lower temperature range of 50–150 K (tunneling dominant) while it is higher at the higher temperature range of 200–300 K (enhanced SRH contribution).

operating regime, we suggest a plot of the sub-60 operating current window versus the average SS over the whole sub-60 operating window. Since the sub-threshold behavior is not V_d dependent in the absence of Drain-Induced Barrier

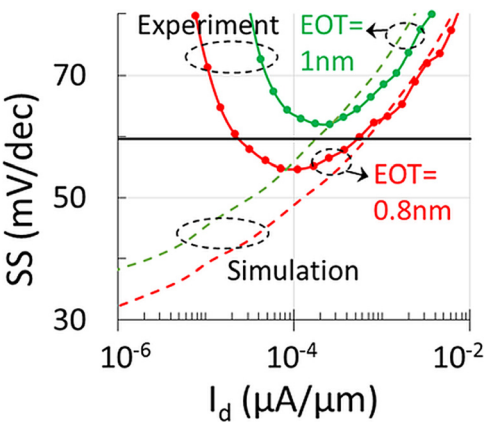

FIG. 5. Semi-classical simulation of the EOT impact on sub-threshold behavior. Simulations closely predict the observed experimental behavior when the EOT is scaled by 0.2 nm.

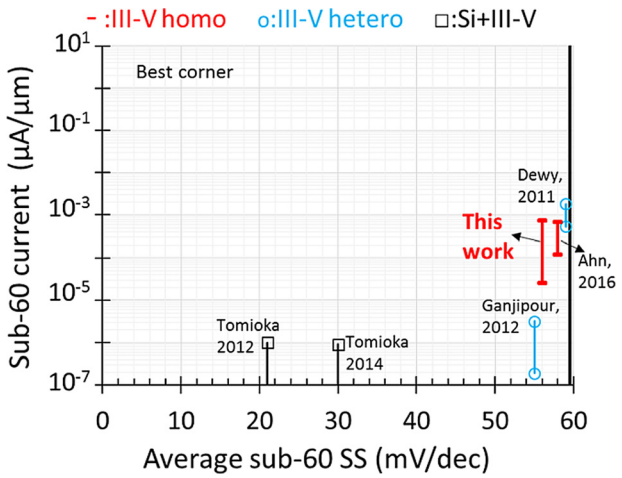

FIG. 6. Benchmark of the sub-60 performance including the sub-60 average SS and the sub-60 operating window. Plot of the sub-60 operating current window versus the average SS over the whole sub-60 operating window. Only III–V based devices are plotted.[7,9,13,14,20] The sub-threshold current of the TFET is not V_d dependent in the absence of DIBL, so the plots are for $V_d \leq 0.5$ V (where available) to be relevant for low power applications. The device of this work stays sub-60 over a current range of 30×.

Lowering (DIBL) and leakage floor interference, no V_d compensation would be needed. The data plotted on this benchmark figure are for $V_d \leq 0.5$ V (where available) to be relevant for low power applications where the supply voltage is limited. This work demonstrates the sub 60 mV/dec performance over a current range of 30× at an average sub-60 SS of 56 mV/dec.

Sub-60 mV/dec DC operation of an InGaAs homojunction planar TFET is demonstrated. The source of the device was formed by Zn diffusion from gas phase self-aligned to the gate which was found to be similar to the diffusion from spin-on dopants. The device has a sub-60 mV/dec performance over 1.5 decades of drain current with a point minimum SS of 54 mV/dec at 100 pA/μm. The enablers are believed to be the high quality III–V layers and the source junction realized by Zn diffusion as well as the EOT scaling keeping a high quality gate stack interface with the III–V channel.

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[1]D. H. Morris, K. Vaidyanathan, U. E. Avci, H. Liu, T. Karnik, and I. A. Young, "Enabling high-performance heterogeneous TFET/CMOS logic with novel circuits using TFET unidirectionality and low-VDD operation," in *2016 IEEE Symposium on VLSI Technology* (2016), p. 222.
[2]M. Noguchi, S. H. Kim, M. Yokoyama, O. Ichikawa, T. Osada, M. Hata, M. Takenaka, and S. Takagi, "High Ion /Ioff and low subthreshold slope planar-type InGaAs tunnel field effect transistors with Zn-diffused source junctions," J. Appl. Phys. **118**, 045712 (2015).
[3]A. Alian, J. Franco, A. Vandooren, Y. Mols, A. Verhulst, S. El Kazzi, R. Rooyackers, D. Verreck, Q. Smets, A. Mocuta, N. Collaert, D. Lin, and A. Thean, "Record performance InGaAs homo-junction TFET with superior SS reliability over MOSFET," Tech. Dig. - Int. Electron Devices Meet. **2015**, 31.7.1–31.7.4.
[4]R. Pandey, H. Madan, H. Liu, V. Chobpattana, M. Barth, B. Rajamohanan, M. J. Hollander, T. Clark, K. Wang, J.-H. Kim, D. Gundlach, K. P. Cheung, J. Suehle, R. Engel-Herbert, S. Stemmer, and S. Datta, "Demonstration of p-type $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ and n-type $GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ complimentary heterojunction vertical tunnel FETs for ultra-low power logic," in *2015 Symposium on VLSI Technology (VLSI Technology)* (2005), p. T206.
[5]E. Lind, E. Memisevic, A. W. Dey, and L.-E. Wernersson, "IIIV heterostructure nanowire tunnel FETs," IEEE J. Electron Devices Soc. **3**, 96 (2015).
[6]D. K. Mohata, R. Bijesh, Y. Zhu, M. K. Hudait, R. Southwick, Z. Chbili, D. Gundlach, J. Suehle, J. M. Fastenau, D. Loubychev, A. K. Liu, T. S. Mayer, V. Narayanan, and S. Datta, "Demonstration of improved heteroepitaxy, scaled gate stack and reduced interface states enabling heterojunction tunnel FETs with high drive current and high on-off ratio," 2012 Symposium on VLSI Technology (VLSIT) (2012), p. 53.
[7]G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H. W. Then, and R. Chau, "Fabrication, characterization, and physics of III–V heterojunction tunneling field effect transistors (H-TFET) for steep sub-threshold swing," Tech. Dig. - Int. Electron Devices. Meet. **2011**, 33.6.1–33.6.4.
[8]X. Zhao, A. Vardi, and J. A. del Alamo, "InGaAs/InAs heterojunction vertical nanowire tunnel FETs fabricated by a top-down approach," Tech. Dig. - Int. Electron Devices. Meet. **2014**, 25.5.1–25.5.4.
[9]K. Tomioka, M. Yoshimura, and T. Fukui, "Steep-slope tunnel field-effect transistors using III–V nanowire/Si heterojunction," 2012 Symposium on VLSI Technology (VLSIT) (2012), p. 47.
[10]G. Zhou, R. Li, T. Vasen, M. Qi, S. Chae, Y. Lu, Q. Zhang, H. Zhu, J.-M. Kuo, T. Kosel, M. Wistey, P. Fay, A. Seabaugh, and H. Xing, "Novel gate-recessed vertical InAs/GaSb TFETs with record high ION of 180 μA/μm at Vds = 0.5 V," Tech. Dig. - Int. Electron Devices. Meet. **2012**, 32.6.1–32.6.4.
[11]R. Bijesh, H. Liu, H. Madan, D. Mohata, W. Li, N. V. Nguyen, D. Gundlach, C. A. Richter, J. Maier, K. Wang, T. Clarke, J. M. Fastenau, D. Loubychev, W. K. Liu, V. Narayanan, and S. Datta, "Demonstration of $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ near broken-gap tunnel FET with ION = 740 μA/μm, GM = 700 μS/μm and gigahertz switching performance at Vds = 0.5 V," Tech. Dig. - Int. Electron Devices. Meet. **2013**, 28.2.1–28.2.4.
[12]H. Zhao, Y. Chen, Y. Wang, F. Zhou, F. Xue, and J. Lee, "InGaAs tunneling field-effect-transistors with atomic-layer-deposited gate oxides," IEEE Trans. Electron Devices **58**, 2990 (2011).
[13]D. H. Ahn, S. M. Ji, M. Takenaka, and S. Takagi, "Performance improvement of $In_xGa_{1-x}As$ tunnel FETs with quantum well and EOT scaling," in *2016 IEEE Symposium on VLSI Technology* (2016), p. 224.
[14]B. Ganjipour, J. Wallentin, M. T. Borgström, L. Samuelson, and C. Thelander, "Tunnel field-effect transistors based on InP-GaAs heterostructure nanowires," ACS Nano **6**(4), 3109 (2012).
[15]A. Alian, G. Brammertz, R. Degraeve, M. Cho, C. Merckling, D. Lin, W.-E. Wang, M. Caymax, M. Meuris, K. De Meyer, and M. Heyns, "Oxide trapping in the InGaAs-Al_2O_3 system and the role of sulfur in reducing the Al_2O_3 trap density," IEEE Electron Device Lett. **33**, 1544 (2012).
[16]S. Agarwal and E. Yablonovitch, "Band-edge steepness obtained from Esaki/backward diode current-voltage characteristics," IEEE Trans. Electron Devices **61**(5), 1488 (2014).
[17]R. M. Iutzi and E. A. Fitzgerald, "Conductance slope and curvature coefficient of InGaAs/GaAsSb heterojunctions at varying band alignments and its implication on digital and analog applications," J. Appl. Phys. **118**, 235702 (2015).
[18]K. Boucart and A. M. Ionescu, "Threshold voltage in Tunnel FETs: Physical definition, extraction, scaling and impact on IC design," in *ESSDERC* 2007, p. 299.
[19]Q. Smets, D. Verreck, A. S. Verhulst, R. Rooyackers, C. Merckling, M. Van De Put, E. Simoen, W. Vandervorst, N. Collaert, V. Y. Thean, B. Soree, G. Groeseneken, and M. M. Heyns, "InGaAs tunnel diodes for the calibration of semi-classical and quantum mechanical band-to-band tunneling models," J. Appl. Phys. **115**, 184503 (2014).
[20]K. Tomioka and T. Fukui, "Current increment of tunnel field-effect transistor using InGaAs nanowire/Si heterojunction by scaling of channel length," Appl. Phys. Lett. **104**, 073507 (2014).