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Short communication

Memristive behavior of the SnO_2/TiO_2 interface deposited by sol–gel

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ABSTRACT

A novel and cheap Resistive Random Access Memory (RRAM) device is proposed within this work, based on the interface between antimony doped Tin Oxide (4%at Sb:SnO_2) and Titanium Oxide (TiO_2) thin films, entirely prepared through a low-temperature sol–gel process. The device was fabricated on glass slides using evaporated aluminum electrodes. Typical bipolar memristive behavior under cyclic voltage sweeping and square wave voltages, with well-defined high and low resistance states (HRS and LRS), and set and reset voltages are shown in our samples. The switching mechanism, explained by charges trapping/de-trapping by defects in the SnO_2/TiO_2 interface, is mainly driven by the external electric field. The calculated on/off ratio was about 8×10^2 in best conditions with good reproducibility over repeated measurement cycles under cyclic voltammetry and about 10^2 under applied square wave voltage.

1. Introduction

An impressive part of the modern research in the field of advanced electronics, is nowadays focused on the study and the application of memristors (memory resistors), a novel type of memory storage device. The memristor (MR) became a part of the circuit's theory in 1971 [1] fulfilling the mathematical relationship between the charge (Q) and the current flux ($J_{(Q)}$). However, the MR remained just a theoretical object until its discovery in 2008 by Hewlett Packard (HP) laboratories [2]. Basically, a MR is a two-terminal element capable of changing its resistance as a function of the flowing charge Q. This special feature makes MR very interesting for several electronics applications such as: unconventional computing, logic and analogic operations [3,4], neural networks and patterns recognition [5]. Resistive random-access memory (RRAM) belongs to memristor's family and it is basically a device with a switchable resistance by rapid voltage pulses (subnanosecond) [6]. A special attention from academic community is being given to this device, as shown by the increase in the number of publications per year and significant progress over the past decade, in order to understand the switching mechanisms behind RRAMs [7,8]. One of the most discussed issues are the improvement of the switching features such as the on/off resistances ratio, the operation speed, and extreme endurance (>10^{12} cycles) in metal oxides [9].

In a typical configuration, a MR consists of a sandwich structure based on thin layers of a semiconducting or insulating material (e.g. TiO_2) with specific charge-transport characteristics between two electrodes. The first model presented a thin layer of doped TiO_{2-x} grown on undoped TiO_2 [2], showing a memristive hysteresis behavior under application of an external voltage bias. To understand the carrier type-dependent switching kinetics, much attention has been paid by the academic community to NiO_x and TiO_x, p and n-type semiconductors, respectively [7]. The combination of both ionic and electronic solid-state transport phenomena lead to a reproducible resistance-switch [2]. The semiconducting layers for MRs, also called the storage layer, can be fabricated by several methods [7], mainly including atomic layer deposition (ALD) [10], pulsed laser deposition (PLD) [11], magnetron sputtering [12], thermal and plasma oxidation [13,14], and sol–gel chemical route [15]. Sol–gel is a chemical wet deposition method which requires considerably less technology and is potentially less expensive in comparison with the above cited techniques. It is suitable for the fabrication of thin oxide layers such as TiO_2 [16] and SnO_2 [17–20], as previous reports. The interest in using transition metal oxides (i.e. TiO_2, SnO_2, ZrO_2, ZnO) is due to their structural simplicity, low power consumption, fast switching and high integration density [7]. In respect to the electronic potential barrier (Schottky barrier), the work function of the metal electrode has shown no strong effect at the interface with TiO_2 [21].

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However, the defects generated by metal deposition and the oxygen vacancies from the oxide govern the electronic barrier at the metal-semiconductor interface [22]. In order to optimize the performance of RRAMs, doping [23], electrode [24] and interface [25] engineering have been reported. Inorganic RRAMs operating as storage media have a remarkable advantage over organics ones in switching stability, while organic RRAMs have advantage in high-mechanical stability, simple fabrication, and low cost [7].

Within this work we propose an inorganic low-cost RRAM based on Sb:SnO_2 and TiO_2 layers deposited by sol–gel. The storage layer grown by sol–gel, creates films with nanocrystalline grains of Rutile SnO_2 and Anatase TiO_2 on the substrate, both intrinsic n-type semiconductors due to their oxygen vacancies and interstitial atoms [26,27], which may contribute to smaller grains that are usually responsible for the creation of electronic barriers within the grain boundaries [21,22]. These material have comparable electronic bandgap energies (E_G = 3.5–4 eV), but optical and electronic properties quite different. TiO_2 shows an optical absorption tendency with weak electronic mobility due to electrons and holes trapping, while SnO_2 is typically an optical-transparent oxide with high electronic conductivity [28].

2. Materials and methods

Sol–gel fabrication of TiO_2 was carried out by hydrolysis and condensation of titanium (IV) isopropoxide alkoxide using a high molar ratio of water:alkoxide (200:1), isopropanol as co-solvent, HNO_3 as catalyst, and Triton X-100 as surfactant [29] (more details in Supplementary Information (SI)). Colloidal suspension of 4 at% Sb:SnO_2 was obtained through an aqueous solution of Sn^{4+} (0.5 mol/l) obtained by dissolution of $SnCl_4{\cdot}5H_2O$ in deionized water mixed to a solution of Sb obtained by dissolution of SbF_3 in deionized water. Hydrolysis of Sn^{4+} and Sb^{5+} ions were promoted by addition of NH_4OH. The suspension was submitted to dialysis against distilled water for elimination of chloride and fluoride ions [17,19].

Aluminum electrode was deposited on clean substrates (see SI) by resistive evaporation at 10^{-3} Pa. A TiO_2 layer was then spin-coated on the as-evaporated Al contact at speed of 2000 rpm for 60 s, using the previous described solution, followed by layer calcination at 80 °C for 10 min. Sb:SnO_2 layer was then deposited following the same spin-coating procedure. A final thermal annealing was performed at 400 °C for 2 h. To finish the device assembling, the top electrode of Al was evaporated. A diagram of the device is shown in Fig. 1a. X-Ray diffraction and UV–vis spectroscopy were collected on the films deposited individually on glass in order to investigate their structure and crystallite size, and bandgap, respectively (details in SI), while the Sb:SnO_2 film morphology and thickness of the Sb:SnO_2/TiO_2 layer were investigated through confocal microscopy. Current *vs* voltage curves, such as Cyclic voltammetry was performed from +5.0 to −5.0 V at 100 mV/s, which results in a frequency of 5 mHz, and square wave voltages from +5.0 to −5.0 V and reading voltage of −0.5 V (details in SI).

3. Results

The indirect bandgap calculated (Fig. S1) for the TiO_2 was about 3.5 eV, and the direct one for Sb:SnO_2 was 4.2 eV. Sb:SnO_2 deposited by sol-gel has presented rutile nanocrystals [19,20], also found here by XRD (Fig. S2). The TiO_2 film presents nanocrystallites of anatase phase (Fig. S2). In both cases the nanocrystallites present sizes of the order of 7 nm [19]. These intrinsic crystal defects lead to conventional bipolar switching behavior, found in our samples, explained by trap controlled space charge limited current (SCLC) [7].

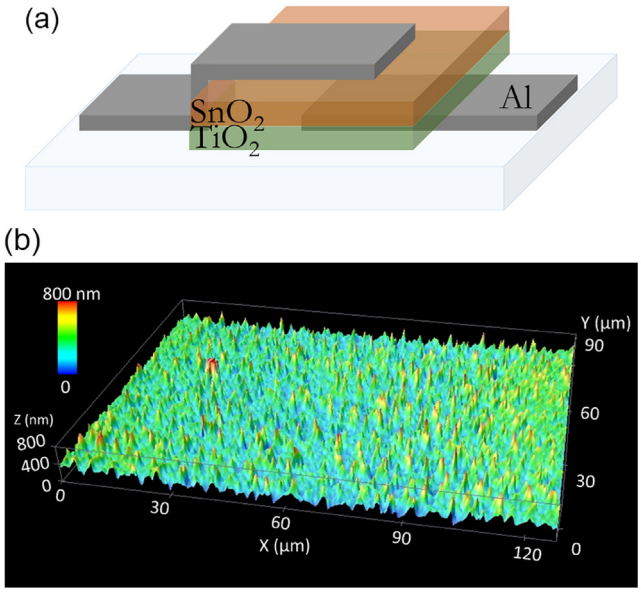

Fig. 1. (a) Device configuration diagram, with top Al/Sb:SnO_2/TiO_2/Al (bottom)/substrate. (b) Confocal Microscopy, topographic mode, of the SnO_2 surface, before Al top electrode deposition.

The Confocal Microscopy image of the SnO_2 surface, Figs. S3a and 1b, presents root mean square (rms) of 108 nm, which represents a considerable roughness on the surface, that may contribute with the generation of defects in the SnO_2/Al interface. Confocal image of the border of the two oxide layers interfacing the Al bottom electrode, shows the thickness of the storage layer is about 460 nm (Fig. S3a and b). The relative thick layer obtained is related to the sol–gel viscosity and spin-coating speed, that affects largely the memory switching speed, where a thinner layer is favorable to a higher frequency of operation [24].

Fig. 2a shows the reversible current response of the Sb:SnO_2/TiO_2 as storage layer on RRAMs over 5 successive cycles. In order to understand the state-transitions between two voltage values (+5 V and −5 V), a triangular wave function (ramp) has been considered for this measurement. Current flowing through the device retraces almost the same pattern exhibited in the previous cycle, which confirms a completely reversible behavior. In Fig. 2a, with absolute values of current, a typical butterfly-shaped plot is obtained, confirming the memristive feature of the device. This can be confirmed considering the "pinched" shape of the current/voltage plot, a sufficient and necessary condition to recognize a device as a memristor [30]. In fact, one can notice that, reading current at a fixed voltage (V_{READ}), it shows different values depending on the position, in the cycle, of the applied voltage. The different current is due to the high resistance state (HRS) and a low resistance state (LRS), which presents low and high current, respectively. Such resistance states are induced by voltage sweep crossing specific values: V_{SET} (−3.0 V), which sets the device into LRS, and V_{RESET} (+1.5 V), which sets it into HRS. The average ratio (on/off) of the current's values in LRS and HRS was 8.3×10^2, at V_{READ} = −0.2 V. The device showed bipolar switching, with negative V_{SET} and positive V_{RESET}, showing non-linear characteristics (non-ohmic behavior) in LRS, typical phenomenon where the electric field rules the device's current [21].

Process (I) in Fig. 2a shows the threshold voltage (V_T = −3.0 V), below which the device is in HRS or off-state. Process (II) shows the device setting, $|V_{SET}| > |V_T|$, where the resistance switches to LRS. Within this process, the information (resistance value) is stored into the device [7,24]. The reading operation (process III) occurs at V_{READ} = −0.2 V. In process IV the device remains in LRS at positive

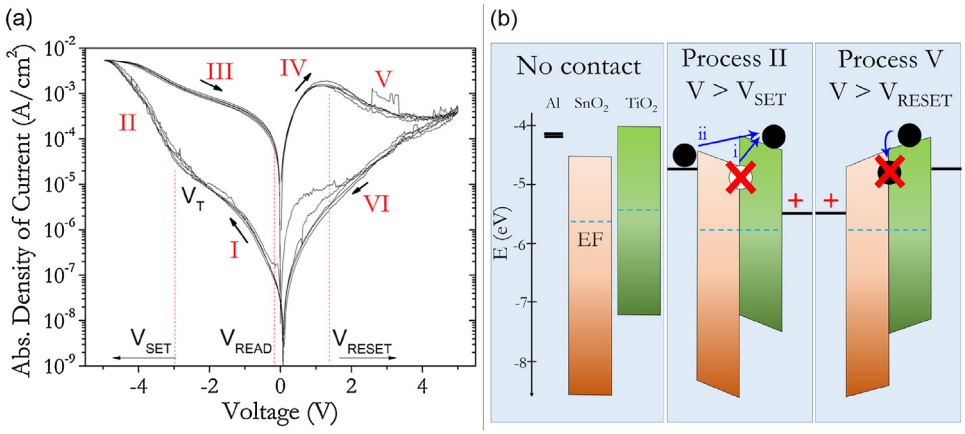

Fig. 2. (a) Absolute logarithm of current density *vs* V curves for the Al/Sb:SnO_2/TiO_2/Al memristor. Black arrows show the order of the current as function of the voltage applied, with forward bias applied on the top electrode. (b) Schematic energy diagram of the semiconductors interface, and the charge trapping and de-trapping processes. In process II occurs the i) de-trapping by Poole-Frenkel field induced emission, and ii) Fowler-Nordheim emission (from the cathode). In Process V the trap-states are filled by electrons incoming from the cathode by tunneling.

bias, and current increases linearly with voltage for values below V_{RESET}, which marks the onset of the reset transition. The resistance starts to increase, leading to a current drop (process V), probably due to the increase of depletion region in the channel [31]. Furthermore, the oxygen vacancies as well as the interfacial defects that accommodate traps for electrons emitted from the cathode, are involved in the reset process [22]. Process (VI) shows the device in HRS. Now, reading the information at V_{READ}, one can notice that the current shows a lower value with respect to that shown in LRS.

The forward bias is applied at the top electrode, in contact with Sb:SnO_2. A higher current is found when reversed biased, showing a slightly rectification behavior (Fig. S4), due to the heterojunction n^+-n with the TiO_2. Multilevel of traps may be found in this device, such as: internal layer traps, semiconductors interfacial traps, and traps at the semiconductor-metal (Al) interfaces. The rectifying phenomena appear at these last interfaces when there are Schottky barrier [7].

Both oxide layers are composed by nanocrystallites, presenting defects such as oxygen vacancies, mainly at the interface between them. Interfacial oxygen vacancies probably contribute to cation interlayer diffusion. Besides the ionic contribution, electrons trapped in the multiple defects are predominant carrier charge in the conduction mechanism and switching effect. The defects act as reservoir of carriers, which causes the switching to occur at the interface with less oxygen vacancies [22]. The combination of both ionic and electronic carrier charge transport results in a reproducible resistance-switch [2]

Looking at the transition to LRS (regions I–II in Fig. 2a), one can see that the initial I *vs* V characteristic of the HRS follows a linear ($I \propto V$) behavior at low voltage (process I), followed by a quadratic term at higher voltage ($I \propto V^2$), which is typical of an insulator with shallow traps [7], process II in Fig. 2b. With increasing electric field, the injected electrons are pushed toward the conduction band by both Poole-Frenkel field induced emission, tunneling from traps, and Fowler-Nordheim emission (from cathode) [21], illustrated in processes i and ii in Fig. 2b, respectively. This de-trapping processes are probably responsible for HRS/LRS transition [22]. Electrons drawn from multilevel traps (Schottky and semiconductor interfaces) leave positive charged ions working as traps. Such effect provides an additional electric field into the oxides layer which reduces the build-in potential and the depletion width, creating a conduction path through the channel [7,22,32], setting the junction to LRS, as shown in process II in Fig. 2a and b.

With positive voltage sweep (Fig. 2a IV–V), electrons start tunneling into the Schottky barrier (metal/semiconductor), establishing a space-charge field, opposite to the applied electric field, thus reducing the flowing current [7]. This produces a negative derived resistance region in Fig. 2a (region V). Another possible mechanism involves electrons filling trap states within the semiconductors and their interface, process V in Fig. 2b, resulting in neutral-charged occupied trap states [22]. These trapping mechanisms cause the degradation of the conducting filaments in the channel, resetting the heterojunction back into the HRS, where the barriers recover their original state [7].

Different charge states of Sb centers of Sb:SnO_2 could have an important role in the switching mechanism of the device. As reported by Geraldo and collaborators [26], Sb^{5+} gives rise to oxygen vacancies, that may generate more defects into the lattice and these defects allow more ionic diffusion. Such effects are noticeable by varying the scan rate. As reported in S.I. one can notice that the intensity of the anodic peak at 1.5 V of Fig. S5a (and Fig. 2a) decreases at higher scan rates. This suggests a possible ionic contribution driven by diffusion through the film.

In order to verify the device under operation at square waves, the V_{SET} of −5 V, V_{RESET} of +5 V, and V_{READ} = −0.5 V were applied at a frequency of 40 mHz. The set and reset voltages were higher than obtained from Fig. 2a in order to ensure the on/off switching. The result of 40 reproducible cycles is shown in Fig. S6. Fig. 3 presents only 3 cycles for better conception. The on-state occurs at (3.4 ± 1.2) x10^{-5} A and the off-state at $(3.9 \pm 1.1) \times 10^{-7}$ A, which produces an on/off ratio of about 9×10^1. Despite the low frequency, the device shows promising memristive characteristics that should be improved by optimizing thickness, doping level, or even the electrode of the devices.

4. Conclusion

We hereby propose a two dimensional Sb:SnO_2/TiO_2 interface as active layer of bipolar memristors, deposited by cost-effective sol–gel route. This binary oxide heterojunction working as storage layer operates as bipolar switching, related to the asymmetry in the interfaces, resulting in a repeatable switching behavior, with well-defined switching polarity. The as-built devices have shown switching at low operating voltages ($V_{RESET} \sim 1.5$ V and $V_{SET} \sim -3.0$ V), as well as a high switching resistance ratio of about 8×10^2. This switching mechanism could be explained by charges trapping/de-trapping in the multiple defects in the interfaces of the device, ruled mainly by the build-in and applied electric fields. Considering the low cost of the sol–gel method and the encouraging results, this memristor layout should be considered for a more

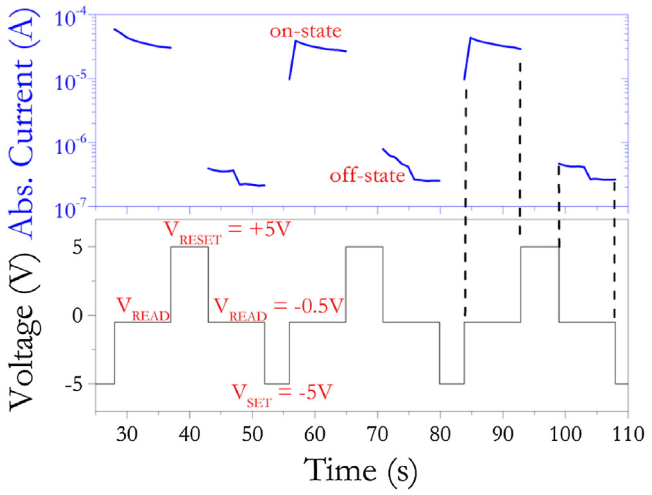

Fig. 3. Applied square wave voltage and corresponding output current as function of time. Only 3 out of 40 cycles of operation of the Sb:SnO_2/TiO_2-based memristors are presented for better conception. V_{SET} and V_{RESET} occur at −5 and +5 V, respectively, and V_{READ} occurs at −0.5 V. In Fig. S6 is presented all the 40 cycles, that shows the reproducibility of the data.

in-depth study focused on its optimization. Particularly the whole thickness of the device should be reduced and optimized to increase its switching frequency. Furthermore, the effects of ionic diffusion should be studied as a function of the thickness.

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Appendix A. Supplementary data

Supplementary data associated with this article can be found, in the online version, at http://dx.doi.org/10.1016/j.apsusc.2017.03.132.

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