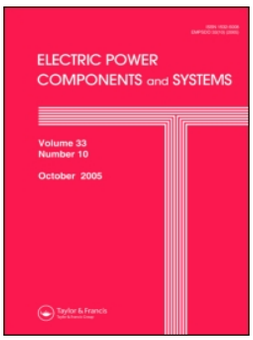

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Selective Sharing of Load Current Components Among Parallel Power Electronic Interfaces in Three-phase Four-wire Stand-alone Microgrid

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CONTENTS

Abstract—This paper investigates selective sharing of load current components among the parallel operation of distributed generators (DGs) in three-phase four-wire stand-alone microgrids. The proposed control method is based on master-slave operation of DGs, and the goal of selective sharing of load current components is to have DGs located in close proximity of the load operating in slave mode, in order to inject their available energy and also compensate the non-active load current components, while the distant DGs might operate in master mode to share the remaining load autonomously. Droop control is employed due to impracticality of communication at remote nodes, and resistive line impedance compensation is adopted to decouple active and reactive power controllers and ensure proper active power sharing among master DGs, irrespective of the mitigation of non-active current components by the slave inverters. The sharing factors for each current component are determined by a higher level control. The Conservative Power Theory (CPT) decompositions provide decoupled power and current references for the inverters, resulting in a selective sharing strategy. The principles supporting the developed control strategy are discussed, and the effectiveness of the control is demonstrated through computational simulations using PSIM software.

Keywords: active power filter, conservative power theory, distributed generation, four-leg inverter, load current sharing, microgrids, power quality improvement

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1. INTRODUCTION

The microgrid, a local AC network, with advantages such as flexibility, reliability, and high power quality is considered as a cluster of distributed generation (DG) resources, connected through power electronics interface (PEI) with energy storage capabilities to feed distributed loads in both grid-connected and islanded modes [1–5]. In such systems, due to the presence of linear and non-linear single-phase and three-phase loads, distorted and unbalanced voltages and currents may appear, possibly leading to harmful operating conditions,

which should be rapidly detected and resolved, in order to avoid, for example, efficiency and performance deterioration, equipment life-time reduction, control instabilities, inappropriate protection operation, and interference problems [6, 7].

In this sense, the use of intelligent interface converters connecting the DGs and the local grid is mandatory. Usually, these PEIs have a final stage consisting of voltage source inverters (VSIs), which can be either current-controlled for grid-following mode or voltage-controlled in grid-forming operation [8]. In the stand-alone operation, while any load step generally affects the voltage magnitudes at the load buses [9], highly non-linear and unbalanced loads cause distortion and imbalance on the load voltage [10]. Moreover, considering that PEIs have unequal capabilities of generating different power components [11, 12], a selective sharing strategy is required to enable the control of each current component, independently, and meet the desired operating criteria for the microgrid, such as load demands, voltage support and reactive, harmonics and unbalance compensation, while ensuring efficient utilization of PEIs.

Several methods for DGs power control have been proposed, which can be mainly classified as two types: communication-based [13–18] and non-communication-based [17–19] control strategies.

Power sharing strategies based on communication include concentrated control, master-slave control, and distributed control [13, 17, 18]. In the concentrated control technique, common synchronization signals and current-sharing modules are required [18]. The PLL circuit of each module ensures the consistency between the frequency and phase of the output voltage and the synchronization signal. Besides, the current-sharing modules observe the total load and each module tracks the average current to achieve equal current distribution. This method directly adds current error to each inverter unit as a compensation component of the voltage reference in order to eliminate the differences among their output currents [18]. However, this control scheme must include a centralized controller, which can limit the system's expandability. Moreover, there is the possibility of being compromised with single-point faults. The distributed control, also represented as the instantaneous average current-sharing control, has no central control board and every module is symmetric [14, 18]. Further, average current-sharing requires a current-sharing bus and reference synchronization for the voltage. An additional current-control loop is used to enforce each converter to track the same average reference current, provided by the current-sharing bus. When a fault happens in any module, it can smoothly disconnect from the microgrid, and the rest of modules can still operate in parallel. In the master/slave control, master module regulates the output voltage and specifies the current reference for the rest of slave modules. Then, slave units track the current reference provided by the master in order to achieve equal current distribution. Based on this scheme, inverters do not need any PLL for synchronization, since these units communicate to the master units [15, 16, 18].

In case of short distances, it is reasonable to use a communication link among DG inverters with potential improvement in controllability and dynamic response and, consequently, in PCC voltage regulation and proper power sharing [18, 20]. Moreover, in contrast to non-communication-based strategies, the output voltage amplitude and frequency are generally close to their ratings without using a secondary control [18]. However, there are some drawbacks in communication-based approach, such as the requirement for high-bandwidth communication links, which can be an unfeasible and costly solution for microgrids with long distances among the inverters. Long-distance communication lines get interfered easier, thereby reducing system reliability and expandability [18].

On the other hand, the control strategies without communication are generally based on the droop concept [18, 19], relies on the ability of individual DGs to adjust the output voltage and frequency without any communication, while sharing the active and reactive power demands; thereby enhancing the reliability of the system. In [21], each DG unit of a microgrid is controlled as a negative-sequence conductance to compensate for the voltage unbalance. In such approach, compensation is done by generating a reference for negative-sequence conductance based on the negative-sequence reactive power in the synchronous reference frame. Then, this conductance is applied to generate the compensation current reference, injected at the output of the voltage control loop. However, such compensation will be considered a disturbance to be rejected by the voltage control loop. In other words, there is a trade-off between the unbalance compensation efficiency and voltage regulation. To cope with this problem, [22] proposes the direct change of the voltage reference to compensate for voltage unbalance in a microgrid. This way, the compensation reference is considered as a command followed by the voltage controller.

In [23] resistive-capacitive virtual impedances have been presented for LCL-terminated voltage source inverters in order to provide proper sharing for all current components, except for the fundamental positive sequence, and to compensate LCL filter output voltage distortion. In such a case, output voltage distortion is mitigated by inserting capacitive virtual impedance for negative sequence of fundamental component as well as positive and negative sequences of main harmonic components. The capacitive impedance presented

in [23] has a fixed value and is realized by a negative inductance equal to the output inductor of LCL filter of interface inverters. This way, the voltage quality after the LCL filter is improved. However, enhancement of filter output voltage quality is achieved at the price of increasing the voltage distortion at filter capacitance. Furthermore, for a proper load sharing, resistive virtual impedances are added, which leads to output voltage distortion as a result of voltage drop on the virtual resistances. The quality of LCL filter output voltage is important since the sensitive loads may be installed at or near to LCL filter terminal. However, if the Sensitive Load Bus (SLB) is located far from the LCL filter output, the quality of SLB can degrade since its voltage is not controlled in [23]. In [24], a hierarchical control scheme is proposed for the enhancement of SLB voltage quality in microgrids. The primary control level comprises DGs local controllers; each of them includes a selective virtual impedance loop, which is considered to improve sharing of fundamental and harmonic components of load current among the microgrid. The sharing improvement is achieved at the expense of distorting DGs' output voltage as a result of voltage drop on the virtual resistances. Thus, for selection of virtual resistance values, a tradeoff should be considered between the output voltage distortion and power sharing. Therefore, the secondary control level is applied to control the selective compensation of SLB voltage unbalance and harmonics by sending proper control signals to the primary level. After activating selective compensation, SLB voltage quality is improved. However, the improvement is achieved at the expense of voltage distortion increase at DGs terminals. Thus, considering the required power quality, possible practical limitations still remain. In [23, 24], the fundamental positive sequence component of the load current is shared by droop controllers and the resistive-inductive virtual impedance is considered to enhance the droop performance. In such a case, the inductive part makes the system impedance inductive enough to have decoupled active and reactive power and the resistive part increases the system damping.

Therefore, communication links should be always an enhanced technical solution, since they have the potential to provide better controllability and better load sharing response [20]. Therefore, a current-sharing scheme should be developed so that the potential of each DG could be exploited at most. Thus, this paper proposes that DGs located close to the load should operate as slave inverters, in order to inject their available energy and to provide rapid load sharing for non-active current compensation, while feeding the remaining load autonomously using distant DGs through droop control.

Consequently, the contributions of this paper can be summarized as follows: First, in the proposed master-slave control strategy, it has been assumed that DGs may have different rated powers; thus, the compensation effort of each DG unit is controlled to be proportional to its rated power. The sharing effort is controlled locally by a supervisory control, on which the non-active current references for each slave inverter are synthesized from the load current based on the CPT decompositions. This is different from conventional master-slave control strategies, on which slave units track the current reference provided by the master, in order to achieve equal current distribution [18]. Second, droop control method and resistive line impedance compensation is adopted to decouple active and reactive power controllers and ensure proper active power sharing among master PEIs. Third, the enhancement of voltage unbalance and harmonic levels and also compensation of fundamental positive sequence of voltage to the value near the rating at master PEIs terminal and load bus are achieved simultaneously as a result of the non-active load current mitigation by the slave PEIs. Fourth, the slave PEIs do not require PLL circuits for the synchronized operation, providing a means for easy expansion of this type of parallel-connected Inverters. Fifth, four-leg PEI is implemented for connecting renewable energy sources such as solar, wind, and others to the microgrids for active power provision and non-active compensation, with the capability of supplying, selectively, the single-phase loads through its fourth leg.

2. STAND-ALONE MICROGRID ARCHITECTURE

Figure 1 shows the proposed master-slave-based islanded microgrid. It illustrates the control strategy of the master and slave DGs. The DGs are properly controlled to simultaneously compensate for voltage unbalance and distortion, while sharing the compensation effort and also active and reactive powers. The master PEI is controlled as a voltage source to establish the load voltage and, autonomously, to share load current components with the current-controlled or slave PEIs. The active and reactive power droop controllers are developed based on the predominantly inductive line impedance. However, the accuracy of the power sharing provided by the droop controllers is affected by the distribution lines, leading to coupling between P and Q [18, 25]. To deal with this problem, various methods such as voltage active power droop and frequency reactive power boost (VPD/FQB) droop control, complex-line impedance-based droop control, resistive-inductive virtual impedance method, and virtual frame transformation method have been introduced [18]. In this paper, compensation of resistive line impedance is

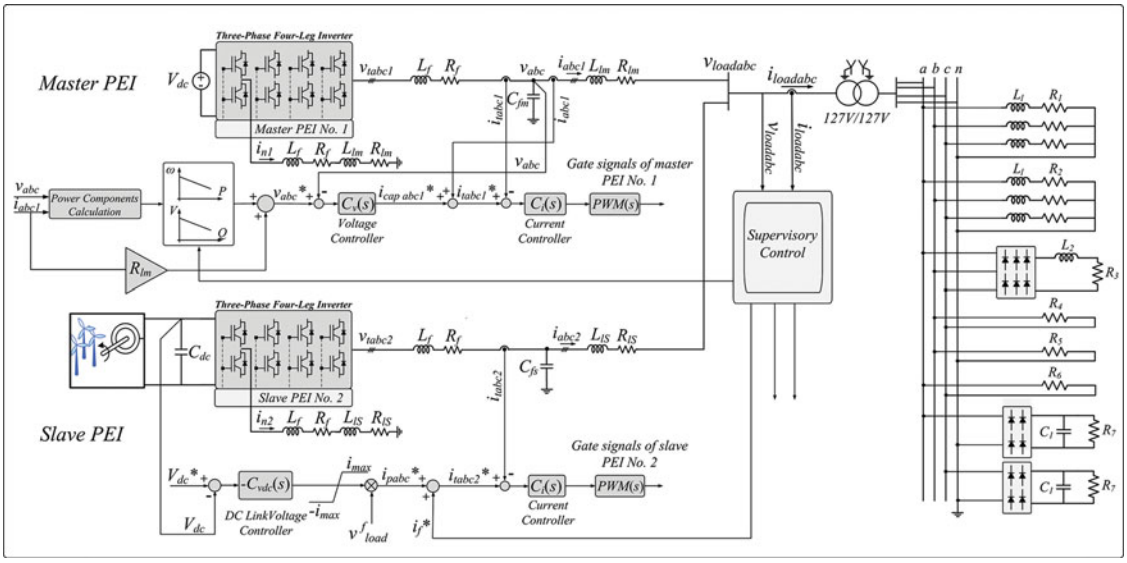

FIGURE 1. Diagram of the proposed master-slave-based stand-alone microgrid.

implemented to decouple P and Q by a current feedback loop, which adds the resistive voltage drop on distribution line to the reference voltage. The gain of this feedback loop is equal to the resistive impedance of the line causing to have decoupled active and reactive power controllers and proper active power sharing among DGs.

Each PEI consists of a four-leg VSI with a three- phase *LC* filter, connected to the network load via different line impedances. The inductance and capacitance of the output filter are L_f and C_f, respectively, and R_f models the ohmic loss of the inductor. L_{lm}, L_{ls}, R_{lm}, and R_{ls} represent the inductance and resistance of the master and slave distribution lines, respectively. For the master PEI, the effect of the primary energy source is represented by a DC voltage source, connected in parallel with the VSI DC link capacitor. For the slave PEI, the effect of the local power source is modeled as a DC current source, I_{dc} connected in parallel with the VSI DC link capacitor C_{dc}. The local power source could be a photovoltaic array, a fuel cell, or a wind generator. The parameters of the microgrid system and network load are provided in Tables 1 and 2, respectively. The network contains balanced and unbalanced linear and non-linear loads, isolated from the rest of the microgrids using an isolating transformer Y–Y connection with grounded neutral.

Nominal load pick phase voltage, v_{load}	180 V
Grid frequency, f	60 Hz
Maximum power output of inverters	5 kVA
Switching frequency, f_s	18 kHZ
Output filter inductor, L_f	3 mH
Output filter resistor, R_f	0.1 Ω
Output filter capacitor of Masters, C_{fm}	15 µF
Output filter capacitor of Slaves, C_{fs}	1 µF
Line inductor, L_{lm}	1.5 mH
Line resistor, R_{lm}	1.5 Ω
Line inductor, L_{ls}	1 mH
Line resistor, R_{ls}	1 Ω
DC link voltage reference, V_{DC}	450 V
DC link capacitor, C_{dc}	1 mF
Carrier amplitude voltage, v_{tri}	5 V

TABLE 1. Microgrid parameters

Load inductor, L_1	50 mH
Load inductor, L_2	4 mH
Load capacitor, C_1	220 µF
Output resistor, R_1	50 Ω
Output resistor, R_2	70 Ω
Output resistor, R_3	30 Ω
Output resistor, R_4	40 Ω
Output resistor, R_5	50 Ω
Load resistor, R_6	35 Ω
Load resistor, R_7	25 Ω

TABLE 2. Load parameters

3. MODELING OF THE SLAVE DGS

In this section, the current-controlled slave four-leg PEIs are designed. The control system of such inverters consists of two feedback control loops. The first is a fast loop, which controls the output current [26, 27] and the other is a slower loop, which regulates the DC link voltage [28]. The DC link keeps the power balance between the power that is delivered to the

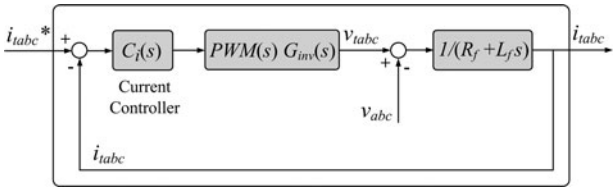

FIGURE 2. Block diagram of the current-control scheme.

system and the power in the DC link. A robust current-control scheme is devised with a fast dynamic response, showing that i_{ta}, i_{tb}, i_{tc}, and i_n can rapidly track their respective reference commands i_{taref}, i_{tbref}, i_{tcref}, and i_{nref}. It should be pointed out that i_{nref} is determined as $i_{nref} = -(i_{taref} + i_{tbref} + i_{tcref})$. Figure 2 presents a closed-loop control structure to regulate inverter output current. The open-loop transfer function of the current-controlled scheme $G_{oi}(s)$ is obtained as in Eq. (1), where $C_i(s)$ is the controller of the current-control scheme. The proposed current controller in the *abc* frame must have large bandwidth and high gain at the relevant harmonic frequencies. This can be achieved using resonant controllers, since a PI controller would not be able to provide a high gain at high frequencies. The current controller $C_i(s)$ in Eq. (2) is based on the proportional resonant plus harmonic controller (PR + HC) [29]. The proportional and integral gains of resonant controller are k_p and k_i, respectively. The bandwidth of each resonant frequency is presented by ω_c, h is the harmonic order, and ω_0 is fundamental frequency. This controller is designed considering that the output filter can be simplified to a total inductance. Thus, k_p is calculated by Eq. (3). Having the crossover frequency of the current loop $f_{ci} = 3$ kHz, the bandwidth of resonant controller $\omega_c = 5$ *rad/s*, the integral gain of resonant controller $k_i = 100$, the gain of inverter $G_{inv} = 225$, and the carrier amplitude $v_{tri} = 5$, the proportional gain of resonant controller is obtained as $k_p = 1.256$. The closed-loop transfer function of the current-controlled scheme $G_{ci}(s)$ is given by Eq. (4).

$$G_{oi}(s) = \frac{PWM(s)\,G_{inv}(s)}{R_f + sL_f} C_i(s) \tag{1}$$

$$C_i(s) = k_p + \sum_{h=1,3,5,7,11,13} \frac{2k_i\omega_c s}{s^2 + 2\omega_c s + (h\omega_0)^2} \tag{2}$$

$$k_p = \frac{2\pi f_{ci} L_f v_{tri}}{G_{inv}} \tag{3}$$

$$G_{ci}(s) = \frac{i_{tabc}(s)}{i^*_{tabc}(s)} \approx \frac{C_i(s)\ PWM(s)\ G_{inv}(s)}{L_f s + R_f + C_i(s)\ PWM(s)\ G_{inv}(s)} \tag{4}$$

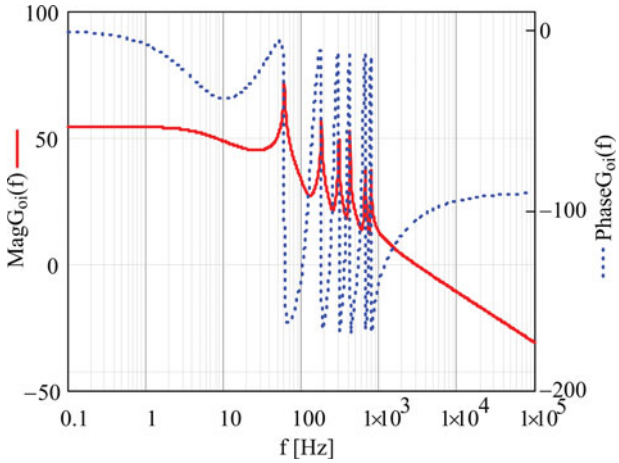

FIGURE 3. Bode plot of the open-loop current transfer function $G_{oi}(s)$.

Figure 3 shows the frequency response of the open-loop current-control scheme $G_{oi}(s)$. The phase margin is about 70°, and the bandwidth of the current loop is 3 kHz.

For digital implementation of the control system in the z-domain, the (PR + HC) controller transfer function of Eq. (2) is discretized with a sampling time of T_s equal to the switching period. Therefore, the controller transfer function $C_i(z)$ can be expressed as Eq. (5):

$$C_i(z) = k_p + \sum_{h=1,3,5,7,11,13} \frac{n_2 z^2 + n_1 z^1 + n_0}{d_2 z^2 + d_1 z^1 + d_0} \tag{5}$$

Let us define a constant called C_t, which is given by:

$$C_t = \frac{k_i {\omega_c}^2}{B} e^{-0.5\omega_c T_s} \sin(T_s B) \tag{6}$$

where the parameter B is given by:

$$B = \sqrt{(h\omega_0)^2 - 0.25{\omega_c}^2} \tag{7}$$

The numerator parameters of (Eq. (5)) are calculated as follows:

$$\begin{aligned} &n_2 = k_i\omega_c T_s,\ n_1 = 0, \\ &\text{and } n_0 = T_s[-k_i\omega_c e^{-0.5\omega_c T_s}\cos(T_s B) - C_t] \end{aligned} \tag{8}$$

and the dominator parameters are calculated as (Eq. (9)):

$$d_2 = 1,\ d_1 = -2e^{-0.5\omega_c T_s}\cos(T_s B), \text{ and } d_0 = e^{-\omega_c T_s} \tag{9}$$

For $T_s = 1/18$ kHz, the parameters in the z-domain controller transfer function of Eq. (5) for the fundamental resonant frequency are calculated as $n_2 = 0.0277$, $n_1 = 0$, $n_0 = -0.0277$, $d_2 = 1$, $d_1 = -1.9992$, and $d_0 = 0.9997$. The same procedure is followed for the harmonic resonant frequencies.

The current reference, i_{pabc}, is used to inject the active power delivered by I_{dc} through the inverter. The waveform

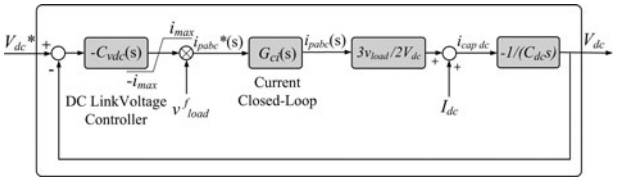

FIGURE 4. Closed-loop control diagram of DC voltage controller.

of the active current reference is defined from the fundamental component of the measured load voltage, v^f_{load}, configuring sinusoidal current. In this paper, the fundamental component of the measured load voltage is used to inject the active current, configuring a sinusoidal current synthesis. Therefore, the active current is a pure sinusoidal current, in phase with the fundamental component of the instantaneous load voltage. Dimensioning of the DC link voltage controller is determined by the transfer function between the defined current reference and the DC link voltage.

From power balance of the PEI terminal, Eq. (10) is achieved, where $i_{cap\ dc}$ is the DC link capacitor current and 3/2 factor comes from the average AC power flow using peak values. The current through the DC link capacitor is obtained as in Eq. (11). The same current in terms of voltage across the DC link capacitor is given by Eq. (12). From Eqs. (11) and (12), the differential equation for the DC voltage is obtained as in Eq. (13). Based on Eq. (13), the DC voltage is regulated by controlling the active current i_{pabc}. The block diagram of the DC voltage control loop is shown in Figure 4. The DC link voltage controller $C_{vdc}(s)$ is multiplied by -1 to compensate for the negative sign of the DC bus voltage dynamics. The open-loop transfer functions of the DC voltage control scheme, $G_{ovdc}(s)$, is presented in Eq. (14). A type 2 controller is chosen for $C_{vdc}(s)$ in Eq. (15). Using the K-factor approach [30], for crossover frequency of the DC voltage loop $f_{cvdc} =$ 18 Hz and phase margin of 60°, the parameters in the controller transfer function are calculated as $f_z = 4.797$ Hz, $f_p =$ 67.543 Hz, and $k_c = 0.0317$.

$$\frac{3}{2}v^f_{load}i_{pabc} + V_{dc}I_{dc} + V_{dc}i_{cap\ dc} = 0 \tag{10}$$

$$i_{cap\ dc} = -\left(\frac{3v^f_{load}i_{pabc}}{2V_{dc}} + I_{dc}\right) \tag{11}$$

$$C_{dc}\frac{dV_{dc}}{dt} = i_{cap\ dc} \tag{12}$$

$$\frac{dV_{dc}}{dt} = \frac{-1}{C_{dc}}\left(\frac{3v^f_{load}i_{pabc}}{2V_{dc}} + I_{dc}\right) \tag{13}$$

$$G_{ovdc}(s) = C_{vdc}(s)\,G_{ci}(s)\,\frac{3v^f_{load}{}^2}{2V_{dc}}\,\frac{1}{C_{dc}s} \tag{14}$$

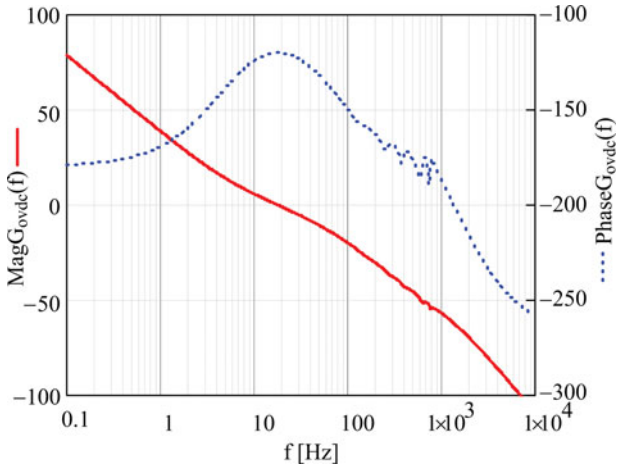

FIGURE 5. Bode plot of the open-loop DC voltage transfer function $G_{ovdc}(s)$.

$$C_{vdc}(s) = \frac{k_c}{s}\frac{(1 + s/\omega_z)}{(1 + s/\omega_p)} \tag{15}$$

Figure 5 shows the frequency response of the open-loop DC voltage control scheme $G_{ovdc}(s)$. The phase margin is about 60°, and the bandwidth of the DC voltage loop is 18 Hz.

For digital implementation of the control system in the z-domain, the controller transfer function of Eq. (15) is discretized with a sampling time of T_s equal to the switching period. Therefore, the controller transfer function $C_{vdc}(z)$ can be expressed as Eq. (16):

$$C_{vdc}(z) = \frac{n_2z^2 + n_1z^1 + n_0}{d_2z^2 + d_1z^1 + d_0} \tag{16}$$

where the numerator parameters are calculated as follows:

$$n_2 = \frac{{T_s}^2 + 2T_s/\omega_z}{(4/k_c\omega_p) + 2T_s/k_c},\ n_1 = \frac{2\ {T_s}^2}{(4/k_c\omega_p) + 2T_s/k_c} \text{ and}$$
$$n_0 = \frac{{T_s}^2 - 2T_s/\omega_z}{(4/k_c\omega_p) + 2T_s/k_c} \tag{17}$$

and the dominator parameters are calculated as Eq. (18)

$$d_2 = 1,\ d_1 = \frac{-8/k_c\omega_p}{(4/k_c\omega_p) + 2T_s/k_c} \text{ and}$$
$$d_0 = \frac{(4/k_c\omega_p) - 2T_s/k_c}{(4/k_c\omega_p) + 2T_s/k_c} \tag{18}$$

For $T_s = 1/18$ kHz, the parameters in the z-domain controller transfer function of Eq. (16) are calculated as $n_2 = 1.2262e^{-5}$, $n_1 = 2.0514e^{-8}$, $n_0 = -1.2241e^{-5}$, $d_2 = 1$, $d_1 = -1.9766$, and $d_0 = 0.9766$.

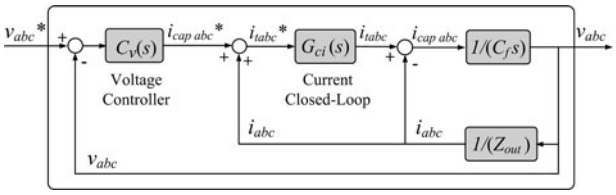

FIGURE 6. Block diagram of the voltage control scheme.

4. MODELING OF THE MASTER DGS

In voltage control mode, the control of the master four-leg PEI consists of active and reactive power droop controllers, a resistive line impedance compensation feedback loop, and voltage and current controllers. The inverter is controlled as voltage source to establish the load voltage and autonomously share load current components with the current-controlled or slave DGs. A feed-forward-based control is developed in a multi-loop voltage control scheme with the current-controlled scheme as inner loop to regulate load voltage/frequency under various load conditions [31]. Applying the filter inductor current as inner feedback variable, the inductor current is now measured directly, allowing overcurrent protection to be easily added to the control scheme. Figure 6 illustrates the control scheme to regulate $v_{abc}(s)$. From Figure 6, $v_{abc}(s)$ is controlled by $i^*_{capabc}(s)$, where $i^*_{capabc}(s)$ is the output of the voltage controller. Substituting for $i^*_{tabc}(s)$ from Eq. (4) in Eq. (19), Eq. (20) is obtained. Taking Laplace transform of Eq. (21), and then substituting for $i_{tabc}(s)$ from Eq. (20) in Eq. (21), Eq. (22) is acquired. The term $[1 - G_{ci}(s)]$ is negligible, and Eq. (22) can be approximated as Eq. (23). Eq. (23) indicates the transfer function between $v_{abc}(s)$ and $i^*_{capabc}(s)$. $G_{ov}(s)$ in Eq. (24) is the open-loop transfer function of the voltage control scheme, where $C_v(s)$ is the controller of the outer voltage control loop. Eq. (25) shows that the output voltage dependence on both the reference voltage and the inverter output current. The proportional resonant plus harmonic controller (PR + HC) of Eq. (26) is applied for the outer voltage regulation loop, ensuring almost zero steady-state error by introducing high gain at the relevant harmonic frequencies in the denominator of system output impedance in Eq. (25). Having the crossover frequency of the voltage loop $f_{cv} = 1$ kHz, the bandwidth of resonant controller $\omega_c = 5$ *rad/s*, the

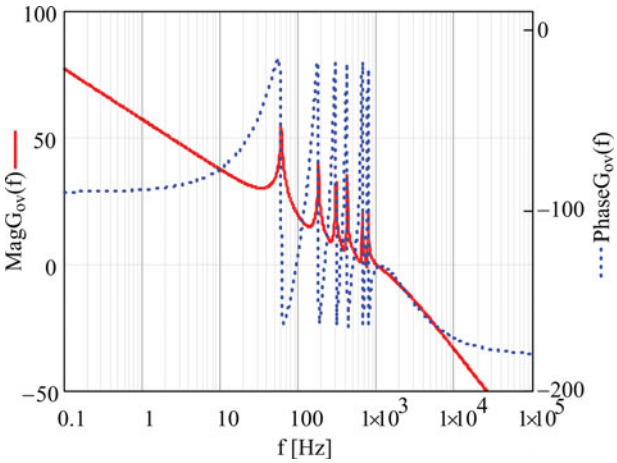

FIGURE 7. Bode plot of the open-loop voltage transfer function $G_{ov}(s)$.

integral gain of resonant controller $k_i = 3$, the proportional gain of resonant controller is obtained as $k_p = 0.069$.

$$i^*_{tabc}(s) = i^*_{capabc}(s) + i_{abc}(s) \tag{19}$$

$$i_{tabc}(s) = G_{ci}(s)\, i^*_{capabc}(s) + G_{ci}(s)\, i_{abc}(s) \tag{20}$$

$$C_f \frac{dv_{abc}(t)}{dt} = i_{tabc}(t) - i_{abc}(t) \tag{21}$$

$$C_f\, s\, v_{abc}(s) = G_{ci}(s)\, i^*_{capabc}(s) - [1 - G_{ci}(s)]\, i_{abc}(s) \tag{22}$$

$$G_{Plant}(s) = \frac{v_{abc}(s)}{i^*_{capabc}(s)} \approx G_{ci}(s)\, \frac{1}{C_f\, s} \tag{23}$$

$$G_{ov}(s) = C_v(s)\, G_{ci}(s)\, \frac{1}{C_f s} \tag{24}$$

$$v_{abc}(s) = \frac{C_v(s) C_i(s)\ PWM(s)\ G_{inv}(s)}{L_f C_f s^2 + C_f R_f s + C_f C_i(s)\ PWM(s)\ G_{inv}(s) s + C_v(s) C_i(s)\ PWM(s)\ G_{inv}(s) + 1} v^*_{abc}(s) - \frac{R_f + L_f s}{L_f C_f s^2 + C_f R_f s + C_f C_i(s)\ PWM(s)\ G_{inv}(s) s + C_v(s) C_i(s)\ PWM(s)\ G_{inv}(s) + 1} i_{abc}(s) \tag{25}$$

$$C_v(s) = k_p + \sum_{h=1,3,5,7,11,13} \frac{2k_i \omega_c s}{s^2 + 2\omega_c s + (h\omega_0)^2} \tag{26}$$

Figure 7 shows the frequency response of the open-loop voltage control scheme $G_{ov}(s)$. The phase margin is about 50°, and the bandwidth of the current loop is 1 kHz.

The voltage (PR + HC) controller $C_v(s)$ is also discretized for digital implementation. For $T_s = 1/18$ kHz, the parameters in the z-domain controller transfer function of Eq. (26) for the fundamental resonant frequency are calculated as $n_2 =$

e^{-4}, $n_1 = 0$, $n_0 = -8.332e^{-4}$, $d_2 = 1$, $d_1 = -1.9992$, and $d_0 = 0.9997$. The same procedure is followed for the harmonic resonant frequencies.

5. STRATEGY FOR LOAD CURRENT SHARING AMONG DGS

In order to achieve a proper control of DGs interface converters in the isolated microgrid, where a system's voltages might be asymmetrical and/or distorted, a comprehensive power theory can be used to have selective sharing of different power/current components. This paper suggests that in such a context, the CPT [32], which proposes a decomposition of instantaneous currents into current terms related to load behavior, should be used. Therefore, the theoretical basis of the selective sharing of load current components among PEIs, which is based on a master-slave approach and the application of the CPT as an alternative for generating decoupled current references for selective and proper current sharing, is presented.

5.1. Basic Concepts and Definitions from CPT

The CPT [32] is a time-domain-based power theory, valid for single-phase and three-phase systems, with three or four-wire circuits, independent from the purity of voltage and current waveforms [33–35].

In the following description, lowercase and uppercase variables are, respectively, instantaneous and root-mean-square (RMS) values. Boldface variables refer to vector quantities (collective values) and the subscript "m" indicates phase variables. Such theory is valid for generic polyphase circuits under periodic operation. The CPT is based on the orthogonal decomposition of instantaneous phase currents, which can be split into different components

$$i_m = i^b_{am} + i^b_{rm} + i^u_m + i_{vm} = i^b_{am} + i_{nam} \tag{27}$$

such that, i^b_a is the balanced active current; i^b_r is the balanced reactive current; i^u is the unbalance current; i_v is the void current; and i_{na} is the non-active current.

The balanced active currents have been determined as the minimum currents needed to convey total active power ($P = \sum_{m=1}^{M} P_m$) absorbed at the PCC. They are given by

$$i^b_{am} = \frac{\langle \boldsymbol{v}, \boldsymbol{i} \rangle}{\|\boldsymbol{v}^2\|}.v_m = \frac{P}{\boldsymbol{V}^2}.v_m \tag{28}$$

where $\langle \boldsymbol{v}, \boldsymbol{i} \rangle$ represents internal product, which can be calculated by the result from the dot product of voltage ($\boldsymbol{v}$) and current ($\boldsymbol{i}$) vectors through a moving average filter and $\|\boldsymbol{v}\| = \sqrt{V_a^2 + V_b^2 + V_c^2} = \boldsymbol{V}$ is the collective RMS value (Euclidean norm) of the voltages.

Similarly, the balanced reactive currents have been defined as the minimum currents needed to convey total reactive energy ($W = \sum_{m=1}^{M} W_m$) absorbed at the PCC. They are given by

$$i^b_{rm} = \frac{\langle \hat{\boldsymbol{v}}, \boldsymbol{i} \rangle}{\|\hat{\boldsymbol{v}}\|^2} \hat{v}_m = \frac{W}{\hat{\boldsymbol{V}}^2} \hat{v}_m \tag{29}$$

where $\hat{v}_m$ is the phase voltage integral without average value (named unbiased time integral). The balanced active and reactive currents always have the same waveforms of the phase voltages (v_m) and the phase voltage integrals ($\hat{v}_m$), respectively. Note that the term "balanced" refers to load symmetry, not to current symmetry.

In a case of balanced load, the PCC only absorbs balanced active and reactive currents; otherwise it also drains unbalance currents, which have been defined as

$$i^u_m = i^u_{am} + i^u_{rm} = i^u_{am} = i_{am} - i^b_{am} + i_{rm} - i^b_{rm} \tag{30}$$

$$i_{am} = \frac{P_m}{V_m^2} v_m;\ i^b_{am} = \frac{P}{\boldsymbol{V}^2} v_m;\ i_{rm} = \frac{W_m}{\hat{V}_m^2} \hat{v}_m;\ i^b_{rm} = \frac{W}{\hat{\boldsymbol{V}}^2} \hat{v}_m \tag{31}$$

such that i_{am} and i_{rm} are the phase active and reactive currents, respectively.

The void currents are defined as the remaining phase currents. They do not convey active power or reactive energy and represent all the load non-linearity currents (harmonics). However, they cause power loss and/or electromagnetic interference in the utility lines

$$i_{vm} = i_m - i_{am} - i_{rm} \tag{32}$$

By definition, all the terms are orthogonal (decoupled) to each other; thus, the collective RMS current can be calculated by

$$\boldsymbol{I}^2 = \boldsymbol{I}^{b2}_a + \boldsymbol{I}^{b^2}_r + \boldsymbol{I}^{u2} + \boldsymbol{I}_v{}^2 = \boldsymbol{I}^{b^2}_a + \boldsymbol{I}_{na}{}^2 \tag{33}$$

Accordingly, multiplying the collective RMS current and voltage, the apparent power (A) can be split into

$$A^2 = \boldsymbol{V}^2 \cdot \boldsymbol{I}^2 = P^2 + Q^2 + N^2 + D^2 \tag{34}$$

where:

- $P = \boldsymbol{V} \cdot \boldsymbol{I}^b_a$ is the active power (34.a)
- $Q = \boldsymbol{V} \cdot \boldsymbol{I}^b_r$ is the reactive power (34.b)
- $N = \boldsymbol{V} \cdot \boldsymbol{I}^u$ is the unbalance power (34.c)
- $D = \boldsymbol{V} \cdot \boldsymbol{I}_v$ is the void power (34.d)

The active power P is related to the average power transfer. The reactive power Q is related to the reactive energy; the unbalance power N represents the load unbalances. The void power D is the power due to the non-linear behavior of the load and is not related to the useful work or energy storing.

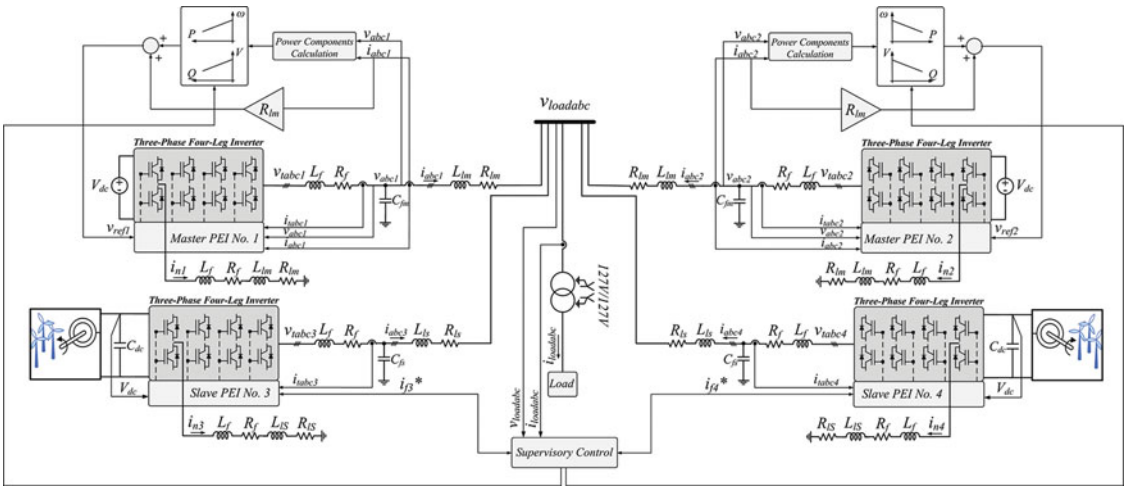

FIGURE 8. Diagram of the considered multi-PEI-based stand-alone microgrid.

5.2. Selective Sharing of Load Current Components among PEIs

Load current sharing is set to ensure efficient utilization of the PEIs' capability in a three-phase four-wire stand-alone microgrid. The microgrid supervisory control defines how the current components are required to be shared among DGs in order to meet any objective function, such as power loss minimization, cost savings, stability, and reliability. One possible goal for load current sharing is to enhance voltage quality at sensitive buses. When a load is non-linear, voltage drops on distribution lines lead to voltage distortion at the load bus. In this paper, the goal of selective sharing of load current components is to have the non-active load current components compensated by the slave DGs located in close proximity and supported by high-bandwidth communication lines. This way, master DGs will be able to establish good-quality voltages at load bus. The slave PEIs are current-controlled and provide current references distributed by the supervisory control. The supervisory control has access to the load current, and act as operation/management unit. It decomposes the load current components into different orthogonal current terms, based on the CPT and assigns each slave converter to supply non-active current components (besides injecting their available energy). Therefore, the master inverters supply the remaining load current autonomously. Since the slave reference currents are synthesized from the load currents, the slave PEIs track the load current at the voltage output frequency, which is controlled by the master PEIs. Consequently, the slave units do not require PLL circuits for the synchronized operation. Therefore, the slaves provide a means for easy expansion of this type of parallel-connected PEIs. Droop control method is employed due to impracticality of communication at remote nodes, and resistive line impedance compensation is adopted to decouple active and reactive power controllers and ensure proper active power sharing among master DGs, irrespective of the mitigation of non-active current components by the slave DGs.

6. APPLICATION EXAMPLES AND DISCUSSION

Figure 8 illustrates the schematic diagram of the considered multi-inverter-based stand-alone microgrid, on which the proposed instantaneous current-sharing strategy has been evaluated using PSIM software. Here, the system under study consists of four sets of four-leg VSI-based PEIs connected through line impedances to the network load. The CPT current decompositions were implemented in an algorithm programmed in a standard *C* compiler, so as to provide a Dynamic Link Library, interpreted by the simulator, while the controllers were implemented using z-domain transfer functions with the switching and sampling frequencies set at 18 kHz. Digital simulation conducted in PSIM is provided to verify the effectiveness of the proposed control strategy. $\underline{v}_{ref1}$, v_{abc1}, and i_{abcn1} represent reference voltage, capacitor voltage, and output current of master PEI number one, respectively, and, $\underline{v}_{ref2}$, v_{abc2}, and i_{abcn2} represent reference voltage, capacitor voltage, and output current of master PEI number two, respectively. $\underline{i}_{f3}$ and i_{abcn3} represent non-active reference current and output current of slave PEI number three, respectively, and $\underline{i}_{f4}$ and i_{abcn4} represent non-active reference current and output current of slave PEI number four, respectively. Note that $v_{loadabc}$ and $i_{loadabc}$ represent voltages and currents at the load bus.

Figures 9 and 10 present the voltage and current waveforms in load terminal and current waveforms in each PEI, under different modes of operations. Initially, the power delivered

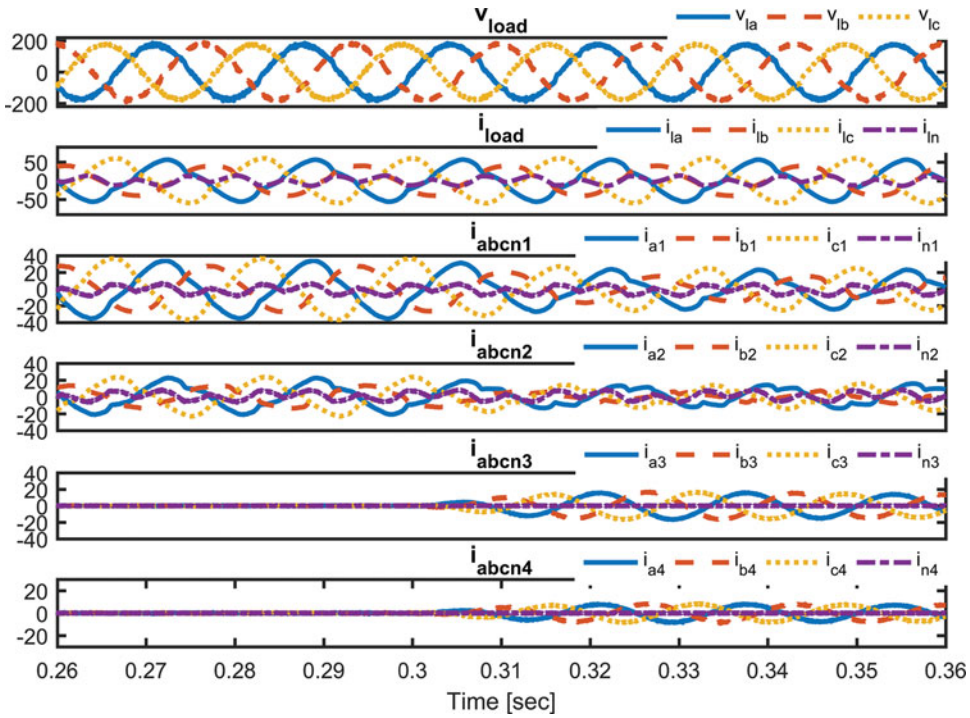

FIGURE 9. Load voltage and current and PEIs current waveforms, when slave PEIs inject active power from local sources (after $t = 0.3$ sec), while master PEIs supplies the remaining load current.

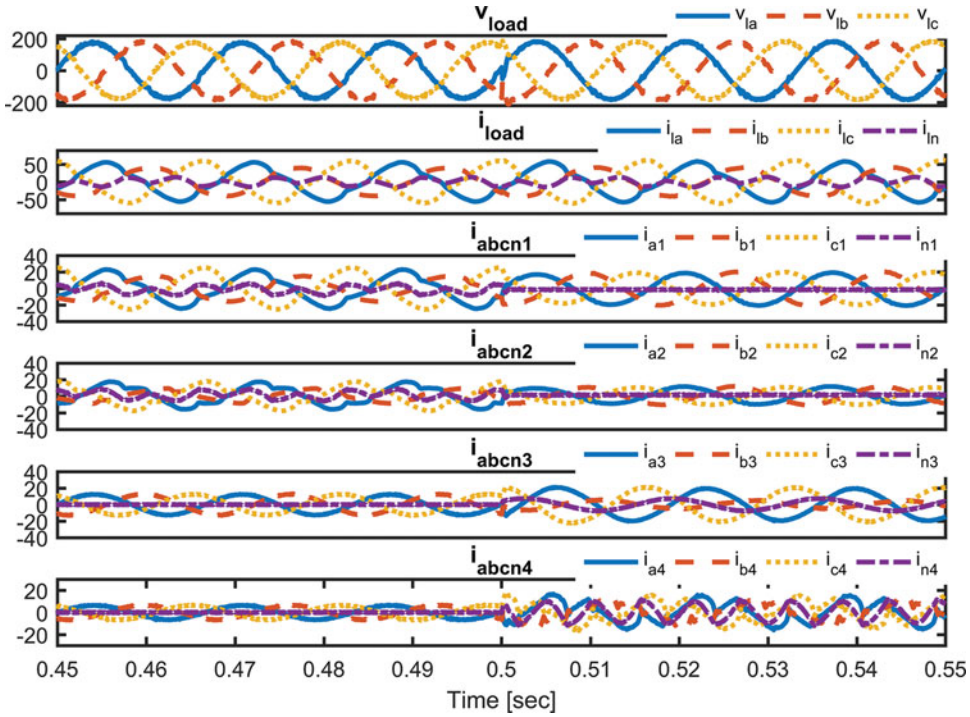

FIGURE 10. Load voltage and current and PEIs current waveforms, when slave PEIs also operate as APF, with non-active currents injection (after $t = 0.5$ sec) with a THD reduction from 5 to 2%.

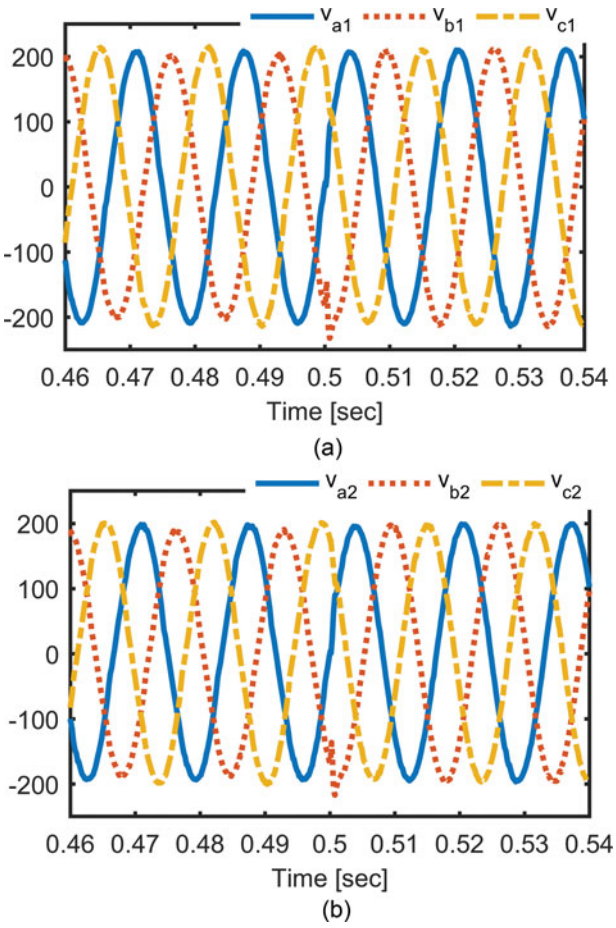

FIGURE 11. Master PEIs voltage waveforms before and after load bus voltage enhancement ($t = 0.5$ sec) with a THD reduction from 3 to 1%: (a) master PEI number one and (b) master PEI number two.

from local power sources of the slave PEIs is zero and the DC-side capacitors are charged (Figure 9). However, the slave units are not operating, and the entire load current is supplied by the master PEIs, which are represented by i_{abcn1} and i_{abcn2} with the droop ratio of ($k_{p1} = \frac{1}{2}\, k_{p2}$) and ($k_{q1} = k_{q2}$) provided by the supervisory control (Figures 12–17). Since the load current is unbalanced and distorted, the load bus voltage is unbalanced and distorted, due to the voltage drops on distribution lines, and this indicates the need for power quality improvement at the load bus. At $t = 0.3$ sec, the four-leg slave PEIs start injecting their power delivered from their local energy source, with slave PEI number three supplying twice the active power of slave PEI number four. Both are based on sinusoidal active currents synthesis. It is also noted that the master inverters supply the neutral current associated with single-phase loads through their fourth legs, that is ($i_{n1} + i_{n2} = i_{loadn}$). Notice that ($i_{loadn}$) includes both linear and non-linear loads among phases and neutral.

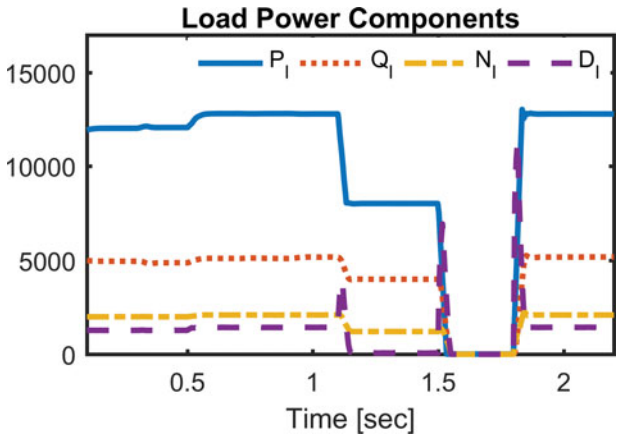

FIGURE 12. Load active, reactive, unbalance, and distortion power components during load changes.

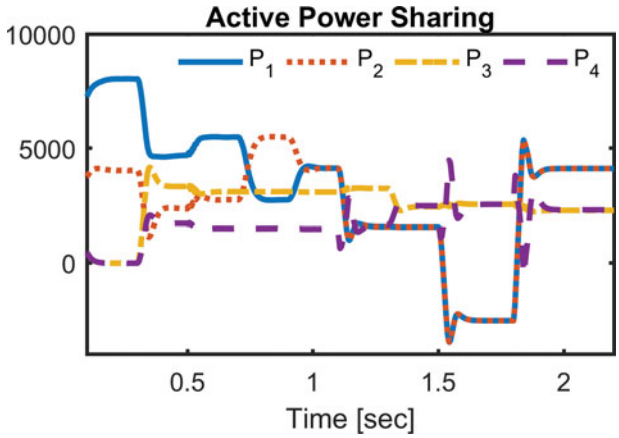

FIGURE 13. Active power sharing among PEIs.

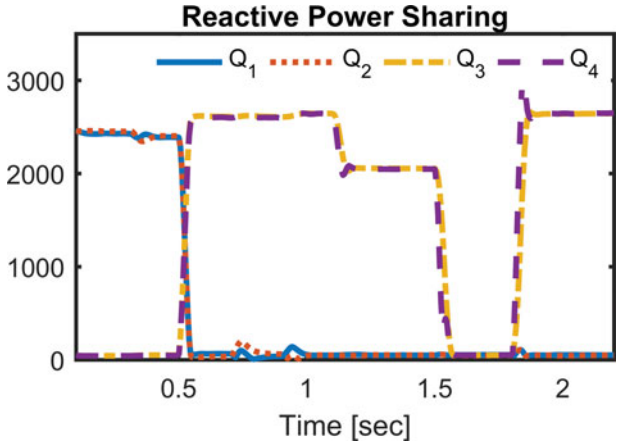

FIGURE 14. Load reactive power sharing among PEIs.

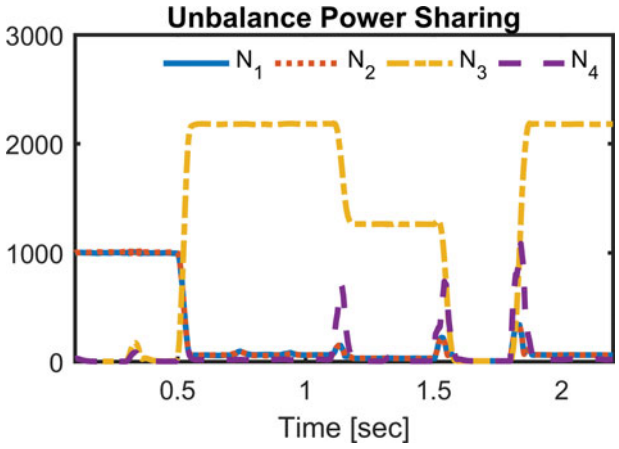

FIGURE 15. Load unbalance power sharing among PEIs.

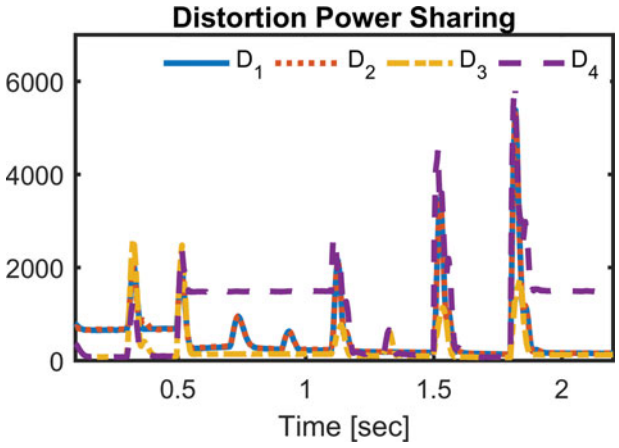

FIGURE 16. Load distortion (void) power sharing among PEIs.

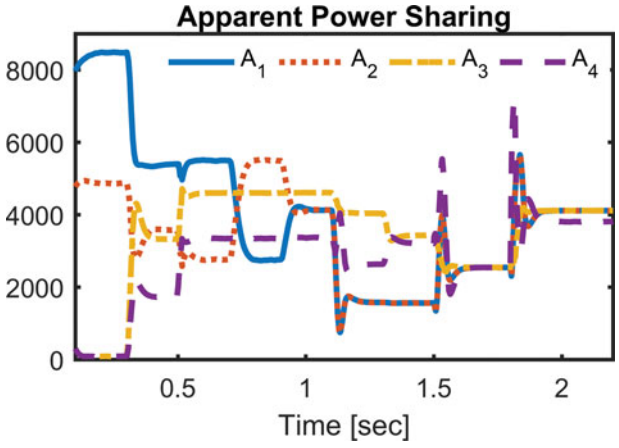

FIGURE 17. Apparent power sharing among PEIs.

To improve the load voltage quality, at $t = 0.5$ sec, the four-leg slave PEIs inject active current and operate as active power filter (APF) simultaneously, supplying all the undesirable current components of the load (Figure 10). This means the master units only need to supply the remaining portion of balanced active current component of the load, which is not supplied by the slaves. This current term is sinusoidal, balanced, and in phase with the load voltages. Consequently, due to not supplying undesirable components, the voltage drops of master PEIs across their distribution lines are not distorted, resulting in the decrease of voltage unbalance and harmonic levels and also compensation of fundamental positive sequence of voltages to the value near the rating at master PEIs terminal and load buses, with a reduction in its THD from 5 to 2%. For this study, each slave PEI supplies half of the load-balanced reactive current component, and the void and unbalanced currents are supplied by slave PEIs numbers three and four, respectively. It can also be observed from Figure 10 that the master PEIs no longer supply the neutral currents associated with single-phase loads, and the slaves take this task through their fourth legs, that is ($i_{n1} = i_{n2} = 0$, $i_{n3} + i_{n4} = i_{loadn}$). It is noted that the slave PEI number three supplies the non-linear part of neutral current associated with single-phase loads, and the slave PEI number four supplies the linear part of neutral current associated with single-phase loads.

Figure 11 presents the master PEIs output voltage waveforms. In [23, 36], the capacitive virtual impedance scheme enhances the LCL filter output voltage quality at the expense of increasing voltage harmonic levels at filter capacitance. Thus, in the cases that capacitor voltage quality is also important, a trade-off should be made between capacitor and output voltage quality. In this paper, the improvement of master PEIs terminal voltage quality and load bus voltage quality is achieved simultaneously as a result of the non-active load current mitigation by the slave PEIs, as it is shown in Figures 10 and 11 (after $t = 0.5$ sec). It means the line impedances of master inverters will not distort their terminal voltages. However, the slave PEIs terminal voltage distortions should not exceed from their maximum allowable values. To apply this constraint, voltages THDs of the slave PEIs terminals are evaluated. Also, the slave PEIs should not be overloaded while compensating loads non-active currents. To apply this constraint, output currents of the slave PEIs are evaluated.

Figure 12 illustrates active, reactive, unbalance, and distortion power components of the load during load switching events, while Figures 13–16 illustrate generated power components by each PEI in stand-alone microgrid. From Figure 12, originally, the system is under the load configuration illustrated in Figure 1, with power components shared

among converters with predefined sharing factors. At t = 1.1 sec, the non-linear part of the load is switched off and the corresponding void power decreases to zero. At t = 1.5 sec, the remaining part of the load is switched off and, thereafter, the system continues operating under no-load conditions. After t = 1.8 sec, the load is turned on again. It can be seen that the adverse effect of load switching event in the islanded microgrid is reflected in load distortion or void power component (D_{Load}).

Figure 13 shows the sharing of the active power component among PEIs. Until t = 0.3 sec, all the load current is supplied by the master PEIs. As the ratio of active droop line setting is ($k_{p1} = \frac{1}{2}\ k_{p2}$), master PEI number one generates twice of master PEI number two, ($P_1 = 2P_2$). At t = 0.3 sec, slave PEIs are ready to inject their available energy, with slave PEI number three supplying twice the active power of slave PEI number four. At t = 0.7 sec, the supervisory control sets new ratio for master PEIs active power droop slope as ($k_{p1} = 2\ k_{p1}$), meaning that master PEI number two supplies twice the balanced active power component master PEI number one, ($P_2 = 2P_1$). At t = 0.9 sec, the supervisory control again changes ratio for the master PEIs active power droop slope as ($k_{p1} = k_{p2}$), meaning that the master PEIs number one and two share the demanded active power component of load equally ($P_2 = P_1$). At t = 1.1 sec, the non-linear part of the load is disconnected resulting in the reduction of the active power supplied by the master PEIs, as the slave PEIs inject sufficient active power from their local power sources to supply the linear loads. It can be observed that slave PEI number three still supplies twice the active power of slave PEI number four. At t = 1.3 sec, the slave PEIs start supplying the same amount of active power, from their local power source. This means lack of energy for slave PEI number three and increasing energy for slave PEI number four with equal rate. It is observed that as the total provision of active power by the slaves is constant, the active power supply by the master inverters will not be affected. At t = 1.5 sec, after the remaining part of the load is switched off, the slave PEIs are still injecting their power delivered from their local power sources to the DC link of the master PEIs, represented by DC voltage sources. It is observed that the active power supplied by the master PEIs have negative values, meaning they are absorbing the slave PEIs injected active power. This is equivalent to the situation in which the master units are charging their storage elements with unity power factor. At t = 1.8 sec, the load is switched on and active power components are shared among PEIs with the predefined sharing factors, within a reasonable time.

Figure 14 shows the sharing of the load reactive power component (Q_{Load}) among the PEIs. As the ratio of reactive droop line setting for master inverters is ($k_{q1} = k_{q2}$), they share the total load balanced reactive power component equally, i.e., ($Q_{1 =}\ Q_2$). After t = 0.5 sec, the slave PEIs start supplying the balanced reactive current component of the load, with each slave providing one half as set by the supervisory control, implicating that the master PEIs are no longer supplying the reactive power component of the load. At t = 1.1 sec, t = 1.5 sec and t = 1.8 sec, the load decreases, is switched off and switched on, respectively. After t = 1.8 sec, the reactive power component of the load is shared based on the previous sharing factors. It is noticed that due to the implementation of resistive line impedance compensation in droop control, P and Q are decoupled and changing the ratio of active power droop slope between master PEIs in Figure 13 has no impact on Q, as can be seen in Figure 14.

Figures 15 and 16 show the sharing of the unbalance and distortion power components of the load (N_{Load}) and (D_{Load}) among the PEIs, respectively. Until t = 0.5 sec, the master PEIs supply the load unbalance and distortion power components equally. After t = 0.5 sec, to improve power quality at the load bus, supervisory control sets slave PEIs number three and four to inject the unbalance and distortion power components of the load, respectively, as illustrated in Figures 15 and 16. Note that from Figures 13–16, the power components supplied by slave PEI number four exhibit overshoots during load switching events at t = 1.1 sec, t = 1.5 sec, and t = 1.8 sec. This is because according to CPT definitions, any disturbances in the microgrid are reflected in the void current, such as disturbances during load switching events at t = 1.1 sec, t = 1.5 sec, and t = 1.8 sec, and since the slave PEI number four is assigned to supply the void current, all the power components supplied by this slave converters are affected. These overshoots are also reflected in the master PEIs as their currents are affected by the slave inverters. The same overshoots can be seen for (D_{Load}) in Figure 12. However, these disturbances are damped in a reasonable time. It is also noted from Figures 15 and 16 that as the non-linear part of the load is switched off at t = 1.1 sec, unbalance power related to the unbalanced non-linear part of the load and total distortion power related to the balanced and unbalanced non-linear part of the load become zero.

Figure 17 illustrates the apparent power of the PEIs, which is composed of inverters' generated active, reactive, unbalance, and distortion power components. It can be seen that after t = 0.9 s, the apparent powers of the master PEIs (A_1 and A_2) are equal as they are generating same power components ($k_{p1} = k_{p2}$). Between t = 1.5 sec and t = 1.8 sec, master PEIs have positive apparent power, while absorbing the injected slave PEIs' active power. Note that in this time interval, all the inverters have equal apparent power, since the slave PEIs are supplying equally active power, from their

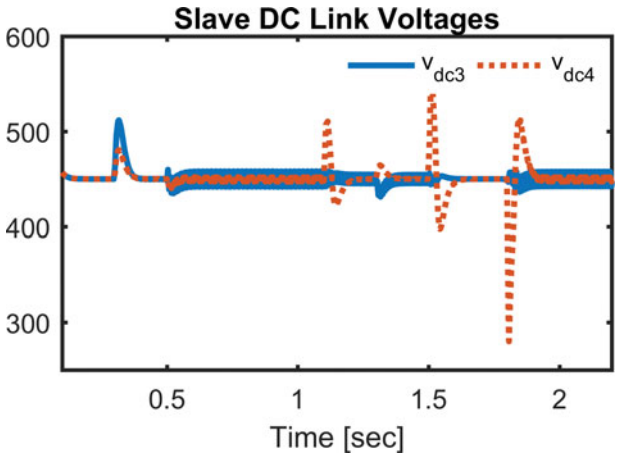

FIGURE 18. Slave PEIs DC link voltages.

local power sources, while the master PEIs are absorbing those slave active power with ($k_{p1} = k_{p2}$).

Figure 18 shows the regulation of slave PEIs DC link voltages at their reference value, 450 V. The controller performance was satisfactorily tracking their corresponding reference commands. It is observed that DC link voltage for slave PEI number three has more ripple, as it supplies unbalance power component of load and, DC link voltage for slave PEI number four has more overshoots during load changes, since it supplies load change events that are reflected in load distortion power.

Figure 19 shows the load bus RMS voltages. It is observed that the provision of load non-active current components by the slave PEIs help the master units to regulate the load bus voltages at nominal value under different load conditions of Figure 12, since the compensation of resistive line impedance is implemented in the droop control system.

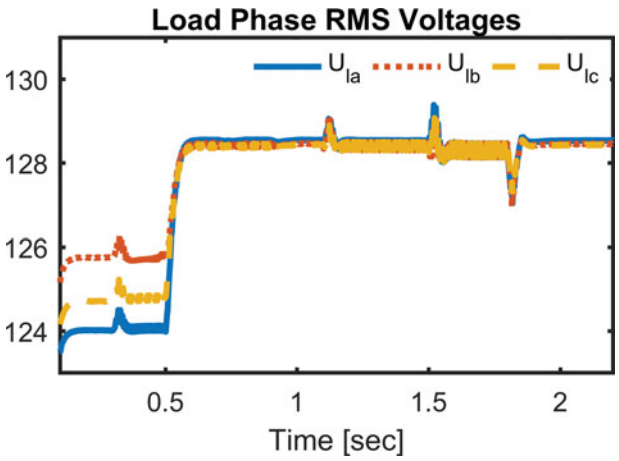

FIGURE 19. RMS phase voltages of the load.

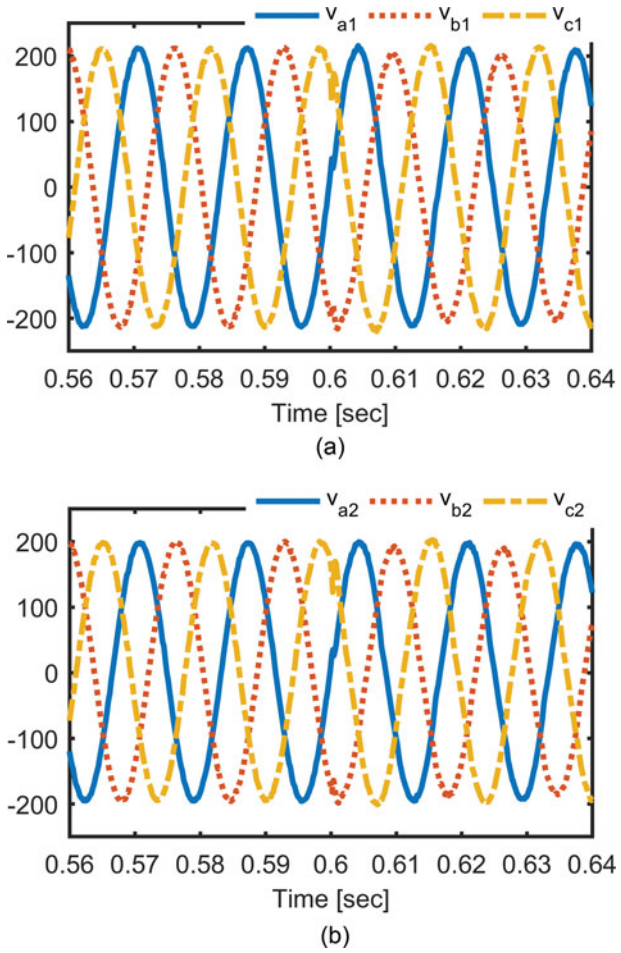

FIGURE 20. Effect of communication interruption on Master PEIs voltage waveforms (after $t = 0.6$ sec) with a THD increment to 3%: (a) master PEI number one and (b) master PEI number two.

Assuming the proposed selective load current-sharing strategy, Figure 20 depicts the effect of a communication interruption on master PEIs. At $t = 0.6$ sec, the slave inverters communication with the supervisory control is disconnected and the non-active current is shared by the master units. Therefore, slave PEIs still inject active current but they no longer operate as APF. It is observed that the provision of non-active components by the master PEIs leads to terminal voltage distortion.

7. CONCLUSION

This paper has proposed a master-slave-based control strategy for selective sharing of load current components among PEIs, valid for a three-phase four-wire stand-alone microgrid, on which the DGs located close to the loads would operate in salve mode to inject the available energy from local power sources and enhance the load bus voltage quality as a result of

the non-active load current mitigation by the slave DGs, while the remaining load would be shared among distant DGs using droop control. Due to complex values of the line impedance, which leads to coupling of active and reactive power droop controls, compensation of resistive line impedance is implemented to decouple the control of those power terms. Therefore, the goal of selective load current sharing in this paper has been load voltage enhancement, in order to meet the desired operating criteria of the microgrid at sensitive load buses and to ensure efficient utilization of renewable energy sources and DGs.

The applied power theory (CPT) makes it possible to identify the load power terms related to non-active behavior and, based on some criteria, which could be the power rating of the converter or its current capability, choose the power components to be compensated. Moreover, using the CPT, no reference-frame transformation is required for the proposed current-sharing strategy.

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