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Quasi-Y Source Multifunctional Inverter for Distributed PV Power Generation

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ATA DA DEFESA PÚBLICA DA TESE DE DOUTORADO DE RAFAEL DOS SANTOS, DISCENTE DO PROGRAMA DE PÓS-GRADUAÇÃO EM ENGENHARIA ELÉTRICA, DA FACULDADE DE ENGENHARIA - CÂMPUS DE BAURU.

Aos 25 dias do mês de agosto do ano de 2023, às 14:00 horas, por meio de Videoconferência, realizou-se a defesa de TESE DE DOUTORADO de RAFAEL DOS SANTOS, intitulada **QUASI-Y SOURCE MULTIFUNCTIONAL INVERTER FOR DISTRIBUTED PV POWER GENERATION**. A Comissão Examinadora foi constituida pelos seguintes membros: Prof. Dr. FLÁVIO ALESSANDRO SERRÃO GONÇALVES (Orientador(a) - Participação Presencial) do(a) Departamento de Engenharia de Controle e Automacao / Instituto de Ciencia e Tecnologia UNESP Campus de Sorocaba, Prof. Dr. JOSÉ ANTENOR POMÍLIO (Participação Virtual) do(a) Departamento de Sistemas e Energia - DSE / Universidade Estadual de Campinas - UNICAMP, Prof. Dr. RICARDO QUADROS MACHADO (Participação Virtual) do(a) Departamento de Engenharia Elétrica e de Computação / Escola de Engenharia de São Carlos - USP, Prof. Dr. MOACYR AURELIANO GOMES DE BRITO (Participação Virtual) do(a) Faculdade de Engenharias, Arquitetura e Urbanismo e Geografia / Universidade Federal de Mato Grosso do Sul, Prof. Dr. LUIS ARMANDO DE ORO ARENAS (Participação Presencial) do(a) Departamento de Engenharia Ambiental / Instituto de Ciencia e Tecnologia - UNESP - Campus de Sorocaba. Após a exposição pelo doutorando e arguição pelos membros da Comissão Examinadora que participaram do ato, de forma presencial e/ou virtual, o discente recebeu o conceito final: APROVADO. Nada mais havendo, foi lavrada a presente ata, que após lida e aprovada, foi assinada pelo(a) Presidente(a) da Comissão Examinadora.

Prof. Dr. FLÁVIO ALESSANDRO SERRÃO GONÇALVES

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This work is dedicated to the Virgin Mary,
'Totus tuus ego sum, et omnia mea tua sunt'.
I also dedicate it to my beloved wife, Priscila, and my dearest daughters: Isabel, Catarina, and Helena.

Esse trabalho é dedicado à Virgem Maria,
"Totus tuus ego sum, et omnia mea tua sunt".
Também dedico à minha amada esposa Priscila e filhas muito queridas: Isabel, Catarina e Helena.

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"Ora et Labora"

Resumo

Os geradores solares fotovoltaicos conectados à rede elétrica podem executar mais funcionalidades do que apenas injetar potência ativa na rede elétrica, podendo também executar serviços ancilares, tal como preconiza a normativa IEEE 1547-2018. Nesse sentido, o emprego de inversores baseados em redes de impedância em geradores solares fotovoltaicos apresenta-se como uma solução potencialmente relevante. Em particular, a topologia de rede de impedância Quasi-Fonte Y destaca-se por possuir características vantajosas para integrar geradores solares fotovoltaicos, tais como flexibilidade de projeto ao se definir a proporção de espiras δ dos indutores-acoplados e a razão cíclica de *shoot-through* D_{st}, modo de condução contínua da corrente no estágio de entrada e capacidade de prover elevados ganhos de tensão com menores razões cíclicas. Todavia, não há trabalhos na literatura empregando tal topologia em geradores fotovoltaicos explorando operação multifuncional. Desta forma, o objetivo principal desta tese está relacionado com a modelagem, projeto e desenvolvimento prático de um inversor Quasi-Fonte Y, incluindo as estratégias de controle que viabilizem sua utilização em um gerador solar fotovoltaico multifuncional trifásico a três fios. Assim sendo, no presente trabalho desenvolve-se um projeto detalhado da rede de impedância, por meio da demonstração das formulações matemáticas necessárias para se especificar seus componentes, baseando-se em valores típicos encontrados em inversores fotovoltaicos comerciais. Adicionalmente, apresenta-se uma metodologia para determinação dos controladores responsáveis pela regulação do barramento CC e corrente do estágio CA do inversor, respectivamente. Para isso, utiliza-se de modelos de pequenos sinais baseados na média de espaço de estados e demonstra-se a obtenção de todas as funções de transferência necessárias para o projeto. Além disso, propõe-se uma metodologia de projeto de um controlador linear MPPT baseado no algoritmo "perturba e observa", incluindo requisitos dinâmicos de controle e determinação das funções de transferência necessárias para o projeto. Para demonstrar a operacionalidade do conversor, simulações computacionais foram realizadas considerando o emprego do inversor fotovoltaico multifuncional Quasi-Fonte Y atuando com diferentes cargas conectadas ao ponto de acoplamento comum. Através dos resultados de simulação, demonstra-se a capacidade do inversor de injetar potência ativa e realizar serviços ancilares simultaneamente, além de se indicar a correta sequência de ativação das diferentes malhas de controle envolvidas, garantindo o funcionamento integral do sistema. Ao fim do trabalho, resultados experimentais são apresentados, a partir de um protótipo de pequena escala com capacidade de processamento de 1,2 kW, tensão de entrada de 250 V_{cc} e conexão com rede CA trifásica de 220 V_{rms} de linha e 60 Hz. Finalmente, por meio da análise dos resultados obtidos, pode-se concluir que a viabilidade da aplicação proposta, incluindo as metodologias de projeto apresentadas, foram confirmadas satisfatoriamente.

Palavras-chave: Engenharia Elétrica, Eletrônica de Potência, Sistema fotovoltaico, Redes de impedância, Quasi-Y-Source.

Abstract

Solar photovoltaic generators can perform more functionalities than just injecting active power into the electrical grid. They can also provide ancillary services, as recommended by the recent update of IEEE 1547-2018 regulations. In this sense, the use of impedance-based inverters in solar photovoltaic generators appears as a potentially relevant solution. In particular, the Quasi-Y Source impedance network topology stands out for its advantageous characteristics for integrating solar photovoltaic generators, such as design flexibility on definition of coupled-inductors winding's proportion δ and shoot-through duty-cycle D_{st}, continuous current conduction mode in the input stage, and the ability to provide high voltage gains with lower duty ratios. However, there are no works in the literature employing such topology in photovoltaic generators exploring multifunctional operation. Therefore, the main objective of this thesis is related to the modeling, design, and practical development of a Quasi-Y Source inverter, including control strategies that enable its use in a three-wire three-phase multifunctional solar photovoltaic generator. Thus, this work develops a detailed design of the impedance network by demonstrating the necessary mathematical formulations to specify its components, based on typical values found in commercial photovoltaic inverters. Additionally, a methodology for determining the controllers responsible for regulating the DC bus and the current of the AC stage of the inverter is presented, respectively. For this purpose, small-signal models based on the average state-space technique are used, and all the necessary transfer functions for the design are obtained. Furthermore, a methodology for designing a linear MPPT controller based on the "perturb and observe" algorithm is proposed, including dynamic control requirements and the determination of transfer functions necessary for the design. To demonstrate the operability of the converter, computational simulations were performed considering the use of the multifunctional Quasi-Y Source photovoltaic inverter with different loads connected to the common coupling point. Through the simulation results, the inverter's ability to inject active power and perform ancillary services simultaneously is demonstrated, along with indications related to the correct activation sequence of the different control loops involved, ensuring the integral functioning of the system. At the end of the work, experimental results are presented based on a small-scale prototype with a processing capacity of 1.2 kW, a DC input voltage of 250 V_{dc}, and connection to a three-phase AC grid of 220 V_{rms} line voltage and 60 Hz. Finally, through the analysis of the obtained results, it can be concluded that the viability of the proposed application, including the presented design methodologies, has been satisfactorily confirmed.

Keywords: Electrical engineering, Power electronics, Photovoltaic energy systems, Impedance Networks, Quasi-Y-Source.

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1 Introduction

The energy demand was never so critical as today. This scenario was intensified by the recent sanitary crisis caused by the Covid-19 pandemic, which fostered the seek for energy in many emergent markets (AGENCY, 2021). However, the lack of solutions to some issues related to electrical energy distribution still favors the utilization of fossil fuels and their derivatives, partially reverting the progress obtained with the utilization of alternative energy sources. In this scenario, the use of renewable energy is presented as an interesting solution to solve several problems related to the supply of electrical energy (IRENA, 2021).

Moreover, the integration of distributed energy resources (DER) in the main electric energy distribution system characterizes what is defined as "Distributed Generation"(JENKINS; EKANAYAKE; STRBAC, 2010). However, many challenges related to power quality, stability, and energy management arise from such a power generation strategy. Despite the many types of renewable energy sources that can be used in DGs, in the last years, applications based on photovoltaic (PV) generation had been gaining popularity, due to the decreasing costs in several components that comprise a PV power generation system and improvements in solar energy technology, with a great number of research work dedicated to finding solutions to many challenges related to this field (ZEB et al., 2018b).

Hence, to better contextualize this issue and outline the context of this work, some of the most basic challenges regarding PV power generation and integration with the main grid should be discussed.

1.1 PV power generation challenges and opportunities

The voltage magnitude provided by a single PV module is relatively low when compared with the required value necessary to integrate such energy sources through grid-connected inverters (GCI). For instance, single solar PV panels have a typical voltage range of 20-45 V_{dc} (ANDERSEN et al., 2003), (BADDIPADIGA; FERDOWSI, 2016) whereas typical values for GCI DC link voltages range from 200-600 V_{dc}, depending on the application (SIWAKOTI et al., 2014e), (CALLEGARI et al., 2020).

As related in several works in the literature, examples of common solutions to this problem may involve a) The utilization of series association of PV panels; b) The adoption of two-stage GCIs, such that the first stage is responsible to increase the input voltage value (voltage step-up) while simultaneously explores the maximum available power through MPPT control strategy, guaranteeing the second stage converter successfully integrates the generated energy into the main grid. Additionally, commercial inverters may use modified single or three-

phase full bridge configurations, with galvanic isolation at the DC or AC sides (KHAN et al., 2020); or transformerless topologies, such as HERIC, H5, H7, ZVR, or four-leg, among other configurations (DUONG et al., 2022). These alternatives may introduce additional power conversion stages, with the objective of solving safety issues related to the leakage current in PV power generation systems (ESTÉVEZ-BÉN et al., 2020). On the other hand, due to the stochastic behavior of PV panels, caused by the variability of solar irradiation, the energy supply available by such power sources is intermittent, which offers greater energy integration challenges. This type of problem requires that the used power converters must be flexible and reliable in different operational scenarios.

Besides the challenges related to the characteristics of PV panels themselves, the increasingly non-linear characteristic of the modern electric grid creates many challenges for maintaining power quality (BAJAJ; SINGH, 2020). In this context, it is expected that significant changes in the roles played by power distribution organizations and electrical energy consumers must be an increasing trend (BUTT; ZULQARNAIN; BUTT, 2021). In this new context, the owners of distributed generators could perform ancillary services, helping to solve power quality issues on the grid, for example. Hence, grid-connected distributed generation systems based on PV, due to existing power electronics and control systems, could perform more tasks than simply providing the maximum available active power or operating in island conditions in critical situations. Recent normative changes, such as IEEE Std 1547-2018 (IEEE, 2018), fostered this scenario, stating that inverters can perform other systemic functions besides simply injecting active power, and characterizing the multifunctional operation of such converters.

In this context, the use of power theories that allows the characterization and distinction of the different components that comprise the available electrical energy at the point of common coupling (PCC) are useful for establishing power compensation control references for PV inverters (PAREDES, 2011), (NEJABATKHAH; LI; TIAN, 2019). There are in the literature several power theories available such as pq (AKAGI, 1983), FBD (Fryze-Buchholz-Depenbrock) (DEPENBROCK, 1993), and CPC (Currents Physical Components) (CZARNECKI, 2008). However, Conservative Power Theory (CPT) (TENTI; PAREDES; MATTAVELLI, 2010), (DING; MAO; CHANG, 2021) presents interesting characteristics of orthogonality, allowing the generation of suitable current references for selective compensation, which enable the provision of ancillary services by GCI. Furthermore, another advantage of the CPT theory lies in its ability to provide an intuitive understanding of the physical meaning of each power term component.

As can be seen, the challenges and opportunities related to PV power generation are deeply dependent on a technological interface comprised of many elements, including power electronics, digital systems, and passive filters, among other devices. Therefore, before proposing a different scheme to be used in PV DGs in an on-grid setup, the conventional solution often found in the literature must be understood and the gaps and issues of such strategy should be analyzed before proposing new approaches.

1.2 Typical power electronics solution to PV power generation

Figure 1.1 shows typical power electronics solutions applied in a PV power generation scheme, considering the on-grid setup. The PV panels could be connected in series or parallel, depending on the voltage and current requirement of the application and the number of MPPT trackers available at the inverter (BALATO; COSTANZO; VITELLI, 2015). The input filter usually comprises an arrangement of capacitors and EMI filters, such that voltage and current ripples are minimized, improving the MPPT performance, particularly against noise perturbation (SANTRA et al., 2020). Due to the voltage boost requirement, a DC-DC step-up converter is placed between the PV and DC-AC converter (inverter). Many topologies can be used, including isolated and non-isolated strategies (RAGHAVENDRA et al., 2019) and among the possible converter topologies, those that exhibit current-source input characteristics are more desirable as it promote lower current ripple content.

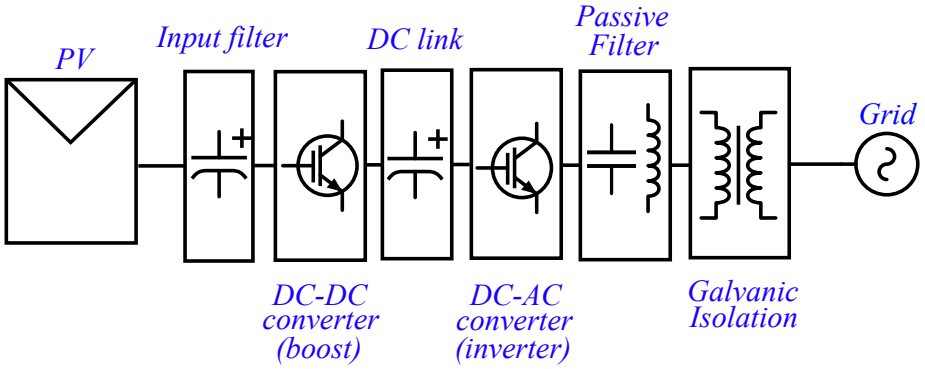


Figure 1.1 – Typical power electronics solution to PV power generation.

The DC link is typically comprised of a group of electrolytic capacitors, such that a stable and low ripple content DC voltage is available at the input stage of the inverter. Due to the presence of the capacitors at the DC link, the inverter is a voltage-source type, with a topology that can vary depending on the configuration of the grid (single or three-phase configuration) and the galvanic isolation requirement, as discussed further in this section. Furthermore, the inverter can be used as a controlled voltage source or current source, but in on-grid configurations, it is usually employed as a controlled current source (ZEB et al., 2018b).

Due to security reasons, galvanic isolation may be required (FREDDY et al., 2013), (DOGGA; PATHAK, 2019). Hence, transformers can be used to implement such isolation, which allows compliance with security requirements and avoid the insertion of DC current components on the grid. In this case, the transformers can be used at the AC or DC sides of the PV DG. When applied at the AC side, they are connected after the passive filters and before the grid, but due to the grid's fundamental frequency, such devices become bulky and expensive. When used on the DC side, they are employed between the PV input filter and inverter DC link, but a relatively complex power electronics system is required. Finally, the transformerless strategy became more popular recently, which avoids the utilization of transformers by employing modified control

modulation schemes or inverter topologies, such as H5, HERIC, REFU, and DCBP, for example, (TEODORESCU; LISERRE; RODRIGUEZ, 2011), (LUO; YE, 2017), (ZEB et al., 2018a).

Many other aspects could be analyzed regarding PV inverters, which can be seen in many reviews found in the literature (MOREY et al., 2023), (KIBRIA et al., 2023), (HAZIM et al., 2023). However, the following issues of the typical solution, depicted in Figure 1.1, for PV power generation can be stated:

1. *Buck type inverter*: Conventional inverters are buck-type converters, that is, the synthesized AC voltage amplitude is lower than the DC link voltage. Such limitation requires the presence of a voltage step-up DC-DC converter connected at the inverter input stage or a higher input voltage, through the association of multiple PV panels in series, for example. In any case, additional implementation costs and lowering of the system's overall reliability are the main concerns of these solutions (ZENG et al., 2013), (AKBAR et al., 2019);

2. *Dead-time requirement*: The simultaneous conduction of the inverter same leg transistors is forbidden in conventional topologies, due to problems derived by the short-circuit caused by this condition. Hence, to avoid this problem, dead-time strategies are employed within the inverter PWM controller. However, it is well-known that dead-time can cause distortions of the output voltage of the inverter, which is known as the dead-time effect (BEN-BRAHIM, 1998), (MALLEMACI et al., 2023);

3. *Double-stage architecture*: Due to the necessity of having a double-stage configuration, comprised of DC-DC and DC-AC converters, the reliability and flexibility of the typical solution depicted in Figure 1.1 are negatively affected. Moreover, the presence of additional controller circuits, heat sinks, and power switches for each individual stage, requires a more complex power system design and layout when compared with single-stage architectures, which contributed to an increase in volume and cost when compared with the latter solution.

As an alternative to double-stage inverters, it can be found in the literature many buck-boost single-stage inverters topologies (SAHOO et al., 2018). Such topologies present different merits and disadvantages. Among the disadvantages, one can cite the high current stress and bulky inductors, and in some cases an increased number of power switches. Moreover, as can be seen by the solution provided by (BRITO et al., 2015), based on a current-source inverter (CSI), at least one inverter same-leg upper and lower switches should remain activated simultaneously. If this condition is not ensured, then an abrupt change in the flow of inductor current would lead to a voltage spike across the inductor capable of damaging the switches. However, to overcome some of the disadvantages of conventional inverters, (PENG, 1999) has introduced impedance-source inverters (INI), which employ shoot-through conduction in their modes of

operation. The INI has been receiving an increased research interest in the last years (JAMAL et al., 2022), and presents the following features:

1. *Buck-Boost type inverter*: INIs are buck-boost type converters, that is, there is no need to increase the input voltage or employ additional DC-DC converters to obtain higher AC voltages at the output stage;
2. *Flexible voltage gain determination*: It is possible to obtain different values of DC link voltages by adjusting the shoot-through conduction period, which is responsible for increasing the impedance-source network input voltage;
3. *No dead-time requirement*: There is no need for dead-time protection since INI employs shoot-through conduction to realize voltage boost;
4. *Single-stage topology*: There is no need to design a double-stage power processing converter since the INI can boost the input voltage and implement the DC-AC conversion in a single-stage architecture.

Due to these interesting characteristics of INI [1], particularly considering PV power generation, the operational principles of this kind of inverter are further analyzed in the next section.

1.3 Impedance-source network inverters (INI)

The INI was originally developed to overcome the limitations associated with conventional inverters based on voltage source (VSI) due to: a) The activation of switches located on the same inverter leg, by EMI or undesired control actions; b) The buck type characteristic of these converters, which limits the magnitude of the inverter AC output voltage. The Z-Source inverter, introduced by (PENG, 1999), was the forerunner of INI, and its mode of operation remains the same for most of the topologies developed afterward. The Z-Source inverter has two states of operation: active state and shoot-through state.

In the active state, the power source is connected directly to the load, and the inverter operates in the traditional manner. In the shoot-through state, the upper and lower switches located at one or more inverter legs are activated simultaneously (shoot-through conduction). This scenario is now possible since the impedance-source network allows the disconnection of the power supply from the rest of the circuit when shoot-through conduction occurs. Moreover, the impedance-source network promotes particular energy management on its energy storage devices, making the buck-boost operation possible.

[1] It is not the objective of this work to perform a comprehensive review of the different single-stage inverters topologies that can be used in PV power generation systems. However, the interested reader can relate to (SAHOO et al., 2018) and other similar works to obtain more details about this particular topic.

There are many topologies for impedance network converters in the literature for different applications, and as observed by (JAMAL et al., 2022), these converters are based on different combinations of energy storage elements, such as inductors and capacitors, and may contain diodes and other power switches. Figure 1.2 shows the schematic diagram and characteristic waveforms of the conventional inverter and INI, for comparison purposes. It can be seen that with INI, the DC link voltage $V_{DC\,link}(t)$ has a pulsating waveform, with an amplitude greater than input voltage V_{in} by a factor of B (boost gain). The B factor is directly related to the shoot-through duty cycle D_{st}, which defines the period of shoot-through conduction, and the switching period T_s. Furthermore, the AC output amplitude voltage is B times greater when compared with the conventional scheme.

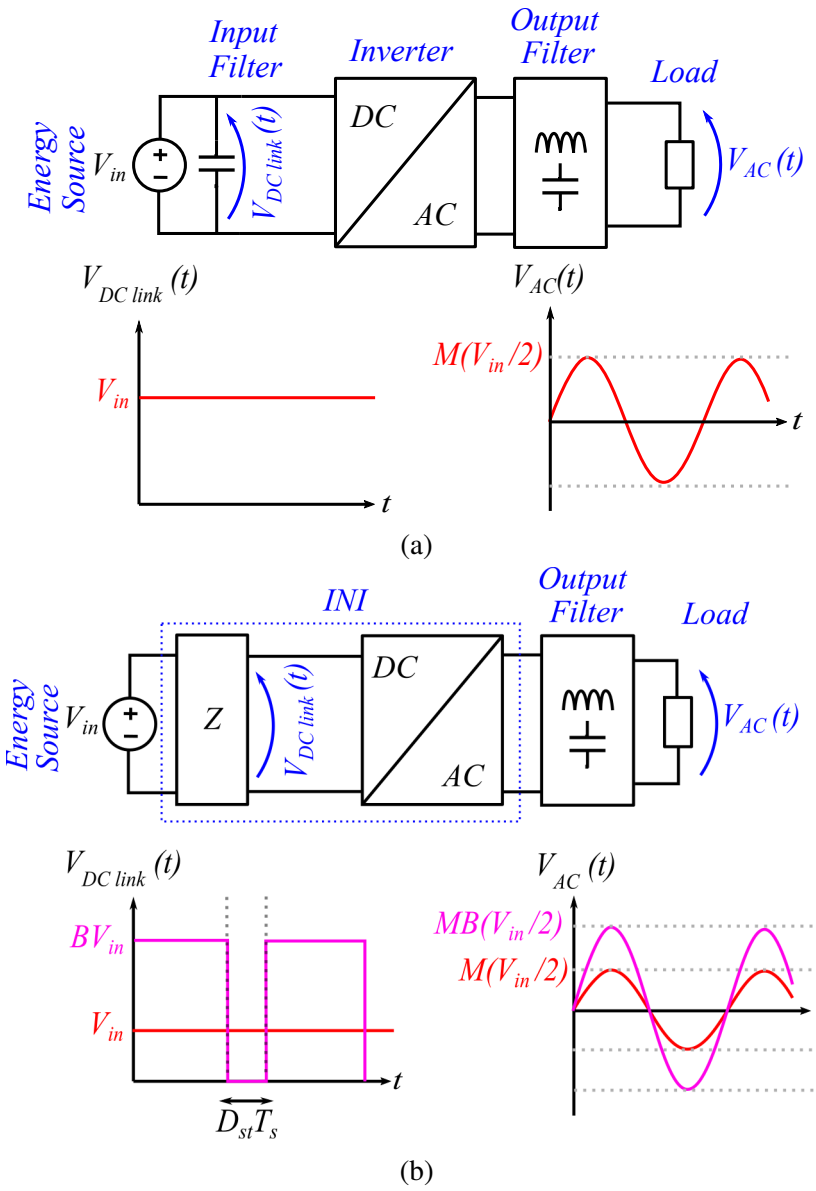


Figure 1.2 – Examples of VSI schemes: a) Conventional; b) INI.

Since the introduction of the Z-Source impedance-source network, research in this field focused on the development of new topologies (SIWAKOTI et al., 2014c), (YADAV et al., 2022)

and several modulation and control techniques (SIWAKOTI et al., 2014d), (ABDELHAKIM; BLAABJERG; MATTAVELLI, 2018), which seeks to improve the performance of the impedance-source converter, while keeping reliability and efficiency. The proposition of new topologies was driven mainly by the purpose of achieving lower power switch stresses while keeping a higher voltage gain. Therefore, many solutions were developed, based on switch inductors (SHARIFI; MONFARED, 2018), tapped inductors (ESMAEILI et al., 2019), and hybrid impedance sources (SABARISH et al., 2021). Among these different topologies, the ones based on magnetic coupling are particularly attractive, since it allows higher converter voltage gain with the aid of coupled inductors.

The insertion of coupled inductors adds an additional degree of freedom to characterize the impedance-source network voltage gain, besides the shoot-through duty cycle, as explored in (LOH; BLAABJERG, 2013), which lead to the development of different converter topologies such as isolated Z-source converters (JIANG; CAO; PENG, 2011), LCCT-Z, (ADAMOWICZ, 2011), TZ-source (NGUYEN; LIM; KIM, 2012), Trans-Z source (QIAN; PENG; CHA, 2011), T-Source (STRZELECKI et al., 2009), A-source (SIWAKOTI et al., 2016) and Y-Source (SIWAKOTI et al., 2014e).

Considering the wide variety of impedance-source networks configurations based on magnetic coupling, the ones based on the Quasi-Y source network are of particular interest, as they can provide one of the highest voltage gains with smaller shoot-through periods (SIWAKOTI et al., 2014b). Therefore, the current research concerning the Quasi-Y source network is further discussed in the next section.

1.4 Quasi-Y source network inverter

In the last years, the research conducted with Y-source impedance networks covered different aspects of this class of impedance-source converter, ranging from:

1. The proposition of new topologies to reducing input current ripple (WANG et al., 2022) and allowing soft-switching (GUAN et al., 2022), higher voltage boosting gains through switched inductors (YAO et al., 2022), or the intrinsic damping of DC-link voltage spikes due to leakage inductances (NIKBAHAR; MONFARED, 2022; SIWAKOTI et al., 2014a);

2. The review of Y-source based magnetic-coupled impedance source networks (YADAV et al., 2022; REDDIVARI; JENA, 2022a);

3. Applications with renewable energy sources based on solar PV or wind-based generators (RAJAEI; YAZDANI; EBADI, 2022; REDDIVARI; JENA, 2022b);

4. The proposition of model-predictive control approaches (ISMEIL; ORABI; ABDELAAL, 2023);

Amid the many topologies proposed to improve the Y-Source converter, the Quasi-Y-Source (QSY) introduced by (SIWAKOTI; BLAABJERG; LOH, 2015a), (SIWAKOTI; BLAABJERG; LOH, 2015b), whose schematic is depicted in Figure 1.3 [2], stands out due to its advantageous characteristics. For example, the QSY network has the possibility of presenting continuous input current, which is beneficial for renewable generation sources such as solar PV panels. Additionally, in this topology, there is an absence of core saturation on the coupled inductors, which has a positive impact on its design. Regarding voltage step-up capability, the QSY network presents one of the highest voltage gains among the impedance-source networks (SIWAKOTI; BLAABJERG; LOH, 2015a), with a relatively lower shoot-through period.

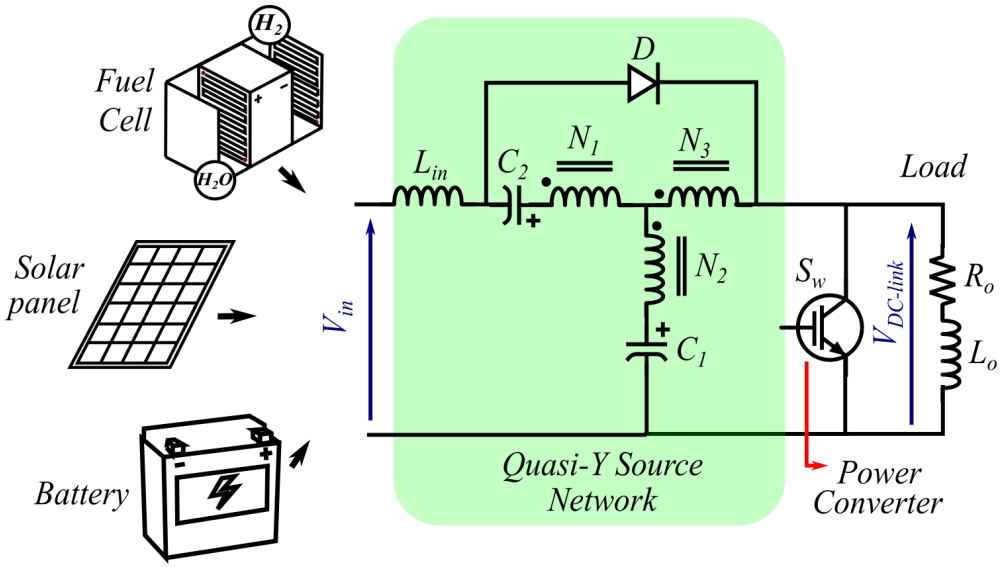


Fig. 1.3 – QSY inverter schematic diagram.

As can be seen in Figure 1.3, the QSY network comprises the diode D, the inductor L_{in} and the capacitor C_2, which avoids core saturation due to DC current component. Also, there are three coupled inductors with windings turn-ratio defined by N_1:N_2:N_3, which together with the capacitor C_1, store energy during the different operational stages (shoot-through and active stages, respectively). The power switches S_w can represent a transistor bridge (half or full bridge configurations) in the case of DC-AC converters. The load impedance is given by R_o and L_o, respectively. A QSY impedance-source inverter, operating in continuous conduction mode (CCM) and with tight magnetic coupling, has two main states of operation, namely, shoot-through and active states, as a conventional INI.

The characteristic voltage and current waveforms for each operational stage are shown in Figure 1.4 [3], where D_{st} is the shoot-through duty cycle and T_s is the switching period. Yet, V_g is the gate signal for S_w, and it is high at shoot-through periods, and low during the active state. The

[2] Not only PV panels can be connected at the input stage of the QSY inverter, but batteries and fuel cells are other power sources that could be used with this converter. They are shown here to illustrate the input stage types that benefit from the characteristics of the QSY network.

[3] The waveforms are not in scale. The main objective is to show the waveform's characteristic shapes for each operational stage, besides indicating other variables of interest.

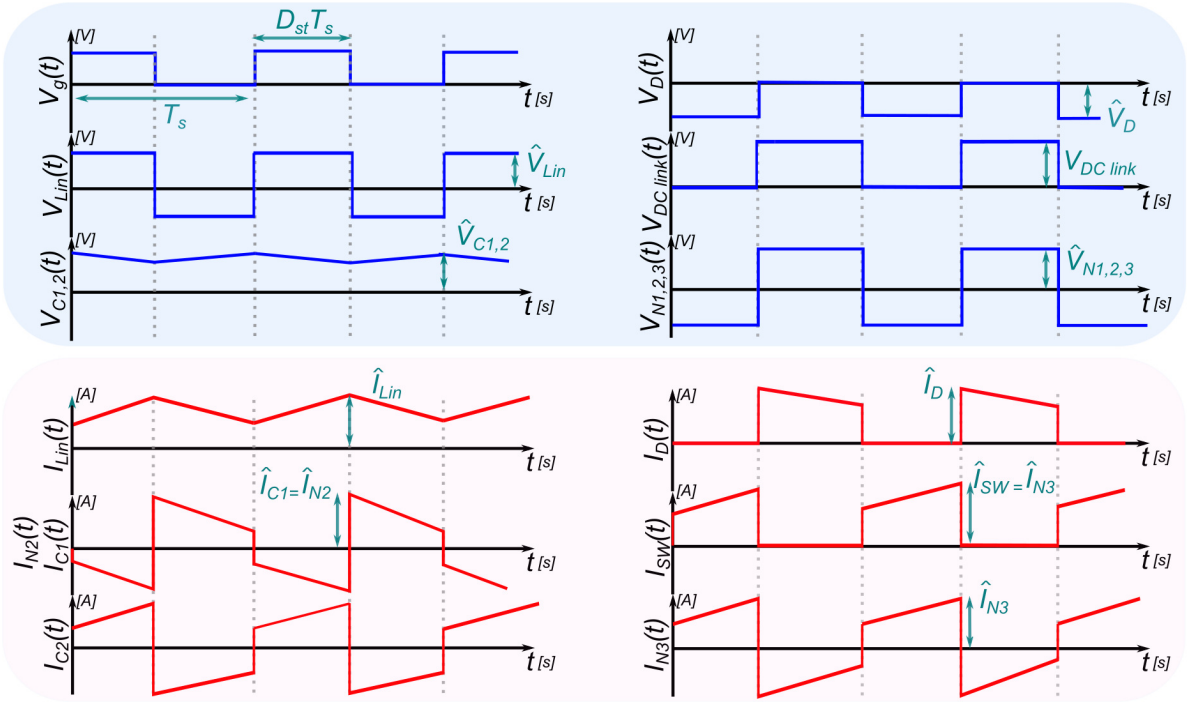


Figure 1.4 – The characteristic voltage and current waveforms of the QSY converter.

converter equivalent circuits for each state are depicted in Figure 1.5 [4]. During the shoot-through conduction state (S_w turned on and D blocked) input energy is stored in the coupled inductors with windings turns ratio N_1:N_2:N_3, and C_1 is discharged, while load current does not depend on the input stage. At the active state (D turned on and S_w turned off), C_1 is charged and the energy coming from V_{in} is delivered to the load through diode D, together with the previously stored energy in the coupled inductors through DC link coupling. Finally, the ideal voltage gain B of the QSY converter is given by (1.1), where δ is related with N_1:N_2:N_3 turns ratio, and given by (1.2) and D_{st} is shoot-through duty-cycle. Notice that depending on the value of δ, the required D_{st} value can be lowered to obtain the same B. This feature brings an additional design degree of freedom for the QSY inverter when compared with other INI. Moreover, auxiliary variables definitions are given as $\delta' = 1 - \delta$ and $D'_{st} = 1 - D_{st}$.

$$B = \frac{V_{DC\,link}}{V_{in}} = \frac{1}{(1 - \delta D_{st})} \tag{1.1}$$

$$\delta = \frac{N_1 + N_2}{N_2 - N_3} \tag{1.2}$$

Given the characteristics of the QSY inverter, the present work aims to develop solutions to the issues stated in section 1.2, through the use of a PV inverter based on the Quasi-Y Source impedance network. The reasons for the adoption of such a strategy are given below:

[4] The currents I_{N1}, I_{N2}, I_{N3} and voltages V_{N1}, V_{N2}, V_{N3} are those present in the inductors that have the respective windings number.

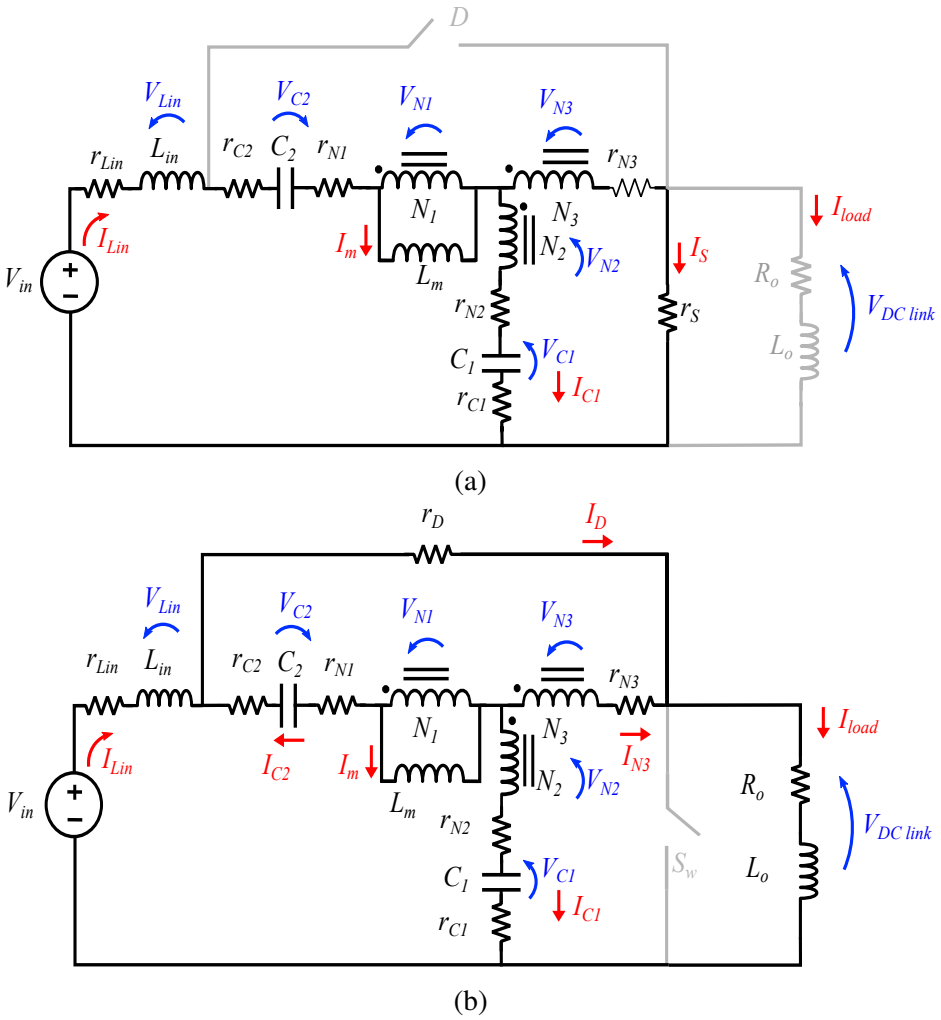


Figure 1.5 – Equivalent circuits of the QSY converter: a) Shoot-through state, b) Active state.

1. Some of the inherent challenges related to PV power generation can be addressed by adopting PV inverters that have voltage step-up characteristics, with continuous and low input current ripple. Moreover, the single-stage configuration is desirable, due to its inherent advantages. This is the case for the QSY inverter. Moreover, the voltage gain flexibility of such a converter facilitates the integration of intermittent sources, as is the case of solar PV panels, satisfying a wider range of operations in different irradiation scenarios. However, the design flexibility feature available in the QSY inverter also brings additional challenges, which will be covered along this thesis.

2. The use of CPT can provide control references for selective current compensation, and can further increase the operational flexibility offered by the QSY inverter, also allowing it to provide ancillary services. In addition, the immunity to shoot-through conduction, either caused by electromagnetic disturbances or control erratic behavior, mitigates power quality problems related to dead-time features, for example. In this case, the PV-based QSY inverter can use the current references generated by the CPT and inject active power to the grid, while compensating other current components if required to do so. Despite

the extensive list of existing works in the literature related to this particular topic, there are few applications of inverter topologies based on the QSY network in multifunctional scenarios. In this sense, it is the objective of this work to explore this gap in the literature.

1.5 Objectives

The global objective of this thesis is to explore methodologies to obtain a multifunctional, three-phase/three-wire and full-bridge inverter based on the Quasi-Y source network, to be used in the PV power generation context, considering the use of Conservative Power Theory (CPT) to allow the execution of ancillary services. The specific goals to be achieved are listed below:

1. Propose a design methodology for the Quasi-Y impedance-source network to be used in a PV multifunctional inverter, considering components' nonidealities characteristics.
2. Propose a linear control design methodology that allows an effective decoupled control of the DC link and inverter AC current stage, realizing its practical implementation with digital controllers in a DSC (Digital Signal Controller) platform.
3. Propose an MPPT control design methodology for the QSY inverter, with an appropriate mathematical definition of the required transfer functions and criteria for dynamic requirements during the design stage.
4. Study and propose the use of the Conservative Power Theory (CPT) to bring multifunctional operating characteristics to the QSY inverter, allowing the converter to extract the maximum power available from PV panels and perform ancillary services simultaneously
5. Validate the obtained simulation results and proposed methodologies with an experimental, low-scale laboratory prototype.

1.6 Summary

In this chapter, the research scope of the thesis was outlined. Some of the main challenges and opportunities regarding PV power generation were pointed out, and typical approaches used as solutions to allow solar electric power generation were presented. The gaps and issues of such strategies were indicated and the use of impedance-source networks was adopted as an interesting candidate to mitigate some of these problems.

Among the many impedance-source networks available in the literature, the Quasi-Y Source network was chosen due to its convenient characteristics for a PV power generation application: Definition of voltage gains with reduced shoot-through periods, higher design flexibility, and the possibility to obtain continuous input current. In the next chapter, an overview

and details about the power processing architecture are discussed, such that the definition of practical design requirements for the QSY inverter can be specified.

2 Power processing architecture

The increasing penetration of DG, including PV inverters, and the presence of non-linear loads creates several power quality problems. To solve these issues, passive filters can be used since they are less expensive and effective in some cases (NADERI et al., 2020). However, this solution is not adaptative for different scenarios, depending on the load profile. Moreover, passive filters can create resonance problems with grid or PCC-connected loads. Active filters are an alternative to passive ones since they are more flexible and possess high compensation capability for both voltage and current (NADERI et al., 2018).

However, active filters are costly and are not designed to integrate active power into the grid. Instead, the multifunctional PV inverter can inject active power from a PV panel and realize ancillary services simultaneously, inheriting all the advantages of an active filter (GUO; XU, 2023). Yet, the type of ancillary service executed by the multifunctional PV inverter will require a specific connection to the PCC, which will directly affect the design of the converter. In this sense, the different kinds of arrangements related to multifunctional PV inverters are investigated.

2.1 Possible arrangements for multifunctional PV inverters

There are three connection arrangements for multifunctional PV inverters: a) Series; b) Parallel and c) Unified, as shown in Figure 2.1. In the series connection, the PV inverter behaves as a controlled voltage source, such that a controlled voltage is inserted in series with the grid phase voltage. This strategy presents a relatively complex control and design structure and is used to compensate for voltage-related power quality disturbances, such as harmonics, sags, and swells on the grid voltage (ANTUNES et al., 2018). The parallel arrangement relies on controlled currents that are injected into the grid by the PV inverter. This strategy presents a less complex control and design structure and is used to compensate power quality issues related to currents, such as current harmonics, non-active power, and phase unbalance (MARAFÃO et al., 2015)(QI et al., 2018).

Since many power quality problems are directly related to current, this strategy is commonly found in the literature. Finally, in the unified scheme, such as the unified power quality conditioner (UPQC) there is a simultaneous compensation of voltage and current disturbances, such that voltage sag/swell, harmonics and unbalance, and also currents harmonics and reactive power injection/absorption are possible in a single structure (HEENKENDA et al., 2023). Considering all the possible arrangements shown in Figure 2.1, the QSY inverter is thus designed in the parallel scheme, with a focus on compensating current-based power quality disturbances. The parallel or shunt connection is also typical in many grid-connected PV inverters. However,

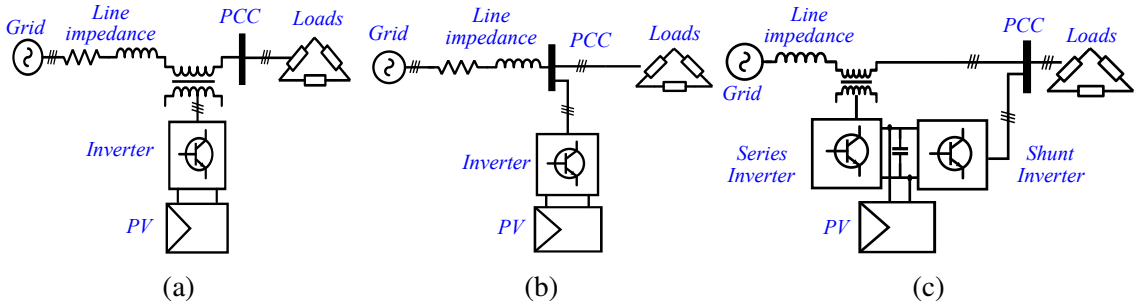


Figure 2.1 – Arrangements of multifunctional PV inverters: a) Series; b) Parallel; c) Unified.

there are several ways in which a PV power generation system connected in parallel to the grid can be designed, which depends among other factors, on the power processing level, number of PV arrays, the number of phases, grid frequency, and voltage levels of the grid. Therefore, an overview of the different PV power generation schemes is needed, such that a specific scenario in which the QSY inverter is applied can be defined, and its operational parameters can be determined.

2.2 Configuration of grid-connected PV inverters

Conventional PV inverters can be categorized into four types: central, string, multi-string, and AC modules. Each category presents different operational characteristics and is used in different power generation levels and applications (ZEB et al., 2018a), (JANA; SAHA; BHATTACHARYA, 2017), (BLAABJERG; IONEL, 2017). Figure 2.2 presents these different schemes for a three-phase/three-wire network, showing the power ratings, application scenarios, and the number of grid phases in which such strategies are used. In the AC module, there is a central module that contains all the functionalities of the PV power generation system in a single structure. Furthermore, an additional DC-DC converter can be used, depending on the application. In this way, the implementation and installation complexity is lower when compared to other strategies. Nonetheless, only a few hundred watts are generated with AC modules. There is also the possibility of using multiple DC modules, which are DC-DC power converters that integrate the power generated by single PV panels into the inverter DC link. Therefore, it is possible to apply individual MPPT in each PV panel.

Additionally, in the single-string scheme, multiple PV panels are connected in series and the power produced is processed by a single inverter. Both in DC-modules and single-string strategies, the power processed can reach 1 - 10 kW. On the other hand, the multi-string scheme inherits all the advantages of DC modules and string inverters and allows the delivery of more generated power, in the range of 10 - 30 kW. Finally, the central inverter is used when higher power generation levels are required. In this strategy, multiple PV panels are connected in series/parallel, and power diodes are placed in each string to allow the parallel connection between PV arrays. The total generated power is processed by a single, high-rating central

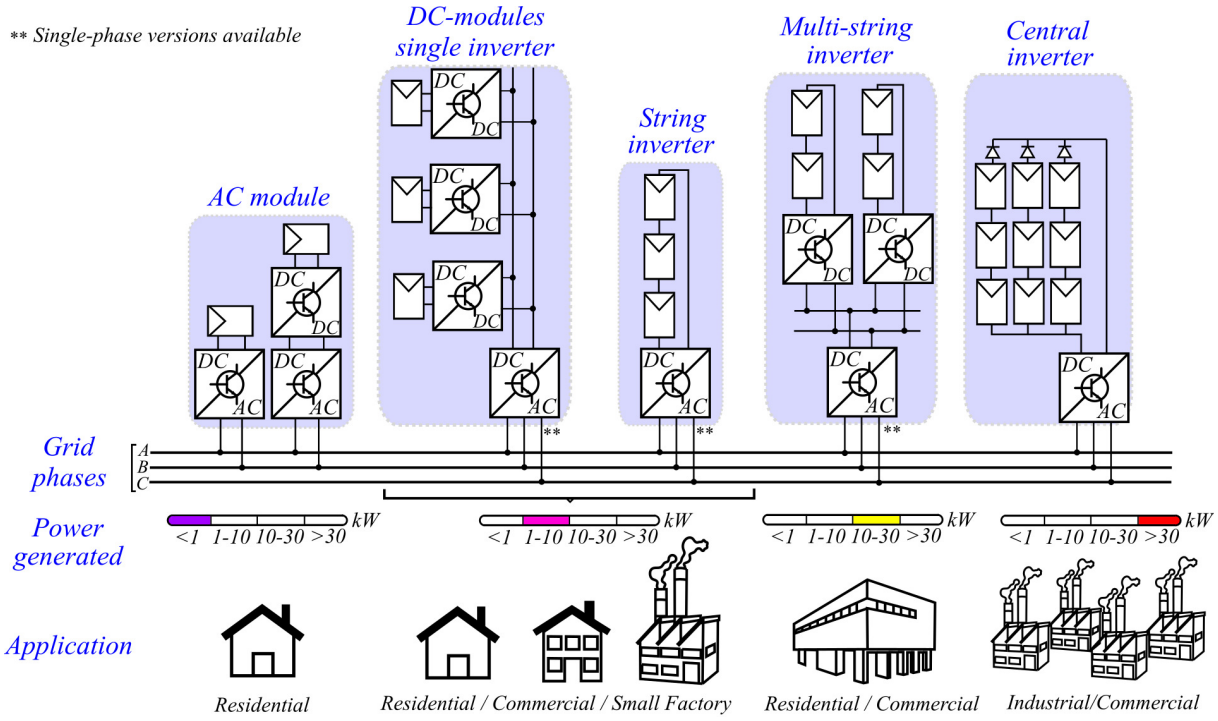


Figure 2.2 – PV generation architectures for different applications and power generation levels.

inverter. It is worth mentioning that the DC-module, string, and multi-string inverters are also available with single-phase versions.

Since the designed QSY inverter is a single-stage PV inverter, with a single voltage input and three-phase/three-wire topology, its PV inverter type is defined as string-inverter. In this sense, it is necessary to know the typical power ratings of such inverters, based on commercially available products, prior to designing the QSY network and specifying the inverter requirements.

2.3 QSY inverter requirements definition

Table 2.1 shows the main parameters of some three-phase PV inverters presently available in the market. It can be seen that most models have more than one MPP tracker, working with a multi-string strategy, which means that multiple PV strings can be connected to the same inverter with independent MPP tracking. As a conventional three-phase inverter has separate DC-DC converters to implement the MPPT algorithm, this feature means that more than one DC-DC converter is present at the inverter DC-side.

Some works in the literature propose MPPT schemes with impedance-source networks that allow the insertion of two PV strings in the same impedance network, inserting one string at the input side and another in parallel with a capacitor located in the network (LASHAB et al., 2019). In this work, it is adopted the single string strategy with the QSY inverter, and future studies can be done considering multiple MPP trackers within the impedance network. All the inverters listed in Table 2.1 deliver a line-to-line voltage between 230-415 V, in a three-phase

Table 2.1 – Commercial three-phase PV inverters parameters.

Manufacturer	Model	No. MPP trackers	Output voltage (V_{ac-rms}) @ 3~EN 50/60 Hz	Nominal power (kW)	Max. efficiency (%)	Volume (m^3)	Voltage range Vin/Vmppt (V)	Nominal Input Voltage (V)	Max. input current (A)	Nominal AC output current (A)	THD_i (%)	PF (lead/lag)
Fronius	Gen 24 Symo	2	400/230 380/220	3-10	98.2	0.04	80-1000 / 80-800	610	12.5 - 25	4.5 - 14.5	3.5	0.7 - 1
SolarEdge	SE Hybrid	1	400/230	5-10	97.8	0.06	375-450	-	14 -28	8 - 16	-	-
Sungrow	SG-RT	2	380/220 400/230 415/240	5-20	98.5	0.035	180-1100 / 160-1000	600	12.5 - 25	8.3 - 31.9	3	0.8 - 1
SolaX	X3 Hybrid HV	2	400	5-10	97.6	0.06	230-1000 / 230 - 800	720	11 - 20	7.6 - 15	2	0.8 - 1
Goodwe	ET Series	2	400/380	5-10	98	0.038	180-1000 / 200-850	620	12.5	8.5 - 16.5	3	0.8 - 1
Growatt	SPH Series	2	220	3-6	97.5	0.048	150-1000 / 150-550	360	12	7.5 - 15	3	1
Kostal	PLENTICORE Plus	3	400/230	3-10	97.2	0.053	120-1000 / 140-720	570	13	4.33 - 14.43	3	1
PHB	PHB13KT-DT	2	380/220	13	98.3	0.023	160-1000 / 180-850	-	12.5 - 25	20.3	3	0.8 - 1

four-wire, or three-wire schemes at 50/60 Hz. In this sense, the QSY inverter is designed to deliver 220 V line-to-line voltage in a three-phase three-wire distribution network at 60 Hz. In the inverters of Table 2.1, the nominal output power range varies from 3-20 kW. Moreover, the minimum and maximum input voltage levels with MPPT vary from 140-1000 V [1] with a nominal voltage input ranging from 360-720 V. This means that most three-phase PV inverters can deliver high-efficiency power conversion (>97%) at the nominal voltage in the input stage. Moreover, lower nominal voltages are not desired due to the increase in current ratings, and the expected increase in cable costs, maintenance, and installation.

Taking all the previous comments into consideration, for the development of a QSY inverter with commercially viable characteristics: a) The nominal output power is defined as 3 kW, but it is supposed that the inverter can handle up to 3.75 kVA when ancillary services are executed; b) The admitted input voltage range varies from 200-1000 V with MPPT; c) The nominal input voltage is defined as 250 V with a maximum input current of 12 A. Finally, the output-rated current is defined at 7.9 A_{rms} at 3 kW - 220 V line voltage, with the total harmonic current distortion ($THDi$) lower than 3%.

Considering the reactive power compensations characteristics foreseen in IEEE 1547-2018, it is adopted that the QSY-inverter is a category A DER, which means that it covers the minimum performance capabilities needed for Area APS voltage regulations and it is adequate for applications where the DER penetration in the distribution system is lower, not being subject to frequent large power output variation (IEEE, 2018). As such, the inverter should have the minimum capability of delivering 44% of rated apparent power as reactive power and absorbing 25% of apparent power as reactive power. Hence, the power factor definition for the QSY inverter should vary in the range of 0.9-1.0 leading/lagging. Another important aspect to be covered is related to DC link voltage requirements to allow power injection into the grid and the execution of ancillary services if required. Since the QSY inverter has the flexibility of operating with a variable DC link and complying with different ancillary requisitions, the DC link voltage range

[1] Except Fronius Gen 24 Symo, which allows a minimum voltage of 80 V with MPPT

is fixed at 400-600 V. The maximum DC link voltage value $V_{DC\,max}$ is related to overvoltages due to stray or leakage inductance, and it is a project parameter to design the LCD regenerative snubber for the DC link. Considering a maximum deviation of 35% from the maximum DC link value, $V_{DC\,max}$ is defined as 745 V. Now, to allow the shoot-through conduction, conventional sinusoidal pulse-width modulation techniques (SPWM) must be modified. There are several schemes available in the literature, both based on control carriers and space-vector approaches, including Simple Boost modulation (SBC), Maximum Boost Modulation (MBC), and Maximum Constant Boost Modulation (MCBC) (SANTOS; GONÇALVES, 2021).

Regardless of the scheme, the shoot-through conduction often occurs twice at every switching period, which means that the shoot-through frequency is defined as $f_{st} = 2f_s$, where f_s is the AC modulation switching frequency. Now, if the inverter PWM control signals are used to trigger the Digital Signal Controller (DSC) Analog-to-Digital converter (ADC), the number of samples acquired at grid frequency is an integer, both in single update or double update schemes. Moreover, if the three-phase inverter is comprised of IGBT switches, with a frequency range normally defined up to 36 kHz, it is defined that f_{st} is given by 36 kHz which means that f_s is 18 kHz. Hence, if the inverter PWM is configured to be in double-update mode, the ADC can acquire 300 samples (sampling frequency of 18 kHz) for signals at 60 Hz. Such sampling frequency is acceptable for IGBT operation both during active and shoot-through states, PLL implementation, and AC side current control strategies (SIMÕES; FARRET, 2016) besides being sufficient to handle the DC and AC sides control loops separately.

Lastly, PV inverters may require galvanic isolation between PV and the grid. With impedance-source networks, this strategy can be implemented through topology modifications and control schemes (BRADASCHIA et al., 2011), (GUO et al., 2018). In this work, however, galvanic isolation will not be covered and it will be the focus of future studies since the main goal of this design is to validate the concept of QSY-based inverter as a multifunctional PV inverter. Considering all the previous comments, the general parameters of the QSY inverter are presented in Table 2.2. With the parameters defined, it is now possible to design the QSY network elements, which is the main scope of the next chapter.

Table 2.2 – Proposed Quasi-Y Source solar PV multifunctional inverter parameters.

Model	**No. MPP trackers**	**Output voltage (V_{ac-rms}) @ 3∼EN 60 Hz**	**Nominal power (kW)**	**Voltage range V_{in} & V_{mppt} (V)**	**Nominal Input Voltage (V)**	**Max. input current (A)**	V_{DC}	V_{DCmax}	f_s, f_{st} **(kHz)**	**Nominal AC output current (A)**	THD_i **(%)**	**PF (lead/lag)**
Quasi-Y Source inverter	1	220	3	80-1000	250	14	400-600	745	18, 36	7.5	<3	0.9-1

2.4 Summary

In this chapter, the power processing architecture in which the QSY inverter was implemented was discussed and defined. Therefore, it was indicated that the QSY inverter would

operate in parallel connection, in a three-phase/three-wire configuration connected to the PCC. Moreover, a string-type inverter was considered, aiming at commercial or small-factory environment applications. Evaluating commercial three-phase PV inverter parameters, with power ratings compatible with the intended application, the specifications of the QSY inverter were defined and justified. With these parameters defined, it is possible to design the QSY inverter.

3 Quasi-Y network design

In this chapter the QSY network is designed based on the application requirements specified in Chapter 2. Figure 3.1 shows the complete schematic of the QSY network. It should be noted that the LCD regenerative snubber and diode D voltage damping RC snubber are also present since they are required to operate the QSY inverter at the ratings given in Table 2.2, considering practical overvoltage issues caused by stray inductances. The equivalent series resistances (ESR) of each component are also considered. Since the snubber components' ESR impact on QSY network operational stages are negligible, they are not considered in Figure 3.1. In the next sections, the design methodology adopted to specify all converter components is presented. Note that the presence of snubber circuits does not change significantly the QSY inverter operational stages, and they are omitted during the derivation of the mathematical expressions.

3.1 Impedance network elements design

The design of the impedance network begins with the steady-state analysis. As such, the following assumptions are considered: a) The coupled inductors leakage inductances are negligible due to a tight magnetic coupling; b) The power switches S_w and D have ideal commutation; c) The converter operates in continuous conduction mode (CCM); d) All passive elements are linear, time-invariant and frequency independent. Furthermore, considering the waveforms depicted in Figure 1.4 and the equivalent circuits during shoot-through and active

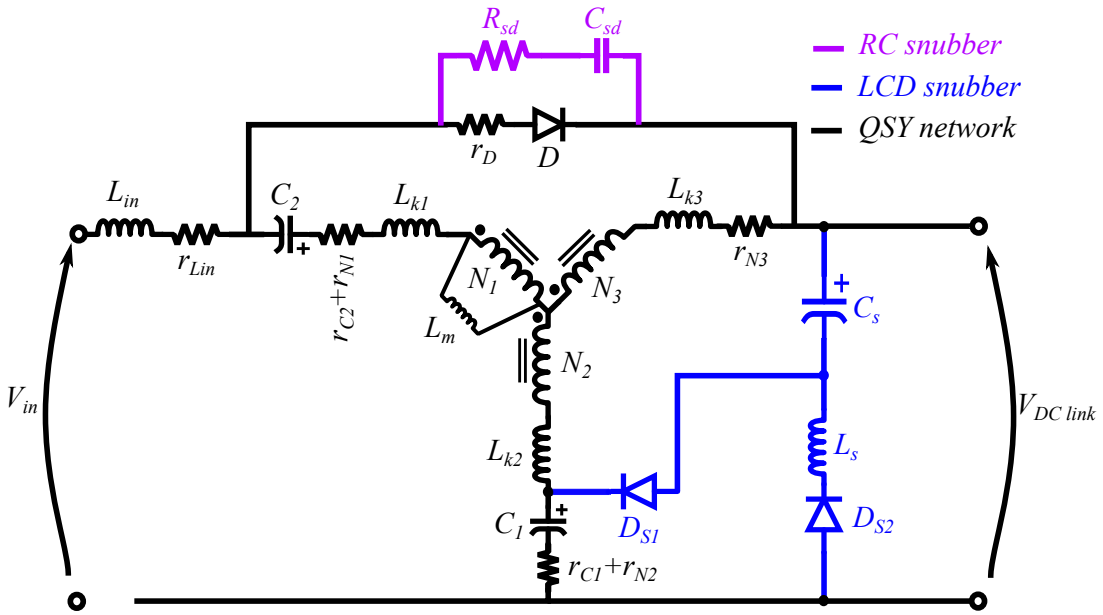


Figure 3.1 – Quasi-Y network complete configuration, including snubber circuits.

states given in Figure 1.5, expressions of design interest can be derived for the components of the QSY network. Table 3.1 presents a summary of the obtained expressions (SANTOS et al., 2023), whose terms are defined through sections 3.1.1-3.1.6.

Table 3.1 – Design expressions for the QSY Impedance Network Components.

Component	**Expression**
L_{in}	$\frac{V_{in}^2(1-B\delta')D_{st}}{f_{st}P_o k_{Lin}}$
L_m	$\frac{N_1^2\mu_0\mu_r A}{l}$
C_1	$\frac{\lvert\delta'\rvert D_{st}P_o}{V_{DC\,link}D'_{st}f_{st}k_{C1}V_{in}}$
C_2	$\frac{P_o}{V_{DC\,link}\lvert\delta'\rvert f_{st}k_{C2}V_{in}}$
R_o	$\frac{V_{DC\,link}^2(1-D_{st})}{P_o}$

3.1.1 Derivation of V_{C1} and V_{C2}

Prior to obtaining the design equations of the QSY network, expressions for V_{C1} and V_{C2} need to be obtained. Applying Kirchhoff's Voltage Law (KVL) energy balance criterium on the circuit depicted in Figure 1.5a, the expression for N_1 winding voltage in the shoot-through state $V_{N1.st}$, can be approximated as (3.1). In the same way, but considering the circuit shown in Figure 1.5b the N_1 winding voltage in the active state $V_{N1.a}$ can be written as (3.2). Now, considering the energy balance criterion (Volts.s) balance in the winding with N_1 turn-ratio, an expression for the average voltage $\overline{V_{N1}}$ can be written as (3.3). Hence, substituting (3.1)-(3.2) in (3.3) one can derive (3.4) which express the relationship between V_{C1} and V_{C2}.

$$V_{N1.st} = V_{C1}\left(\frac{N_1}{N_3 - N_2}\right) \tag{3.1}$$

$$V_{N1.a} = V_{C2}\left(\frac{N_1}{N_1 + N_3}\right) \tag{3.2}$$

$$\overline{V_{N1}} = \frac{V_{N1.st}D_{st}T_s + V_{N1.a}(1-D_{st})T_s}{T_s} = 0 \tag{3.3}$$

$$\frac{V_{C2}}{V_{C1}} = \frac{N_1 + N_3}{N_2 - N_3}\left(\frac{D_{st}}{1-D_{st}}\right) \tag{3.4}$$

However, both in active and in the shoot-through state, applying KVL on the input stage loop, one can obtain (3.5). The average expression of (3.5) can be given by (3.6), which reveals

the relationship between the averaged values of $V_{C1}(t)$ and $V_{C2}(t)$, which are very similar to its instantaneous values due to the low voltage ripple content.

$$V_{in} - V_{Lin} + V_{C2} - V_{N1}\left(\frac{N_1 + N_2}{N_1}\right) - V_{C1} = 0 \tag{3.5}$$

$$V_{C2} = V_{C1} - V_{in} \tag{3.6}$$

Finally, substituting (3.6) in (3.4) the equations for V_{C1} and V_{C2} can be obtained by (3.7)-(3.8).

$$V_{C1} = \frac{V_{in}(1 - D_{st})}{1 - D_{st}\delta} \tag{3.7}$$

$$V_{C2} = \frac{V_{in}D_{st}|\delta'|}{1 - D_{st}\delta} \tag{3.8}$$

3.1.2 Derivation of L_{in}

The V_{Lin} expression can be written as (3.9). In steady-state, during the shoot-through period and considering the waveform of $I_{Lin}(t)$ shown in Figure 1.4, $\frac{dI_{Lin}}{dt}$ can be written as (3.10), where $I_{Lin-min}$ is the minimum value of $I_{Lin}(t)$.

$$V_{Lin} = L_{in}\frac{dI_{Lin}}{dt} \tag{3.9}$$

$$\frac{dI_{Lin}}{dt} = \frac{\Delta I_{Lin}}{\Delta t} = \frac{\hat{I}_{Lin} - I_{Lin-min}}{D_{st}T_s} \tag{3.10}$$

For simplicity, considering a large enough inductance, ΔI_{Lin} can be approximated by a fraction of the average value of the input current $\overline{I_{Lin}}$, through the use of a current ripple factor k_{Lin}, hence $\Delta I_{Lin} = k_{Lin}\overline{I_{Lin}}$, where $\overline{I_{Lin}} = \frac{P_o}{V_{in}}$, being P_o the converter output power, neglecting power loss. Therefore, considering the previous comments, one can obtain (3.11). Now, substituting (3.7), (3.8), (3.1) in (3.5), the L_{in} voltage during shoot-through $V_{Lin.st}$ can be given by (3.12). Finally, applying (3.11) and (3.12) in (3.9) L_{in} can be obtained as (3.13), where f_{st} is the shoot-through frequency.

$$\frac{\Delta I_{Lin}}{\Delta t} = \frac{\overline{I_{Lin}}k_{Lin}}{D_{st}T_s} = \frac{P_o k_{Lin}}{V_{in}D_{st}T_s} \tag{3.11}$$

$$V_{Lin.st} = V_{in}(1 - B\delta') \tag{3.12}$$

$$L_{in} = \frac{V_{in}^2(1 - B\delta')D_{st}}{f_{st}P_o k_{Lin}} \tag{3.13}$$

Considering that the inductor is designed to operate at nominal power levels, it is possible to identify the minimum power processed at the output that would lead the operation to the discontinuous mode. Hence, to ensure continuous conduction mode at the input stage, $I_{Lin-min}$ should be greater than 0 A. This condition is mathematically described by (3.14). Solving (3.14) for k_{Lin}, one can find that k_{Lin}= 2 is the required value for critical conduction mode, that is, $I_{Lin-min}$= 0 A. Now, assuming that all variables in expression (3.13) are constant, except P_o, it is possible to define through (3.15) the minimum output power P_{o-min} that is needed to obtain continuous conduction mode at the input, considering that k_{Lin}= 2, where η is converter efficiency.

$$\overline{I_{Lin}}(1 - \frac{k_{Lin}}{2}) > 0 \tag{3.14}$$

$$P_{o-min} = \frac{V_{in}^2(1 - B\delta')D_{st}\eta}{2f_{st}L_{in}} \tag{3.15}$$

3.1.3 Derivation of L_m

Considering that the coupled-inductor core can be treated as a uniform magnetic circuit, that is, the air-gap reluctance is incorporated in the core body, the expression of the equivalent reluctance $\mathscr{R}$ is given by (3.16), where l is the mean length of the magnetic circuit, μ_o is the air magnetic permeability, μ_r is relative magnetic material permeability and A is the core cross-section area. Now, the magnetizing inductance L_m is classically defined by (3.17) (WITULSKI, 1995), and is related to core's reluctance $\mathscr{R}$ and the number of windings N_1, which is the coupled-inductor energy input coil [1].

$$\mathscr{R} = \frac{l}{\mu_o\mu_r A} \tag{3.16}$$

$$L_m = \frac{N_1^2}{\mathscr{R}} = \frac{N_1^2\mu_o\mu_r A}{l} \tag{3.17}$$

3.1.4 Derivation of C_2

The current and voltage associated with C_2 are related by (3.18), considering the shoot-through state and using the same methodology adopted in the L_{in} design, such that $\frac{dV_{C2}}{dt} \approx \frac{\Delta V_{C2}}{D_{st}T_s}$ and $\Delta V_{C2} = k_{C2}V_{C2}$ [2]. However, during the shoot-through state, $I_{C2} = I_{Lin}$, as can be inferred by the circuit shown in Figure 1.5a. Assuming that $I_{Lin} \approx \overline{I_{Lin}} \approx \frac{P_o}{V_{in}}$, isolating C_2 in (3.18) and considering (3.8), one can obtain (3.19).

[1] Currently, the author is working to develop a more complete L_m design methodology, which considers lower core power losses and reduced operation temperature. However, the statements made in this section can be followed as general guidance to design L_m.

[2] Similarly to k_{Lin}, k_{C1} and k_{C2} are used to relate the ripple voltages $\Delta V_{C2}, \Delta V_{C1}$ with the voltage values V_{C1}, V_{C2}, respectively. Note that due to the low voltage ripple content, $V_{C1} \approx \overline{V_{C1}}$ and $V_{C2} \approx \overline{V_{C2}}$.

$$I_{C2} = C_2 \frac{dV_{C2}}{d_t} = C_2 \frac{k_{C2} V_{C2}}{D_{st} T_s} \tag{3.18}$$

$$C_2 = \frac{P_o}{V_{DC\,link} |\delta'| f_{st} k_{C2} V_{in}} \tag{3.19}$$

3.1.5 Derivation of C_1

The current and voltage association with C_1, given by (3.20), is similar to (3.18), considering the shoot-through state and using the same methodology adopted in the L_{in} design, such that $\frac{dV_{C1}}{dt} \approx \frac{\Delta V_{C1}}{D_{st} T_s}$ and $\Delta V_{C1} = k_{C1} V_{C1}$. As reported in (FOROUZESH et al., 2016), the windings and currents of each coupled-inductor coil are related by (3.21). Applying KCL on the coupled inductors, one can derive (3.22). Despite the fact that $I_{C2} = I_{N1} + I_m$, considering a large enough magnetizing inductance L_m, I_m is comparatively lower than I_{N1} in steady state and hence during shoot-through $I_{C2} \approx I_{N1}$. Therefore, by substituting (3.20) for (3.22), it is possible to derive expressions for I_{N3} and I_{N2} with respect to I_{N1} and I_{C2}, as can be seen in (3.22) and (3.23).

$$I_{C1} = C_1 \frac{dV_{C1}}{d_t} = C_1 \frac{k_{C1} V_{C1}}{D_{st} T_s} \tag{3.20}$$

$$N_1 I_{N1} = N_2 I_{N2} - N_3 I_{N3} \tag{3.21}$$

$$I_{N2} = I_{N3} - I_{N1} \tag{3.22}$$

$$I_{N3} = I_{N1} \delta \approx I_{C2} \delta \tag{3.23}$$

$$I_{N2} = I_{N1} |\delta'| \approx I_{C2} |\delta'| \tag{3.24}$$

Since $I_{C1} = I_{N2}$ then, isolating C_1 in (3.20) and considering (3.7), it is possible to obtain (3.25) [3].

$$C_1 = \frac{|\delta'| D_{st} P_o}{V_{DC\,link} D'_{st} f_{st} k_{C1} V_{in}} \tag{3.25}$$

3.1.6 Determination of R_o and L_o

The determination of R_o, which is used to represent the load connected at the inverter output in the equivalent circuits depicted in Figure 1.5, is based on the AC load power consumption P_o, the value of the RMS DC link voltage $V_{DC\,link-rms}$ and D_{st}. Hence, R_o is

[3] Besides the capacitance values of C_1 and C_2, it is also important to define the correct constructive material type. Considering the waveforms signatures of I_{C1} and I_{C2}, shown in Figure 1.4, the designer may choose to work with a composition of film and electrolytic capacitors, for example, to mitigate reliability issues associated with high-frequency current ripple. Other solutions may be employed as well, but this discussion is beyond the objectives of this section.

derived by (3.26). On the other hand, if the inverter has output filter inductances, L_o has the same value of such filter inductances.

$$R_o = \frac{V_{DC\,link-rms}^2}{P_o} = \frac{V_{DC\,link}^2(1-D_{st})}{P_o} \tag{3.26}$$

3.2 Electrical quantities expressions for the QSY converter

Through the analytical description of the characteristic waveforms depicted in Figure 1.4, and applying Kirchhoff voltage (KVL) and current (KCL) laws to the equivalent circuits depicted in Figure 1.5, considering inductor voltage and capacitor charge balance, the main voltage and current expressions for the QSY network are derived and shown in Table 3.2. For a generic quantity x, its root-mean-square (RMS) value is identified as x_{rms}, mean and peak values by $\overline{x}$ and $\hat{x}$, respectively. It should be noted that the converter efficiency η, for a conservative design, could be defined in the range of $0.8 \leq \eta \leq 0.985$ [4]. The auxiliary design factor σ' is used to approximate the derived results to more realistic scenarios, considering the converter's non-ideal behavior, and is recommended to adopt σ'=1.1.

Table 3.2 – Set of expressions related to the main electrical quantities in the QSY converter.

Variable	Expression	Variable	Expression
$\hat{I}_{Lin}, \hat{I}_{C2}$	$\overline{I_{Lin}}(1+\frac{k_{Lin}}{2})$	I_{N1rms}	$\approx I_{C2rms}$
$\overline{I_{Lin}}$	$\frac{P_o}{V_{in}\eta}$	$\hat{V}_{C1}$	$\overline{V_{C1}}(1+\frac{k_{C1}}{2})$
I_{Linrms}	$\overline{I_{Lin}}\sqrt{1+\frac{k_{Lin}^2}{12}}$	$\bar{V_{C1}}, V_{C1rms}$	$V_{in}BD'_{st}$
$\hat{V}_{Lin}$	$V_{in}(B-1)\frac{D'_{st}}{D_{st}}$	I_{C1rms}	I_{N2rms}
$\overline{I_{N1,2,3}}$	0	$\hat{I_D}$	$\overline{I_{Lin}}\sigma'\left(1+\frac{k_{Lin}}{2}+\frac{2D_{st}}{D'_{st}}\right)$
I_{C2rms}	$\overline{I_{Lin}}D_{st}\sqrt{\frac{k_{Lin}^2D'_{st}+4(D_{st}+3)}{12D_{st}D'_{st}}}$	$\overline{I_D}$	$\overline{I_{Lin}}$
$\hat{I}_{N2}$	$\hat{I_{Lin}}\lvert\delta'\rvert\sigma'$	I_{Drms}	$\frac{\overline{I_{Lin}}}{2\sqrt{3}}\sqrt{\frac{16}{D'_{st}}+(k_{Lin}-2)(k_{Lin}D'_{st}+2(D_{st}+1))}$
I_{N2rms}	$I_{C2rms}\lvert\delta'\rvert$	$\hat{V_D}$	$\frac{V_{in}}{\delta D_{st}}(\delta - D'_{st}(1+B(\delta D_{st}-\delta')))$
$\hat{I}_{N3}$	$\hat{I_{Lin}}\delta\sigma'$	I_{Swrms}	$\overline{I_{Lin}}\delta k_{Lin}\sqrt{\frac{D_{st}}{3}\left(\frac{\sigma'^2-\sigma'+1}{4}+\frac{\sigma'^2(k_{Lin}+1)+\sigma'-k_{Lin}+1}{k_{Lin}^2}\right)}$
I_{N3rms}	$I_{C2rms}\delta$	$\hat{I_{Sw}}$	$\hat{I}_{N3}$
$\hat{V}_{C2}$	$\overline{V_{C2}}(1+\frac{k_{C2}}{2})$	$\bar{I_{Sw}}$	$\frac{\overline{I_{Lin}}D_{st}\delta}{4}(\sigma'(2+k_{Lin})+2-k_{Lin})$
$\overline{V_{C2}}, V_{C2rms}$	$V_{in}(BD'_{st}-1)$	$\hat{V}_{Sw}$	$V_{in}B$
$\hat{V}_{N1}$	$V_{in}\left(\frac{N_1}{N_1+N_2}\right)\left(\frac{D'_{st}(1-B)}{D_{st}}\right)$	$\hat{V}_{N2}, \hat{V}_{N3}$	$\frac{N_2}{N_1}\hat{V}_{N1}, \frac{N_3}{N_1}\hat{V}_{N1}$

[4] The values shown in Table 3.5 were obtained by adopting η=90%, with the objective to achieve a reasonable safety margin. The designer may define other values for η based on different criteria.

3.3 Design parameters for the Quasi-Y network

As the nominal voltage of the QSY inverter is 250 V, the QSY network is designed to deliver maximum voltage gain and power at this input voltage (600 V and 3 kW, respectively, with B=2.4 and ideal D_{st}=0.1944). Furthermore, the δ factor is critical for the impedance-network design. Figure 3.2 show the voltage stress at different components of the QSY network in p.u, with the base value being the nominal input voltage V_{in}=250 and V_{sw} indicates the voltage stress at the inverter switches. As can be seen in Figure 3.2, as δ increases, the required D_{st} decreases to attain the same B, but higher voltage stress is experienced by power switches. If δ=2, then B is similar to the conventional Z-Source network, which does not allow better exploitation of the proposed topology in terms of voltage gain.

However, if δ>4, then higher voltage stress issues arise. In this sense, defining δ=3 offers a good compromise between achieving the boost advantages of the proposed topology without excessive voltage stress. There are several windings proportions that can be used to obtain δ=3, and in this work, the 1:5:3 configuration is used. Considering the parameters presented in Table 2.2 and the previous comments, in Table 3.3 it is shown the impedance network project parameters, that are based on nominal values [5]. Furthermore, considering the expressions given in Table 3.2, the following variables are calculated and shown in Table 3.4: i) L_{in}, considering continuous-conduction mode; ii) C_1 and C_2; iv) Equivalent series resistance values (ESR) r_{Lin}, r_{C1}, r_{C2}, r_D based on typical practical values; v) Load resistance R_o. The values of $r_{N1,N2,N3}$, L_m and N_1:N_2:N_3 (and δ) are obtained based on practical values, such as those presented in Appendix A for different coupled-inductors available in the laboratory. The values of k_{Lin}, k_{C1} and k_{C2} shown in Table 3.3 were chosen such that minimum values of L_{in}, C_1 and C_2 are obtained, considering that the shoot-through frequency is already defined. Using the expressions given in Table 3.2 the electrical quantities of the QSY inverter are calculated and shown in Table 3.5. Notice that the calculated values shown in Table 3.5 does not consider the additional current or voltage stresses caused by leakage inductances.

Table 3.3 – Quasi-Y impedance network project parameters.

V_{in}	$V_{DC\,link}$	P_o	B	δ	N_1:N_2:N_3	D_{st}	k_{Lin}	k_{C1}	k_{C2}
250 V	600 V	3 kW	2.4	3	1:5:3	0.1944	50%	0.1%	5%

In the next sections, the issue of snubbers design for the QSY network is covered to mitigate problems related to overvoltages caused by stray inductances that are unavoidable present in the real converter.

[5] Due to the flexible DC link characteristics, the QSY inverter could operate with different values of $V_{DC\,link}$, if the converter components voltages and currents in this cases respect the limits shown in Table 3.5.

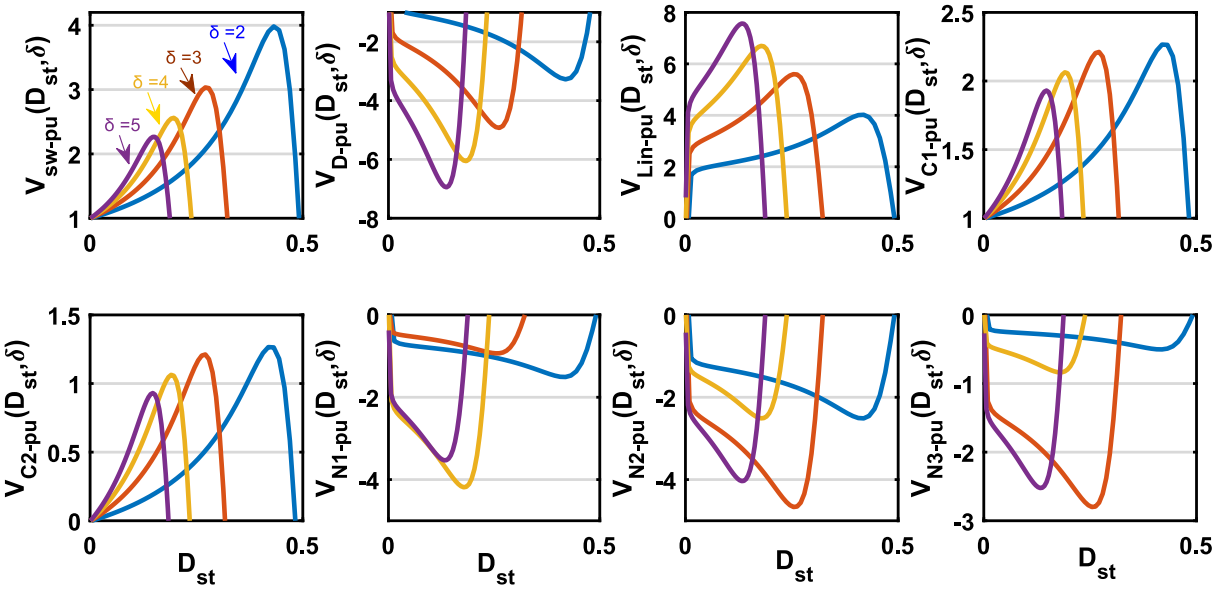


Figure 3.2 – Voltage stress at different components of the QSY network for different δ.

Table 3.4 – QSY converter circuit parameters.

Component	Value	Component	Value
L_{in}	1.3 mH	r_{Lin}	0.35 Ω
C_2	5.56 μF	r_{C2}	10 mΩ
C_1	268 μF	r_{C1}	10 mΩ
r_D	25 mΩ	$r_{N1,N2,N3}$	6, 30, 18 mΩ
L_m	0.217 mH	N_1:N_2:N_3	37:186:112
δ	3	D_{st}	0.1944

3.4 RC and LCD snubber designs

Due to nonideal inductances present in the QSY network, overvoltage issues occurs with D and S_w. In this section, a brief description of the possible solutions to this problem is given.

3.4.1 RC snubber

Figure 3.3 shows the nonideal inductance and capacitance that are present in the QSY converter. The QSY network diode D has parasitic capacitance C_{Dp}, that can be modeled in parallel with the anode-cathode terminals. Moreover, series resistance R_D and depletion layer voltage, which is modeled as V_{Df}, are also used to represent the nonideal behavior of D. Furthermore, equivalent stray inductances L_{k1-k7} and capacitance C_k can be used to model the nonideal behavior of other elements that comprise the QSY network and directly affect the voltage stress across D. The interaction between these nonideal inductances and capacitance produces unwanted voltage resonance due to the series RLC network, which may damage the diode D due to overvoltage.

One classical solution to this issue involves the utilization of a passive snubber circuit

Table 3.5 – Calculated electrical quantities for QSY inverter.

Variable	Value	Variable	Value
$\hat{I}_{Lin}, \hat{I}_{C2}$	17 A	I_{N1rms}	7 A
$\overline{I_{Lin}}$	13 A	$\hat{V}_{C1}$	484 V
I_{Linrms}	14 A	$\bar{V_{C1}}, V_{C1rms}$	483 V
$\hat{V}_{Lin}$	1450 V	I_{C1rms}	14 A
$\overline{I_{N1,2,3}}$	0 A	$\hat{I}_D$	25 A
I_{C2rms}	7 A	$\overline{I_D}$	13 A
$\hat{I}_{N2}$	37 A	I_{Drms}	15 A
I_{N2rms}	14 A	$\hat{V}_D$	-1200 V
$\hat{I}_{N3}$	55 A	I_{Swrms}	19 A
I_{N3rms}	20 A	$\hat{I_{Sw}}$	55 A
$\hat{V}_{C2}$	239 V	$\bar{I_{Sw}}$	8 A
$\overline{V_{C2}}, V_{C2rms}$	233 V	$\hat{V}_{Sw}$	600 V
$\hat{V}_{N1}$	-242 V	$\hat{V}_{N2}, \hat{V}_{N3}$	-1208 V, -726 V

based on an RC network. Nonetheless, an unwanted power loss will occur, despite the overvoltage damping. Currently, further studies are being carried out to solve this issue. For instance, the design of an RC snubber is done somewhat empirically, but complementary methodologies can aid the design process (RIDLEY, 2005b). Figure 3.4a shows the V_D waveform obtained through

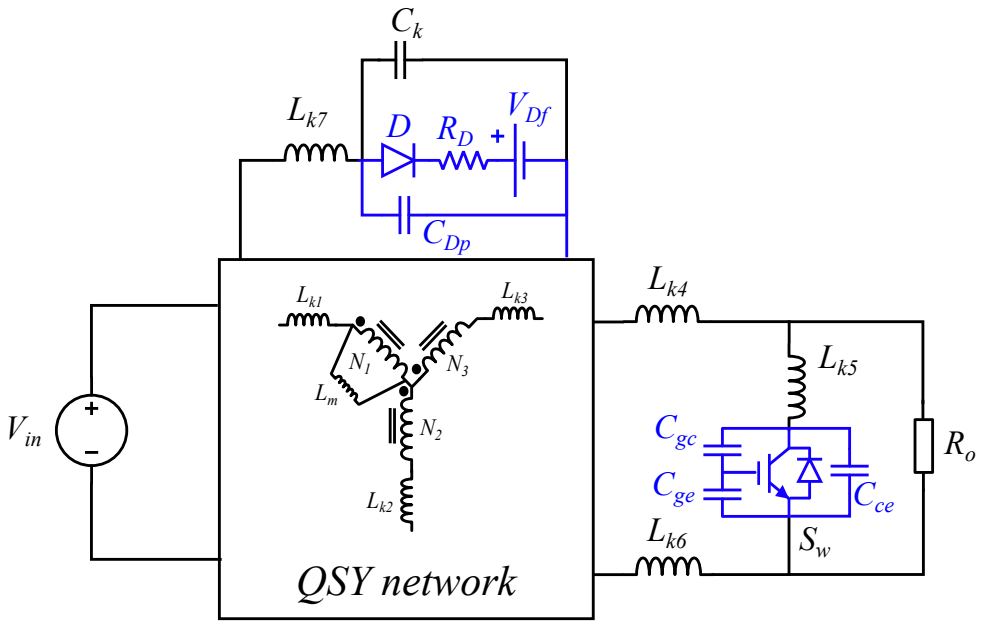
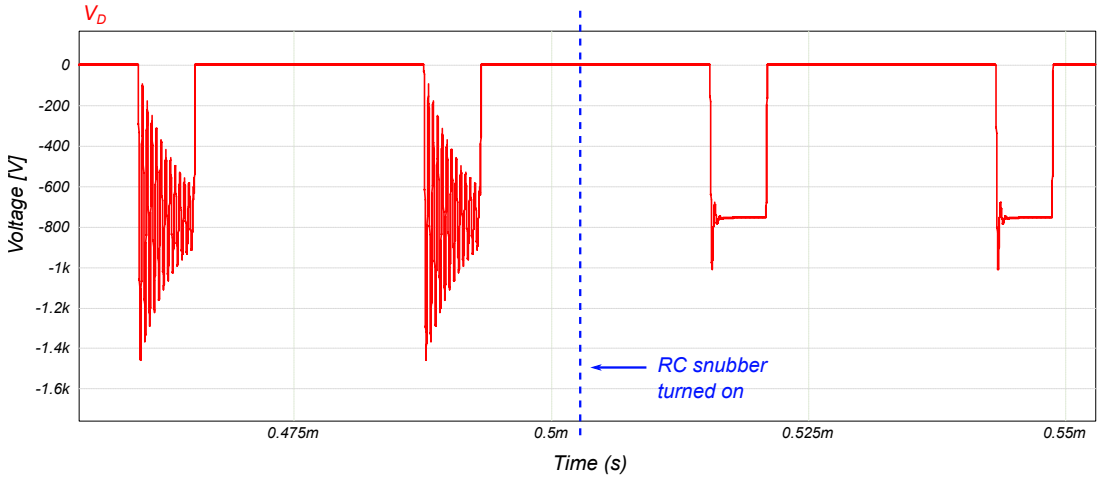
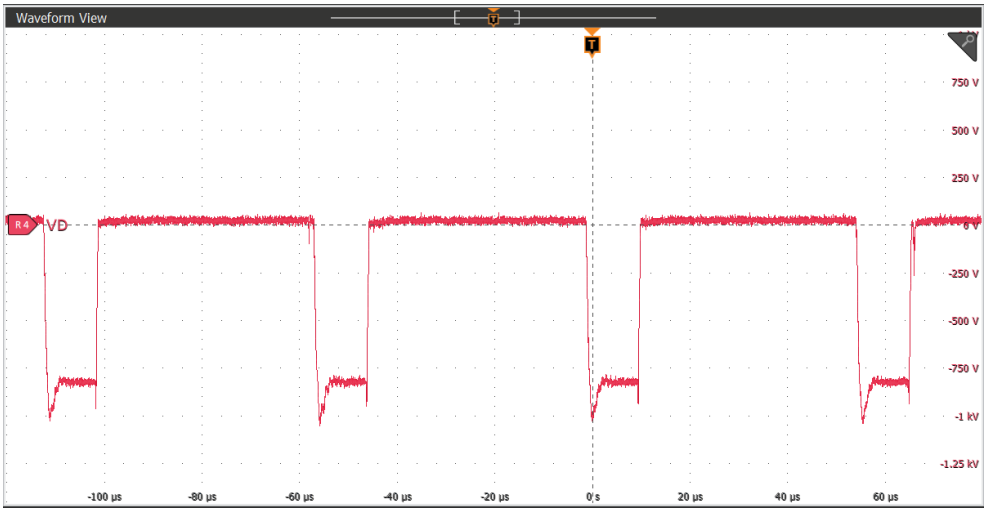


Figure 3.3 – Equivalent circuit showing the stray inductances and capacitance in the QSY inverter. Power switches nonideal elements are shown in blue.



(a)



(b)

Figure 3.4 – Waveforms of voltage ringing at D due to resonance caused by nonideal equivalent capacitances and inductances: a) Simulation; b) Experimental.

simulations, before and after the insertion of the RC snubber across D. In this case, the values of stray inductances were defined empirically. It can be seen that the overvoltage was effectively damped from -1440 V to -1000 V. Figure 3.4b shows a practical waveform of V_D, which is damped with an RC snubber designed with R_{sd} = 270 Ω and C_{sd} = 4 nF, with a peak voltage of 1 kV.

3.4.2 Regenerative LCD snubber

The DC link overvoltage issues also arise due to the interaction of inductances L_{k1-7} during the transition of shoot-through state to active state. Basically, during the shoot-through state energy is stored at the leakage inductances (S_w is turned on). At the transition to the active state, this stored energy is returned to the system as overvoltage, due to large d_i/d_t. There are several solutions to this issue, involving the utilization of new topologies, active and passive snubbers, with and without regenerative features. Table 3.6 presents a non-exhaustive list of

found solutions in the literature for magnetically coupled impedance source (MCIS) inverters, including its references, showing: a) The type of solution - either topology modification (Tp), passive snubber (PSN) or active snubber (ASN); b) Number of devices employed, in terms of inductors (L), capacitors (C), diodes (D) and transistors (T); c) Device ratings, where *** and * means higher or lower ratings, respectively; d) Number of operational stages; e) Regenerative capability; f) Common ground feature; g) Possibility of extending such solution to other types of impedance network (generic solution); h) Continuous input current characteristics and i) Zero magnetizing current.

Table 3.6 – Solutions to DC link overvoltage in Y-source based MCIS inverters.

Solution	References	Type	# (L, C, D, T)	Device ratings	# Op. stages	R	CG	G	CIC	ZMC
Voltage-double YSI	(JI et al., 2017)	Tp	0, 1, 2, 0	***	4	-	✓	-	✓	✓
DC-rail clamping	(CHA; LI; PENG, 2016)	Tp	0, 0, 1, 0	***	-	-	✓	-	✓	-
Low-spike Y-source	(LIU et al., 2019)	Tp	0, 1, 1, 0	***	4	✓	✓	-	✓	-
High step-up Y-Source	(LIU et al., 2018a)	PSN	1, 2, 1, 0	***	4	-	✓	-	✓	-
Smooth DC link Y-source	(NIKBAHAR; MONFARED, 2022)	ASN	0, 1, 2, 1	***	4	-	✓	-	✓	✓
LCD snubber	(FOROUZESH et al., 2018)	PSN	1, 1, 2, 0	*	2	✓	✓	✓	✓	✓

Note: L,C,D,T: Inductor, capacitor, diode, transistor; Tp: topology; PSN: Passive snubber; ASN: Active snubber; R: Regenerative; CG: Common ground; G: Generic solution; CIC: Continuous input current; ZMC: Zero magnetizing current

It can be seen in Table 3.6 that all solutions allow common ground between input source and load and continuous input current, which are beneficial characteristics for power converters used in PV inverters. However, the solutions based on topology modification (JI et al., 2017)-(LIU et al., 2019) demand additional elements with ratings similar to the impedance network itself, which adds additional operational stages, cost, and volume. In this way, more complex analytical analysis is required to obtain dynamic models or component design expressions, for example. Furthermore, these kinds of solutions are not generic, i.e., do not apply to any type of impedance-source network and do not always allow zero-magnetizing current at the coupled inductors or they can regenerate the leakage inductance energy. Surely, those types of solutions offer specific advantages, such as higher voltages gain, but they do not offer solutions to the DC link overvoltage issues in existing topologies, which do not help to continue the improvement and research with current topologies, particularly to deploy such converters in industry applications.

The second type of solution is based on active snubbers (NIKBAHAR; MONFARED, 2022), in which a transistor is used together with energy storage devices and diodes to clamp the DC link overvoltage. This type of solution requires additional design complexity since additional gate drive circuits and higher-rating components are required to implement it. Furthermore, one of the main advantages of the impedance-source networks remains on the single-stage power conversion characteristics, which adds a great level of flexibility to these types of converters. But adding an active snubber resembles the simple solution of joining a DC-DC impedance-source converter with an inverter since the output capacitor of a DC-DC converter naturally acts as a voltage-damping device. Hence, in practice, one has a double-stage power conversion, with the typical disadvantages of such structures, such as higher complexity and cost, and lower reliability. Additionally, not necessarily this type of solution is expandable to other MCIS inverters

Lastly the passive snubber solutions (LIU et al., 2018b)-(FOROUZESH et al., 2018) relies on the use of a mix combination of energy storage devices (inductors and capacitors) and diodes to clamp the DC link voltage. The solutions presented in (LIU et al., 2018b), (LIU et al., 2018a), (LIU; SHI; WANG, 2019) require the utilization of additional high-rating components, including a bulky L_o inductance, which may increase the converter volume and cost. Yet, the strategy proposed by (FOROUZESH et al., 2018) presents interesting characteristics, such as a) Low rating components; b) With an adequate design, it does not modify the converter operational stages ('plug-and-play' type-solution); c) Does not require topology modification; d) It is a generic solution, that can be applied in any type of MCIS or any other impedance network. Moreover, the LCD snubber has regenerative capability and it can be used with converters that allow common ground, continuous input current, and zero-magnetizing current - which is the case of the QSY inverter. Unfortunately, the LCD snubber has a challenging design procedure (NIKBAHAR; MONFARED, 2022) and the paper that originates such structure (FOROUZESH et al., 2018) does not present a concise and clear methodology to design such snubber.

Presently, the author is actively studying and proposing analytical and interactive design methodologies for LCD design, since a clear methodology is not present in the literature, as mentioned earlier. A complete description of these solutions will not be given here since the scope of this work is to show the feasibility of the QSY PV multifunctional inverter. Nonetheless, in appendix B it can be seen in Figure B the flowchart of one of the proposed design algorithms by the author, which shows an optimization-oriented design methodology to obtain an LCD snubber taking into account different design criteria, considering current and voltage stress and final snubber weight, volume and cost. In Figure 3.5 it can be seen the obtained waveforms at $V_{DC\,link}$ before and after the insertion of the LCD snubber. It is clear that the peak voltage was damped from 900 V to a value lower than 600 V, which shows that the LCD design methodology was effective.

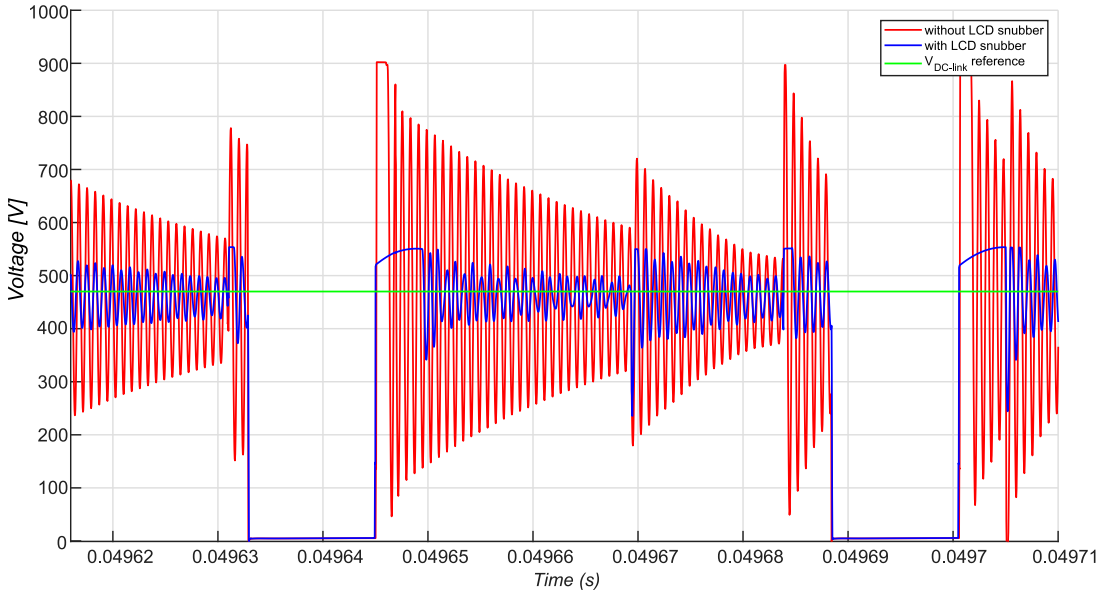


Figure 3.5 – $V_{DC\,link}$ waveform comparison with and without the LCD snubber.

3.5 Summary

In this chapter the QSY network design methodology was presented. Based on the QSY inverter operation, the main design equations were defined, including critical electrical quantities values considering the intended application, defined in Chapter 2. Furthermore, to allow the operation of the inverter considering practical issues, caused mainly by stray inductances, the design of RC and LCD snubber was discussed. With the QSY network parameters defined, the control design of DC link voltage, inverter current, and MPPT closed-loop systems are discussed in the next chapters.

4 DC link voltage control

There are two control variables in the impedance source inverters, namely the shoot-through duty cycle D_{st}, which can be used to regulate $V_{DC\,link}$, and the linear modulation index M, which controls the synthesized inverter AC current. Moreover, the control of these variables can be done independently or not, but satisfactory results are obtained only with the independent schemes (SIWAKOTI et al., 2014d), since a strict regulation of $V_{DC\,link}$ is essential to allow proper energy transfer from DC to AC stages. Hence, this section is concerned to establish a control methodology for the regulation of $V_{DC\,link}$, independently from the inverter AC side current control.

Among the different strategies to regulate $V_{DC\,link}$, the indirect approach proposed by (DING et al., 2007) is used, due to its easiness of implementation and satisfactory results. In this strategy, $V_{DC\,link}$ is indirectly controlled by measuring V_{C1}. Figure 4.1 shows the $V_{DC\,link}$ control strategy used in this work. It is worth mentioning that the MPPT control strategy is performed at the AC side control loop, with the DC side control loop being only responsible for $V_{DC\,link}$ regulation. In the next sections, the control goals and specifications for $V_{DC\,link}$ control are specified.

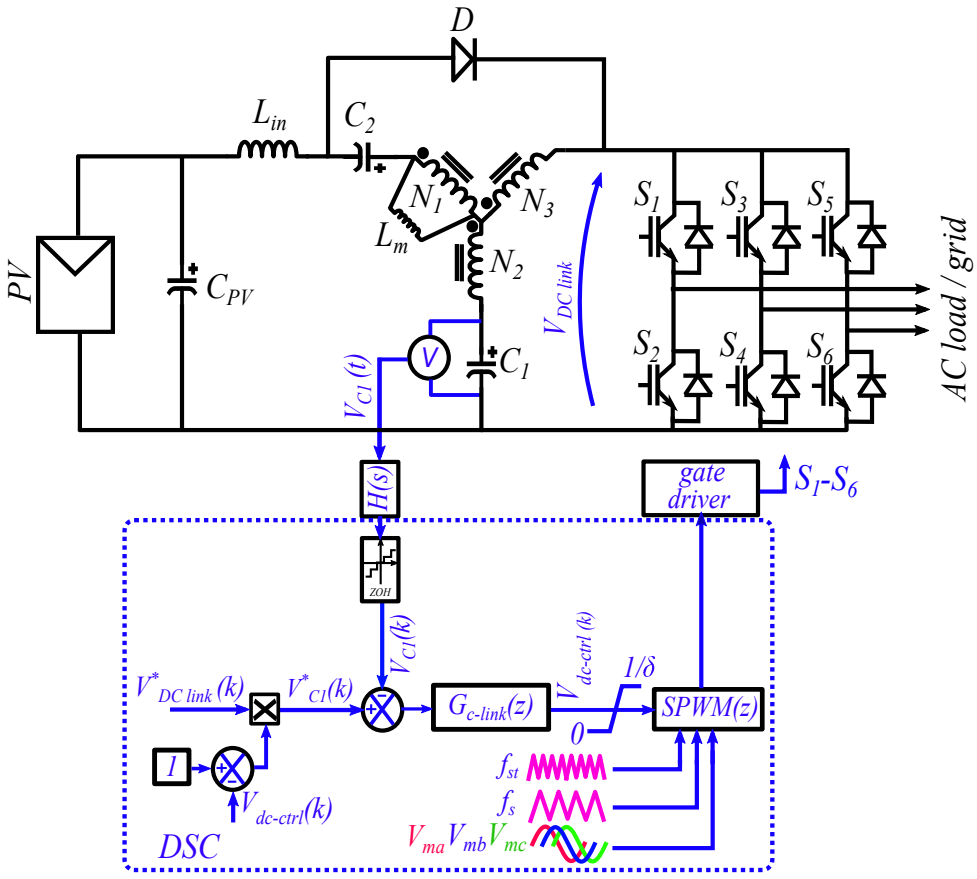


Figure 4.1 – Adopted DC link voltage regulation control system.

4.1 Closed-loop block diagram

Figure 4.2 shows the closed-loop block diagram of the DC link voltage regulation system, where: a) $G_{c-link}(z)$ is the digital controller; b) $SPWM(z)$ is the modified sinusoidal pulse width modulator (PWM); c) $G\frac{V_{C1}}{D_{st}}(s)$ is the V_{C1} to D_{st} transfer function; d) $H(s)$ is the feedback loop dynamics; e) ADC represents the analog to digital conversion dynamics and f) external disturbances are modeled as $\tilde{v}_{in}$ and $\tilde{i}_o$, which represents the input voltage and output current disturbances. In this case, the input voltage disturbance represents the intermittent nature of PV power generation or load variation over time. The $V_{C1}(t)$ voltage is measured by a voltage sensor and signal conditioning board, which are modeled as $H(s)$.

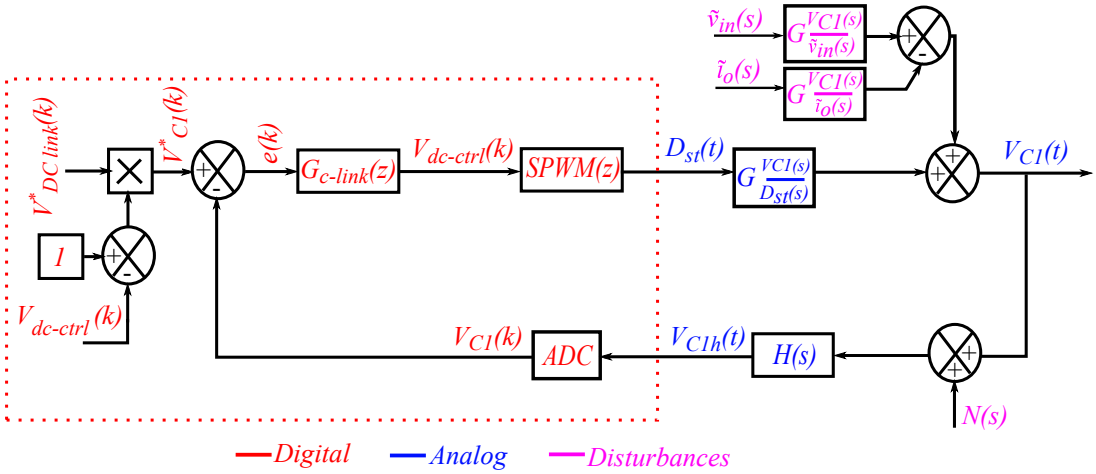


Figure 4.2 – DC link voltage regulation control block diagram.

Additionally, unwanted sensing disturbances may occur, and these are modeled as $N(s)$. The output measured voltage $V_{C1h}(t)$ is then digitalized by ADC, now being a digital value $V_{C1}(k)$. The read voltage is compared with the voltage reference $V^*_{C1}(k)$. Recalling the expressions shown in Table 3.2, $V^*_{DC\,link} = \frac{V^*_{C1}}{D'_{st}}$, hence knowing $V^*_{DC\,link}$, $V^*_{C1}(k)$ is estimated. The difference between $V^*_{C1}(k)$ and $V_{C1}(k)$ values, defined by e_k, is used by the voltage controller $G_{c-link}(z)$ to generate a control signal $V_{dc-ctrl}(k)$, which is used with the modified sinusoidal PWM driver $SPWM(z)$. The $SPWM(z)$ will control the inverter switches with a shoot-through duty-cycle D_{st}, according to $V_{dc-ctrl}(k)$. The transfer function $G\frac{V_{C1}}{D_{st}}(s)$ models how V_{C1} varies with D_{st}. Notice that $V_{C1}(t)$ is affected by input and load disturbances, modeled by $G\frac{V_{C1}}{\tilde{v}_{in}}(s)$ and $G\frac{V_{C1}}{\tilde{i}_o}(s)$. It can be seen that since the desired controller is going to be implemented with a digital signal controller (DSC), then the control system has analog and digital control parts. In this sense, the control design strategy will be made on the continuous time frame, representing the digital blocks in z with an equivalent block in s. After evaluating the system in the continuous time domain, the designed controller is discretized using bilinear transformation, to be implemented in the DSC. In the next sections, additional details are given concerning each block shown in Figure 4.2.

4.2 Feedback dynamics - $H(s)$ and ADC

As can be seen in Figure 4.3, the closed-loop control begins with the feedback signal $V_{C1}(t)$, obtained by the signal voltage sensor (LEM-25P) which also galvanic isolates the power and control sides. The output of the voltage sensor attenuates $V_{C1}(t)$ by a factor of K_{sensor}. Then, an operational-amplifier analog circuit is manually configured to regulate its input signal by a factor of K_{gain}, granting that the read signal is within the scale range of DSC analog to digital converter (ADC). To avoid aliasing, a first-order active low-pass filter with a cut-off frequency defined as $\frac{1}{2\pi R_s C_s} \approx \frac{f_s}{4}$ is implemented by allocating C_s=3.3 nF and R_s=10 kΩ. A voltage limiter circuit is used to grant that the maximum and minimum read voltage values are within the ADC tolerance (in this case a minimum of 0 V and a maximum of 3 V). The resulting signal $V_{C1h}(t)$ is sampled by the ADC at f_s, and once inside the DSC environment, it is re-scaled by K_{adc} such that the feedback path has unity gain, that is $K_{sensor}K_{gain}K_{ADC}$=1. Therefore, considering all the previous comments, the feedback path $H_{ADC}(s)$ is defined as (4.1)

$$H_{ADC}(s) = \frac{1}{1 + sR_sC_s} = \frac{1}{1 + 33 \cdot 10^{-6}s} \tag{4.1}$$

4.3 QSY network dynamics $G\frac{V_{C1}}{D_{st}}(s)$

In this work, the "State-Space Averaging" technique (MIDDLEBROOK; CUK, 1976) is used to derive the small-signal model of the QSY converter. The same assumptions adopted in Section 3.1 are used to derive the small-signal model. Moreover, in the following subsections, the state-space model and its validation, through computational simulations, are presented.

The QSY converter operational states can be mathematically represented in state-space format. Applying KVL and KCL to the equivalent circuit of shoot-through state, as depicted in

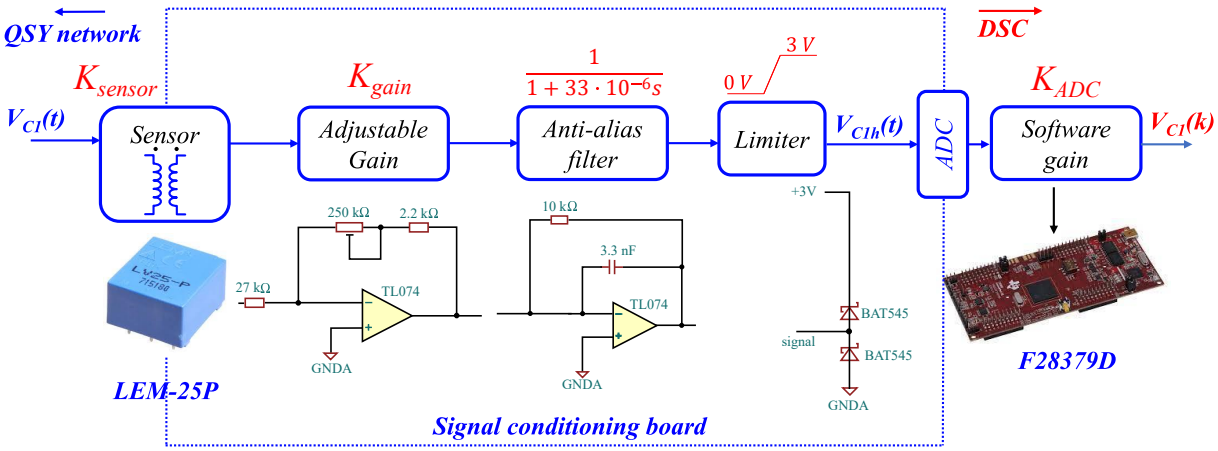


Figure 4.3 – Feedback loop $H(s)$ detailed block diagram.

Figure 1.5a, expressions (4.2)-(4.4) are derived [1].

$$V_{in} - V_{Lin} - V_{rLin} - V_{rC2} - V_{rN1} + V_{C2} - V_{N1}\left(\frac{N_1 + N_2}{N_1}\right) - V_{rC1} - V_{rN2} - V_{C1} = 0 \tag{4.2}$$

$$V_{C1} + V_{rC1} + V_{rN2} + V_{N1}\left(\frac{N_2 - N_3}{N_1}\right) - V_{rS} - V_{rN3} = 0 \tag{4.3}$$

$$I_{Lin} = I_{C1} + I_{N3} = I_{N1} + I_m \tag{4.4}$$

Isolating the state variables derivatives in (4.2)-(4.4), one can obtain (4.5)-(4.10), where $\gamma_1 = \delta\left(r_{N3} + r_S\right)$, $\gamma_2 = -\frac{N_1\left(r_{N3}+r_S\right)}{N_2-N_3}$ and the λ factors present in (4.5)-(4.23) are given in Appendix C.

$$\frac{dI_{Lin}}{dt} = \frac{V_{in}}{L_{in}} + I_{Lin}\lambda_1 + I_m\lambda_2 + V_{C1}\lambda_3 + V_{C2}\lambda_4 \tag{4.5}$$

$$\frac{dI_{load}}{dt} = 0 \tag{4.6}$$

$$\frac{dI_m}{dt} = I_{Lin}\lambda_5 + I_m\lambda_6 + V_{C1}\lambda_7 \tag{4.7}$$

$$\frac{dV_{C1}}{dt} = I_{Lin}\lambda_8 + I_m\lambda_9 \tag{4.8}$$

$$\frac{dV_{C2}}{dt} = I_{Lin}\lambda_{10} \tag{4.9}$$

$$V_{DC\,link} = I_{Lin}\gamma_1 + I_m\gamma_2 \tag{4.10}$$

Similarly, but now considering the active state, it is possible to obtain (4.11)-(4.17) by applying KVL and KCL on the circuit of Figure 1.5b.

$$V_{in} - V_{Lin} - V_{rLin} + V_{C2} + V_{rC2} - V_{N1}\frac{(N_1 + N_2)}{N_1} - V_{rC1} - V_{C1} = 0 \tag{4.11}$$

$$V_{C1} + V_{rC1} + V_{N1}(\frac{N_2 - N_3}{N_1}) - V_{rN3} - V_{R_o} - V_{L_o} = 0 \tag{4.12}$$

$$V_{C2} + V_{rC2} - V_{N1}\frac{N_1 + N_3}{N_1} - V_{rN3} + V_{rD} = 0 \tag{4.13}$$

$$V_{in} - V_{Lin} - V_{rLin} - V_D - V_{R_o} - V_{L_o} = 0 \tag{4.14}$$

$$I_{Lin} = I_D - I_{C2} \tag{4.15}$$

$$I_{C2} = -I_{N1} - I_m = -I_{C1} - I_{N3} \tag{4.16}$$

$$I_{N3} + I_D = I_{load} \tag{4.17}$$

[1] Recall that for a generic quantity x, its root-mean-square (RMS) value is identified as x_{rms}, mean and peak values by $\overline{x}$ and $\hat{x}$, respectively. Moreover, bold variables indicate matrices or vectors (for example, $\mathbf{x}$). Finally, if not otherwise indicated, x refers only to the instantaneous variable value $x(t)$. To keep the notation concise, (t) is omitted in this case.

Isolating the state variables derivatives in (4.11)-(4.17), one can obtain (4.18)-(4.23), where γ_3=$\frac{(r_D\,\delta+r_{N1}+r_{C2})}{\delta'^2}+r_{N2}+\left(\frac{\delta}{\delta'}\right)^2 r_{N3}+r_{C1}$, γ_4=$\frac{-(r_D+r_{N1}+r_{C2})}{\delta'^2}-r_{N2}+\left(\frac{\delta}{\delta'}\right)^2 r_{N3}-r_{C1}$, γ_5=$\frac{N_1(r_D+r_{N1}+r_{C2})}{\delta'(N_1+N_3)}-\frac{N_1\,(N_1+N_2)}{(N_1+N_3)^2}\,r_{N3}$ and γ_6=$-\frac{1}{\delta'}$.

$$\frac{dI_{Lin}}{dt}=\frac{V_{in}}{L_{in}}+I_{Lin}\lambda_{11}+I_{load}\lambda_{12}+I_m\lambda_{13}+V_{C1}\lambda_{14}+V_{C2}\lambda_{15} \tag{4.18}$$

$$\frac{dI_{load}}{dt}=I_{Lin}\lambda_{16}+I_{load}\lambda_{17}+I_m\lambda_{18}+V_{C1}\lambda_{19}+V_{C2}\lambda_{20} \tag{4.19}$$

$$\frac{dI_m}{dt}=I_{Lin}\lambda_{21}+I_{load}\lambda_{22}+I_m\lambda_{23}+V_{C2}\lambda_{24} \tag{4.20}$$

$$\frac{dV_{C1}}{dt}=I_{Lin}\lambda_{25}+I_{load}\lambda_{26} \tag{4.21}$$

$$\frac{dV_{C2}}{dt}=I_{Lin}\lambda_{27}+I_{load}\lambda_{28}+I_m\lambda_{29} \tag{4.22}$$

$$V_{DC\,link}=V_{C1}+I_{Lin}\gamma_3+I_{load}\gamma_4+I_m\gamma_5+V_{C2}\gamma_6 \tag{4.23}$$

Therefore, managing the state variables definitions for active and shoot-through states, given by (4.5)-(4.23), in the matrix format, as indicated by (4.24)-(4.25), where n=1 refers to shoot-through and n=2 to the active state, one can obtain the matrices $\boldsymbol{A_{1-2}}$ and $\boldsymbol{C_{1-2}}$ given by (4.26)-(4.28). Additionally, $\boldsymbol{E_1}$=$\boldsymbol{E_2}$=0 and $\boldsymbol{B_1}$=$\boldsymbol{B_2}$=$\begin{bmatrix}\frac{1}{L_{in}} & 0 & 0 & 0 & 0\end{bmatrix}^T$.

$$\frac{d\boldsymbol{x(t)}}{dt}=\boldsymbol{A_n x(t)}+\boldsymbol{B_n}u(t) \tag{4.24}$$

$$y(t)=\boldsymbol{C_n x(t)}+\boldsymbol{E_n}u(t) \tag{4.25}$$

$$\boldsymbol{A_1}=\begin{bmatrix}\lambda_1 & 0 & \lambda_2 & \lambda_3 & \lambda_4\\ 0 & 0 & 0 & 0 & 0\\ \lambda_5 & 0 & \lambda_6 & \lambda_7 & 0\\ \lambda_8 & 0 & \lambda_9 & 0 & 0\\ \lambda_{10} & 0 & 0 & 0 & 0\end{bmatrix};\ \boldsymbol{A_2}=\begin{bmatrix}\lambda_{11} & \lambda_{12} & \lambda_{13} & \lambda_{14} & \lambda_{15}\\ \lambda_{16} & \lambda_{17} & \lambda_{18} & \lambda_{19} & \lambda_{20}\\ \lambda_{21} & \lambda_{22} & \lambda_{23} & 0 & \lambda_{24}\\ \lambda_{25} & \lambda_{26} & 0 & 0 & 0\\ \lambda_{27} & \lambda_{28} & \lambda_{29} & 0 & 0\end{bmatrix} \tag{4.26}$$

$$\boldsymbol{C_1}=\begin{bmatrix}\gamma_1 & 0 & \gamma_2 & 0 & 0\end{bmatrix} \tag{4.27}$$

$$\boldsymbol{C_2}=\begin{bmatrix}\gamma_3 & \gamma_4 & \gamma_5 & 1 & \gamma_6\end{bmatrix} \tag{4.28}$$

Yet, the state matrices are described by the vector $\boldsymbol{x}=[I_{Lin},I_{load},I_m,V_{C1},V_{C2}]^T$, the input and output variables by $U=V_{in}$ and $y=V_{DC\,link}$, respectively. Through the definitions of matrices $\boldsymbol{A_n}$, $\boldsymbol{B_n}$, $\boldsymbol{C_n}$ and $\boldsymbol{E_n}$ for n=1 and n=2, it is possible to define the average matrices $\boldsymbol{A_{avg}}$, $\boldsymbol{B_{avg}}$, $\boldsymbol{C_{avg}}$, $\boldsymbol{E_{avg}}$, given by (4.29)-(4.32), respectively. Moreover, $\boldsymbol{B_d}$ and $\boldsymbol{E_d}$ matrices are defined by (4.33)-(4.34), where $\boldsymbol{X}$ is the DC terms matrix of state variables, given by (4.35). Finally, the output average value $\boldsymbol{Y}$ is given by (4.36).

$$\boldsymbol{A_{avg}} = \boldsymbol{A_1} D_{st} + \boldsymbol{A_2} D'_{st} \tag{4.29}$$

$$\boldsymbol{B_{avg}} = \boldsymbol{B_1} D_{st} + \boldsymbol{B_2} D'_{st} \tag{4.30}$$

$$\boldsymbol{C_{avg}} = \boldsymbol{C_1} D_{st} + \boldsymbol{C_2} D'_{st} \tag{4.31}$$

$$\boldsymbol{E_{avg}} = \boldsymbol{E_1} D_{st} + \boldsymbol{E_2} D'_{st} \tag{4.32}$$

$$\boldsymbol{B_d} = (\boldsymbol{A_1} - \boldsymbol{A_2})\boldsymbol{X} + (\boldsymbol{B_1} - \boldsymbol{B_2})U \tag{4.33}$$

$$\boldsymbol{E_d} = (\boldsymbol{C_1} - \boldsymbol{C_2})\boldsymbol{X} + (\boldsymbol{E_1} - \boldsymbol{E_2})U \tag{4.34}$$

$$\boldsymbol{X} = -\boldsymbol{A_{avg}^{-1}} \boldsymbol{B_{avg}} U \tag{4.35}$$

$$\boldsymbol{Y} = (-\boldsymbol{C_{avg}} \boldsymbol{A_{avg}^{-1}} \boldsymbol{B_{avg}} + \boldsymbol{E_{avg}})U \tag{4.36}$$

The transfer functions considering the state variables in relation to the control and the input are given by (4.37) and (4.38), respectively, and output variable to input and control, by (4.39) and (4.40), respectively.

$$\frac{\hat{\boldsymbol{x}}(\boldsymbol{s})}{\hat{d}(s)} = (s\boldsymbol{I} - \boldsymbol{A_{avg}})^{-1} \boldsymbol{B_d} \tag{4.37}$$

$$\frac{\hat{\boldsymbol{x}}(\boldsymbol{s})}{\hat{u}(s)} = (s\boldsymbol{I} - \boldsymbol{A_{avg}})^{-1} \boldsymbol{B_{avg}} \tag{4.38}$$

$$\frac{\hat{\boldsymbol{y}}(\boldsymbol{s})}{\hat{d}(s)} = \boldsymbol{C_{avg}}(s\boldsymbol{I} - \boldsymbol{A_{avg}})^{-1} \boldsymbol{B_d} + \boldsymbol{E_d} \tag{4.39}$$

$$\frac{\hat{\boldsymbol{y}}(\boldsymbol{s})}{\hat{u}(s)} = \boldsymbol{C_{avg}}(s\boldsymbol{I} - \boldsymbol{A_{avg}})^{-1} \boldsymbol{B_{avg}} + \boldsymbol{E_{avg}} \tag{4.40}$$

To evaluate the usefulness of the transfer functions obtained from the small-signal model, the QSY inverter equivalent circuit, depicted in Figure 1.5 was simulated using a switched circuit and the transfer functions, using PSIM and considering the parameters given in Table 3.4, with L_o defined as 5.56 mH. The implemented circuit model on PSIM can be seen in Figure 4.4. The transient behaviors of the state space variables due to a step of 3% in D_{st} are shown in Figure 4.5, considering results from the transfer functions $\frac{I_{Lin}(s)}{\hat{d}_{st}(s)}$, $\frac{I_{load}(s)}{\hat{d}_{st}(s)}$, $\frac{I_m(s)}{\hat{d}_{st}(s)}$, $\frac{V_{C1}(s)}{\hat{d}_{st}(s)}$, $\frac{V_{C2}(s)}{\hat{d}_{st}(s)}$ and the respective switched circuit waveform. It should be clarified that the insertion of s_{aux} free-wheel switch is needed to turn the circuit behavior at PSIM similar to what is considered during the small-signal model derivation. The reason for this is that the current through I_{Lo} cannot be interrupted abruptly during the transition from active to shoot-through state - as it is the case in the mathematical model. Moreover, the insertion of s_{aux} do not modify the converter dynamics and the modeling procedure carried out in this chapter. As can be seen, the obtained results show that there is a satisfactory match between the theoretical prediction provided by the dynamic model and the switched converter operation.

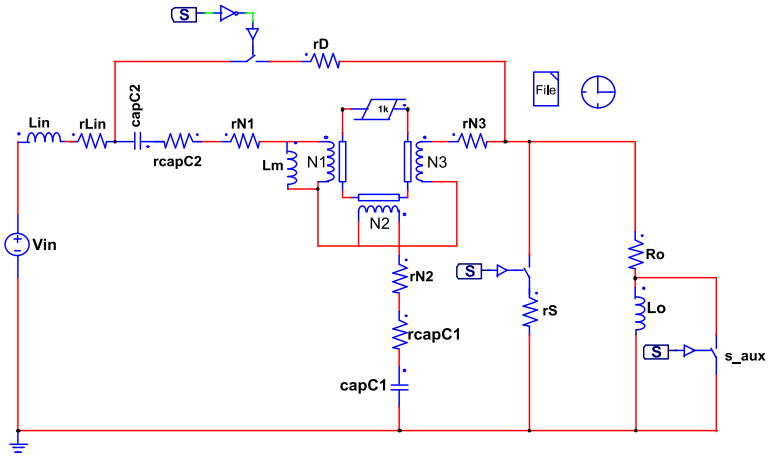


Figure 4.4 – Equivalent QSY converter circuit built on PSIM.

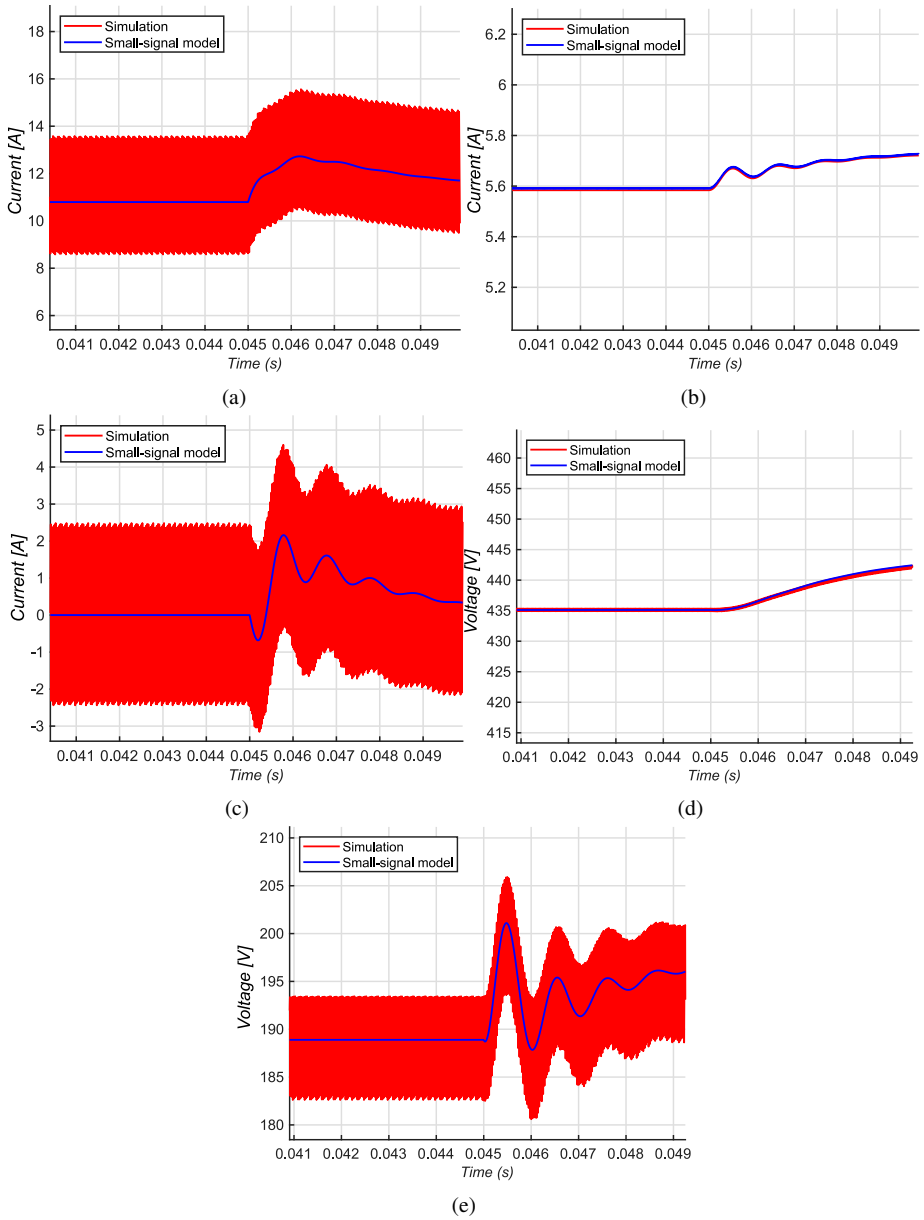


Figure 4.5 – State-Space variables for the switched circuit and dynamic model transfer functions - waveforms comparison: a) $I_{Lin}(t)$; b)$I_{load}(t)$; c) $I_m(t)$; d) $V_{C1}(t)$; e) $V_{C2}(t)$.

4.4 Modified Sinusoidal PWM - SPWM(s)

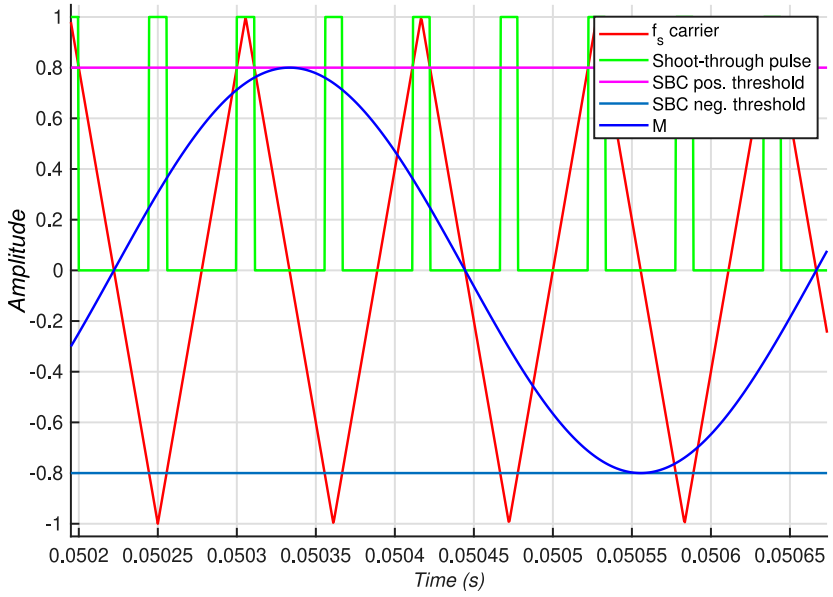
In conventional inverters, as shown in Figure 1.2a, sinusoidal PWM or space vector techniques comprise the main strategies for the control of inverter transistors, such that AC voltages or currents are obtained at the inverter output. However, with impedance-source-based inverters, this control technique must be modified to include the control information that is necessary to establish the shoot-through conduction. There are several ways to achieve this goal using different control schemes, such as Simple Boost (SBC), Maximum Constant Boost (MCBC), and Maximum Boost (MBC) controls. A comprehensive comparison among these techniques applied to the QSY inverter was done by the author in (SANTOS; GONÇALVES, 2021). Table 4.1 presents the different expressions of D_{st} when different modified SPWM techniques are employed. For all these techniques, the control of AC and DC sides are not independent of each other, that is, M is responsible to define D_{st} (and consequently $V_{DC\,link}$) and also follows the AC control voltage/current reference simultaneously. Since the decoupled control of DC and AC sides is desired, then a different approach is needed.

Table 4.1 – Relationship between D_{st} and M for different modified SPWM techniques.

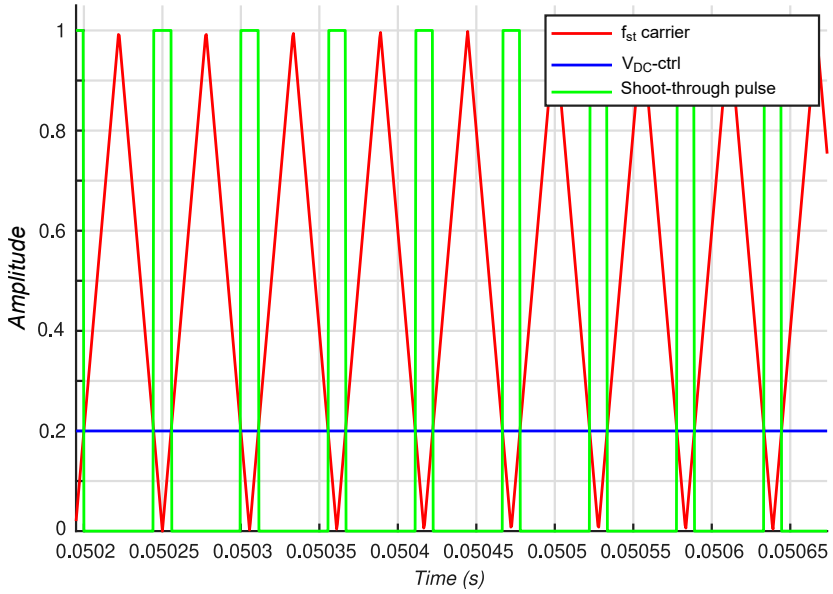
Index	**SBC**	**MBC**	**MCBC**
D_{st}	$1-M$	$\frac{2\pi-3\sqrt{3}M}{2\pi}$	$1-\frac{\sqrt{3}M}{2}$

Figure 4.6 presents the waveforms for the conventional Simple Boost Control (SBC) and modified SBC, proposed by (DING et al., 2007). In the conventional SBC, as shown in Figure 4.6a, one triangular wave carrier with f_s frequency is directly compared with two auxiliary control signals, defined by SBC positive and negative thresholds. Notice that each threshold signal is equal in module to M. When the triangular carrier is greater or lower than the threshold values, a shoot-through pulse with duty-cycle defined as D_{st} is generated. However, the auxiliary signals' positive and negative thresholds change as the AC modulation carrier change, which do not allow decoupled control. The modified SBC strategy shown in Figure 4.6b uses a triangular wave carrier with the frequency defined as twice f_s, that is, the f_{st} frequency. Moreover, the mean value of the new triangular carrier is 0.5, instead of 0, and the maximum and minimum values are defined as 1 and 0, respectively. A single control signal, $V_{dc-ctrl}$ is compared with the triangular carrier to generate the shoot-through pulses with D_{st} duty-cycle, instead of two auxiliary signals, as in conventional SBC.

Yet, the shoot-through pulses do not depend on the AC modulation signal, which is now compared with another triangular carrier with f_s frequency to synthesize the desired inverter AC output voltage/current, allowing decoupled control between inverter AC and DC sides. Analyzing the waveforms shown in Figure 4.6b and considering the inherent delay present in digital PWM with double update mode (BUSO; MATTAVELLI, 2015), one found that the transfer function of D_{st} to $V_{DC-ctrl}$ is given by (4.41). Additionally, as in conventional SBC, the maximum value of



(a)



(b)

Figure 4.6 – Simple Boost Control shoot-through pulses generation schemes: a) Conventional; b) Modified.

M, defined as M_{max}, depends on the maximum value of $V_{dc-ctrl}$, which is theoretically defined as $V_{dc-ctrl-max} = \frac{1}{\delta}$. If M is greater than M_{max}, the inverter AC output will not respond as desired to the control command, and a satisfactory AC reference tracking is not obtained.

$$SPWM(s) = \frac{D_{st}}{V_{dc-ctrl}} = \frac{1 - \frac{s}{4f_{st}}}{1 + \frac{s}{4f_{st}}} \tag{4.41}$$

With all the required transfer functions obtained the discussion can be forwarded to the definition of the control goals and dynamics specifications.

4.5 Control goals and specifications

The first step for the control design of $V_{DC\,link}$ is to define the desired performance requirements that must be met by the closed-loop control system. The following requirements are established:

1. *Requirement 1*: The converter must remain stable in the nominal operation condition, even in the presence of load or input voltage disturbances. Furthermore, the system dynamics should be immune to feedback signal reading noise or another external control disturbances.

2. *Requirement 2*: The dynamic response of $V_{DC\,link}$ should not have excessive overshoot. The desired dynamic should be damped and smooth, with an overdamped characteristic. In this sense, the adopted phase margin is defined at PM=70 °. Considering that the regulation of $V_{DC\,link}$ employs a control bandwidth up to 10 Hz with a phase margin of 70° (MARAFAO, 2004) the adopted cut-off frequency for the closed-loop control system is f_{bw}=5 Hz.

3. *Requirement 3*: The steady-state error (e_{ss}) must be negligible for step control reference input.

With the control requirements defined for the QSY inverter DC link voltage regulation, the design methodology of G_{clink} is given in the next section.

4.6 DC link voltage controller design

In this section, the control design methodology of G_{clink} is performed at the frequency domain, and therefore it will be indicated in the following paragraphs as $G_{clink}(s)$. The design methodology and the assumptions made are listed below:

- *Step 1: Gathering of all the necessary transfer functions*: Table 4.2 summarizes the necessary transfer functions that are necessary to design $G_{c-link}(s)$, and were explained in the previous sections. It should be noted that $G\frac{V_{C1}(s)}{D_{st}(s)}$ is herein numerically presented using the parameters presented in Tables 2.2 and 3.3.

- *Step 2: Open loop gain $T_{DC}(s)$ analysis*: The control loop design is made, analyzing the open-loop gain transfer-function $T_{DC}(s)$, defined by (4.42). It can be noticed from Table 4.2 and (4.42), that $T_{DC}(s)$ is a high-order system, that is, the magnitude of the transfer-function denominator polynomial is greater than 2. To successfully apply the classical linear frequency response control design strategies, it is desirable that an equivalent system with an order equal to 1 or 2 should be obtained (BISHOP, 2011). Table 4.3 shows the

Table 4.2 – Variables required for the controller design.

Variable	**value**
$G\frac{V_{C1}(s)}{D_{st}(s)}$	$\frac{-1\cdot10^5 s^4-3.818\cdot10^8 s^3+9.699\cdot10^{12}s^2-1.98\cdot10^{16}s+6.981\cdot10^{20}}{s^5+1.764\cdot10^4 s^4+9.311\cdot10^7 s^3+6.559\cdot10^{11}s^2+1.086\cdot10^{15}s+3.94\cdot10^{17}}$
$SPWM(s)$	$\frac{1-\frac{s}{144\cdot10^3}}{1+\frac{s}{144\cdot10^3}}$
$H_{ADC}(s)$	$\frac{1}{1+33\cdot10^{-6}s}$
f_{st}, f_{bw}, PM	36 kHz, 5 Hz, 70 °

poles of the uncompensated open-loop gain $T_{uDC}(s)$, in which is possible to observe that the dominant real pole is given by -508.8043. Thus a first-order approximated system $T_{uDCa}(s)$ is defined as 4.43, with a gain adjustment such that the steady-state step response of the approximate system matches $T_{uDC}(s)$. Figure 4.7 shows the frequency response of $T_{uDC}(s)$ and $T_{uDCa}(s)$. It can be seen that there is a good match between $T_{uDC}(s)$ and $T_{uDCa}(s)$ for frequencies below 10 Hz, which is where f_{bw} is located. Hence the controller design will be made considering $T_{uDCa}(s)$.

$$T_{DC}(s) = G_{c-link}(s)\cdot SPWM(s)\cdot G\frac{V_{C1}(s)}{D_{st}(s)}\cdot H_{ADC}(s) \tag{4.42}$$

$$T_{uDCa}(s) = \frac{9\cdot10^5}{s+508.8043} \tag{4.43}$$

Table 4.3 – Poles of $T_{uDC}(s)$.

Poles of $T_{uDC}(s)$
-508.8043
$-851.0862 \pm j6.0589\cdot10^3$
-1482.7
-13950.9
-30303
-144000

- *Step 3: Controller definition and design*: Evaluating the poles of $T_{uDCa}(s)$ is possible to notice that the uncompensated system does not have a pole at the origin, which means that the system is type 0, with non-zero steady-state error for a step input. Hence, to increase the system to type 1 and comply with control requirement 3, an integrator must be added to T_{uDCa} at the controller term, to achieve zero steady-state error for step reference input. Moreover, to add the desired dynamics (f_{bw}=5Hz and PM=70 °) a zero must be added to modify $T_{DC}(s)$ phase margin at f_{bw}. In Figure 4.7 it is possible to observe that the phase

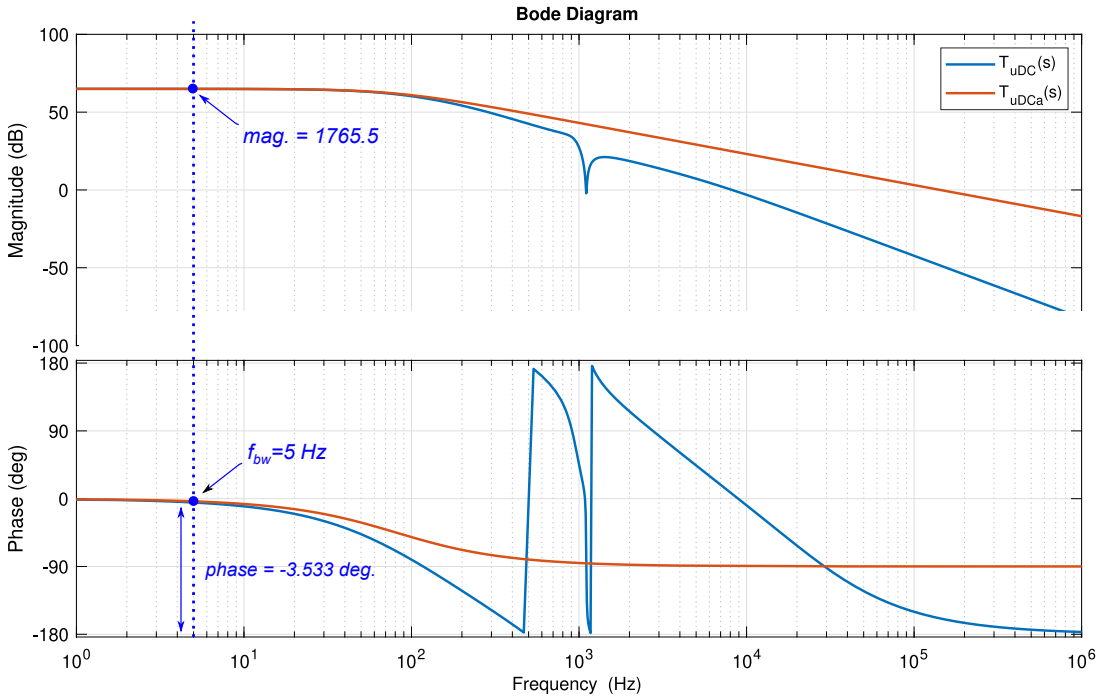


Figure 4.7 – Uncompensated open-loop gain $T_{uDC}(s)$ and approximate transfer function $T_{uDCa}(s)$ comparison.

of T_{uDCa} at 5 Hz is -3.533 ° with a magnitude of G_{udc}=1765.5. To obtain PM=70 ° a phase addition of -106.467 ° is necessary. Nonetheless, the integrator term alone adds -90 °. Hence, a phase-lag compensator is designed to add the remaining Φ_m=-16.467 ° phase at f_{bw}=5 Hz. However, considering the phase error between $T_{uDC}(s)$ and $T_{uDCa}(s)$ at 5 Hz, the phase-lag should add Φ_m=-14.867 ° . The final controller formulation is given by (4.48), and z_{dc}, p_{dc} and K_{gdc} are calculated by (4.45)-(4.47), where α_{dc} is defined by (4.44) and is calculated in terms of Φ_m.

$$\alpha_{dc} = \frac{\sin\Phi_m + 1}{1 - \sin\Phi_m} = \frac{\sin(-14.867°) + 1}{1 - \sin(-14.867°)} = 0.592 \tag{4.44}$$

$$p_{dc} = 2\pi f_{bw}\sqrt{\alpha_{dc}} = 31.416\sqrt{0.592} = 24.172 \tag{4.45}$$

$$z_{dc} = \frac{p_{dc}}{\alpha_{dc}} = \frac{24.172}{0.592} = 40.831 \tag{4.46}$$

$$K_{gdc} = \sqrt{\frac{(2\pi f_{bw})^2 + p_{dc}^2}{(2\pi f_{bw})^2 + z_{dc}^2}}\frac{2\pi f_{bw}}{G_{udc}} = \sqrt{\frac{31.416^2 + 24.172^2}{31.416^2 + 40.831^2}}\frac{31.416}{1765.5} = 13.69 \cdot 10^{-3} \tag{4.47}$$

$$G_{c-link}(s) = \frac{K_{gdc}}{s}\left(\frac{s + z_{dc}}{s + p_{dc}}\right) = \frac{13.69 \cdot 10^{-3}}{s}\left(\frac{s + 40.831}{s + 24.172}\right) \tag{4.48}$$

- *Step 4: Evaluation of controller performance*: With the controller designed it is necessary to evaluate the closed-loop control system performance, particularly if the control requirements are met. Figure 4.8a shows the compensated open-loop gain $T_{DC}(s)$. It is possible to see that the project requirements f_{bw} and PM are satisfied, with minimum

deviation from the design objective. Now, regarding the dynamic response, a simulation at PSIM is performed considering the designed controller, in the following scenarios: a) Input voltage variation; b) Load variation; c) Feedback noise at readings of $V_{C1}(t)$. The obtained results are shown in Figure 4.8b. It can be clearly seen that the closed-loop control system is robust against input, load, and $V_{C1}(t)$ feedback measurement noise disturbances, which means that the controller maintains $V_{DC\,link}$ at the desired control reference even when in the presence of external disturbances, which satisfies all the control objectives. Moreover, an overshoot of 8% was measured when an input voltage disturbance of +10% occurred, and an undershoot of -6% was measured when a load step disturbance of -33% occurred, which is considered to be a smooth variation when compared to the reference value of 600 V. Furthermore, after input voltage and load disturbances, the settling time, considering a 2% criteria (BISHOP, 2011), was measured as 45 ms and 46 ms, respectively, which is the result of the relatively low control bandwidth (10 Hz) and relatively high phase-margin (70 °), but still acceptable. Finally, a negligible steady-state error was measured in steady-state, which attends the control design requirement 3.

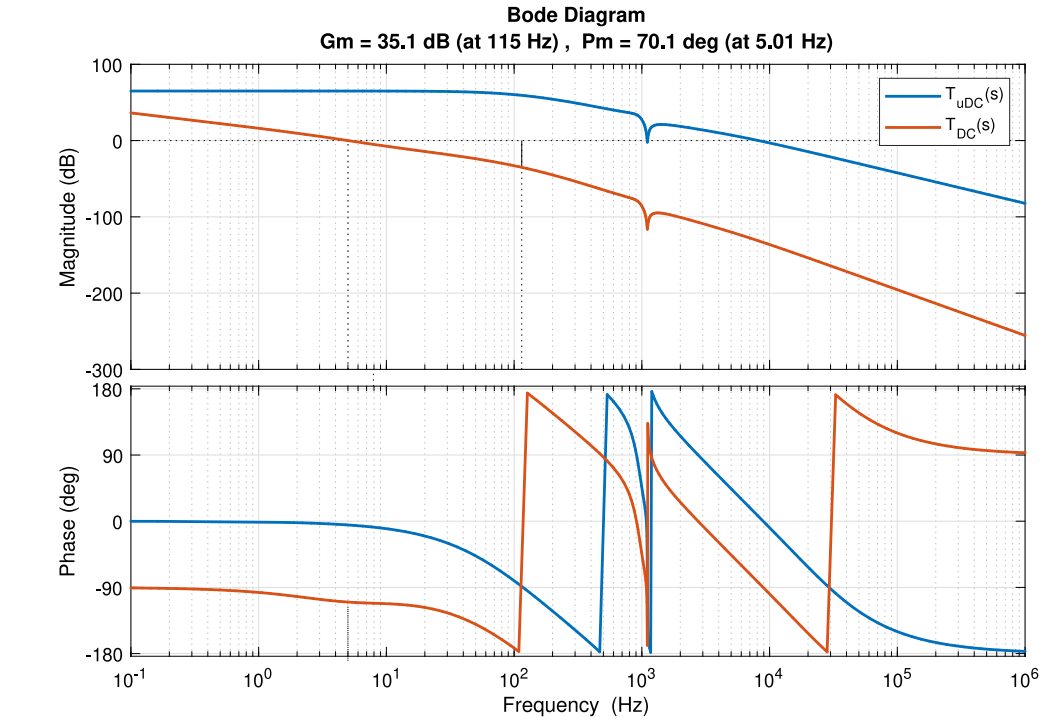
- *Step 5: Controller discretization*: Lastly, to obtain the digital controller formulation, a discretization method should be adopted, in which the s variable in the controller transfer function (4.48) is replaced by one of the possibilities shown in Table 4.4. The selection of one of the different discretization types is conditioned to the insertion of additional dynamic characteristics which may affect the controller performance and must be analyzed prior to being implemented at the DSC. In this case, the Tustin method is selected since it presented the most satisfactory results according to the author experience. Finally, considering the digital implementation it is convenient to represent the controller as a difference equation as can be seen in (4.50), in which the b_z and a_z factors for $G_{c-link}(s)$ are defined in Table 4.5.

Table 4.4 – Discretization methods and alternative ways for s substitution.

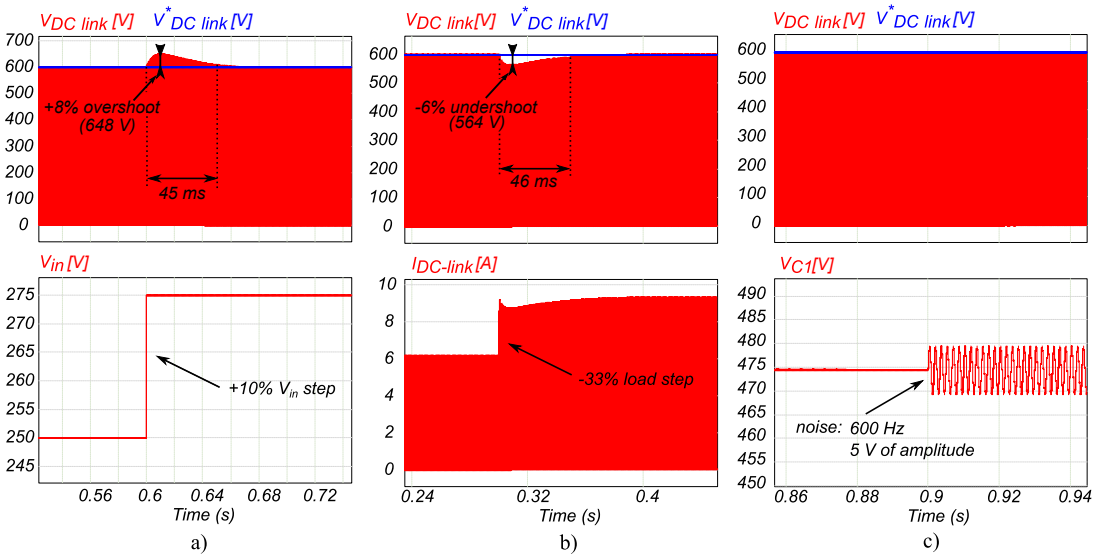
Discretization method	**Substitution for s**
Backward Euler	$s = \dfrac{1 - z^{-1}}{T_s}$
Forward Euler	$s = \dfrac{1 - z^{-1}}{T_s z^{-1}}$
Tustin	$s = \dfrac{2}{T_s}\dfrac{1 - z^{-1}}{1 + z^{-1}}$

$$G(z) = 3.8045 \cdot 10^{-7} \frac{(z+1)(z-0.9977)}{(z-1)(z-0.9987)} \tag{4.49}$$

$$G(z) = \frac{Y(z)}{X(z)} = b_o x(k) + ... + b_n x(k-n) - a_o y(k) - ... - a_n y(k-n) \tag{4.50}$$



(a)



(b)

Figure 4.8 – Controller performance: a) Uncompensated and compensated open-loop gain $T_{DC}(s)$ comparison; b) Simulated dynamic response when with input (a), load(b) and noise at $V_{C1}(t)$ (c) disturbances.

Table 4.5 – Digital controller version of $G_{c-link}(s)$ digital coefficients b_z and a_z.

b_z	a_z
b_0=380.453633264111$\cdot 10^{-9}$	a_0=1
b_1=862.039106763746$\cdot 10^{-12}$	a_1=-1.99865801218138
b_2=-379.591594268369$\cdot 10^{-9}$	a_2=998.658012181376$\cdot 10^{-3}$

4.7 Summary

In this chapter, it was shown how to design the DC link voltage control loop for the QSY inverter. Beginning with the voltage regulation closed-loop control system block diagram, all the transfer functions required to design the controller $G_{c-link}(z)$ were defined. Moreover, the small-signal analysis of the QSY inverter was carried out such that the $G\frac{V_{C1}(s)}{D_{st}(s)}$ transfer function is derived. Finally, the control goals and dynamic specifications were established, and the $G_{c-link}(z)$ controller design was demonstrated through detailed steps.

To validate the obtained controller, several simulations were conducted using PSIM, evaluating the performance of the controller against input voltage and load variations and $V_{C1}(t)$ feedback reading with external disturbances. The obtained simulation results demonstrate the effectiveness of the designed controller to regulate $V_{DC\,link}$. With the DC link controller designed, in the next chapter, the inverter output current controller methodology is presented.

5 Inverter current control

With the DC link controller designed, it is necessary to define the inverter AC current controller. Before the controller definition and design, the inverter topology, low-pass passive filter, and PLL strategy must be selected. All these aspects are covered in this chapter. The three-phase DC-AC converter (inverter) used in this work is shown in Figure 5.1a and is comprised of six IGBTs, with three-legs individually controlled by a sinusoidal carrier-based PWM control with the Simple Boost modification (SBC-SPWM), as described in Section 4.4. The S_1-S_6 terminals represent the gate control terminals of each IGBT. The SBC-SPWM driver block diagram is shown in Figure 5.1b.

It can be seen that the gate signals S_1 and S_2 have an OR logic scheme to integrate the shoot-through pulses s_t. This means that the shoot-through only occurs in the first inverter leg, with the rest operating only with control signals generated by the direct comparison between triangular wave with f_s frequency and M_a, M_b and M_c sinusoidal carriers. The two triangular wave carriers, with frequencies f_s and f_{st}, are shown in Figure 5.1b, such that one is responsible for the shoot-through pulses generation and the other for the inverter AC output current, respectively. Besides the frequencies, both triangular carriers have different phase displacements, such that shoot-through pulses occur only in the null state, as required by the Simple Boost control approach.

To attend to the project inverter's current THD requirement, a proper low-pass passive filter should be used. Among the possible solutions, the L, LC, and LCL passive filters are the most common options found in the literature. In this chapter, the LC filter is selected, since it presents an interesting compromise between high-frequency current components damping and design complexity.

5.1 LC filter design

At the inverter output there is a passive low-pass filter comprised of an LC arrangement. The design of the LC filter adopted in this work is based on the methodology developed by (SILVA; POMÍLIO; VENDRUSCULO, 2010). The parameters listed in Table 5.1 present a summary of the main requirements for the LC filter design. Since the processed power is 3 kVA, adopting a safety factor value of 25%, it is possible to consider an effective power design parameter of 3.75 kVA. To minimize the presence of harmonic components in the phase current, and at the same time avoid the utilization of bulky inductors, a ripple factor of 5% was adopted. The inductor series resistance is stipulated as 15% the value of the filter inductive reactance at 60 Hz. The resonance frequency of the filter is based on the inverter switching frequency, such that a sufficient bandwidth for the synthetization of harmonic currents is possible. Hence, the

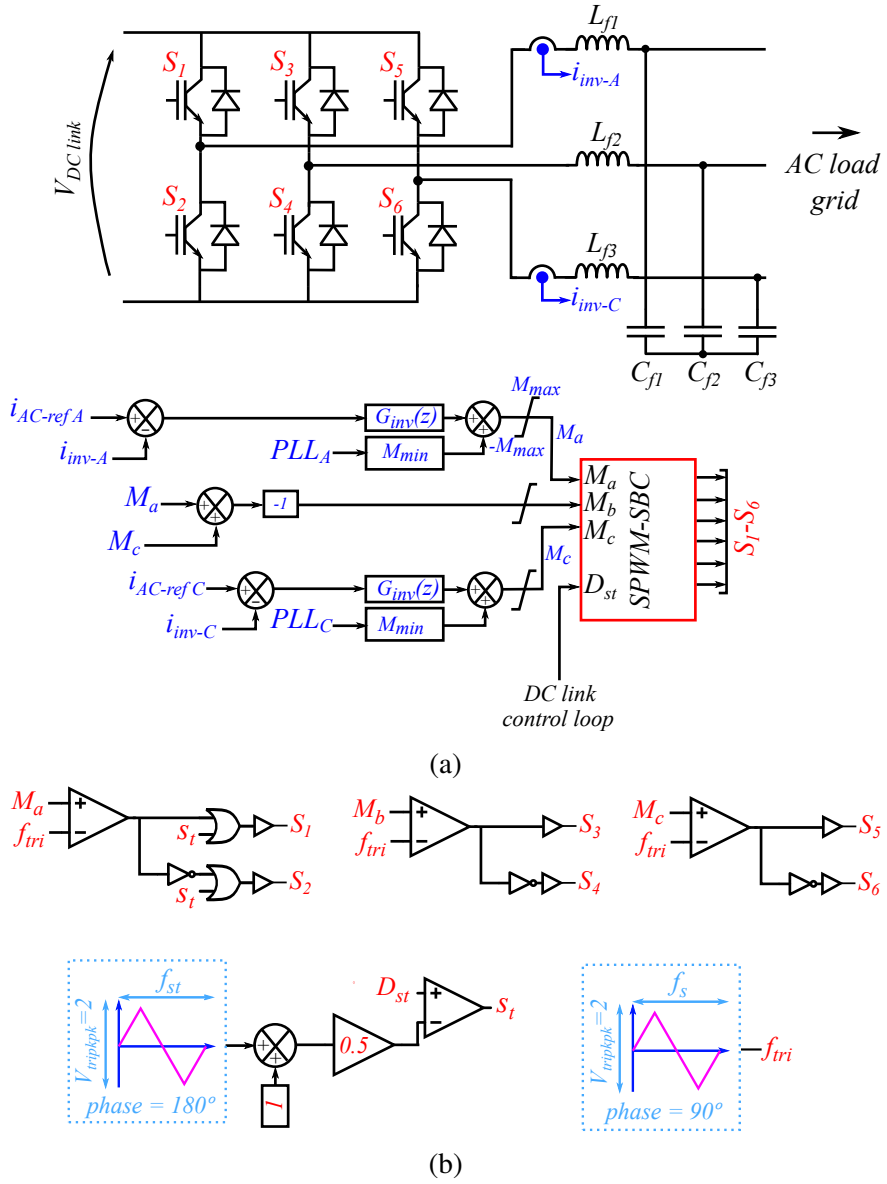


Figure 5.1 – The DC-AC conversion part of the QSY-inverter: a) DC-AC converter configuration for the QSY inverter; b) Block diagram of the SPWM-SBC.

resonance frequency is defined as $\frac{f_s}{10}$=1.8 kHz. With the values listed in Table 5.1, the values of $r_{Lf1,2,3}$, $L_{f1,2,3}$ and $C_{f1,2,3}$ were obtained through the expressions given in Table 5.2. The frequency response of the LC filter is shown in Figure 5.2 [1]. With the inverter passive filter properly designed, is now possible to derive the inverter current to control transfer function $G\frac{\tilde{i}_{Lf}(s)}{M(s)}$, which is used during the current controller design.

5.2 $G\frac{\tilde{i}_{Lf}(s)}{M(s)}$ definition

As the inverter output filter capacitors $C_{f1,2,3}$ behaves as a high impedance path for the current bandwidth synthesized by the inverter (f_{AC} to $\frac{f_s}{10}$) the equivalent inverter model when

[1] Particularly for off-grid applications, the utilization of a damping strategy may be desired to alleviate the high gain at resonance frequency.

Table 5.1 – LC filter design parameters.

Parameter	Value
Total power $A_{inv-max}$	3.75 kVA
Current ripple factor $I_{o-ripple}$	5%
Equivalent series resistance (percentage of reactance at 60 Hz)	15%
Switching frequency	18 kHz
Resonance frequency f_{res}	1.8 kHz
Grid phase rms voltage $V_{grid-rms}$	127 V
Fundamental frequency f_{AC}	60 Hz
DC link value	600 V

Table 5.2 – LC filter design expressions.

Element	Expression	Value
$L_{f1,2,3}$	$\frac{V_{DC\,link}}{8 f_s I_{o-max} I_{o-ripple}}$	6 mH
$C_{f1,2,3}$	$\frac{1}{(2\pi f_{res})^2 L_{f1,2,3}}$	1 μF
$r_{Lf1,2,3}$	$(15\%) 2\pi f_{AC} L_{f1,2,3}$	339 mΩ
I_{o-max}	$2\frac{A_{inv-max}}{3\sqrt{2}V_{grid-rms}}$	13.92 A

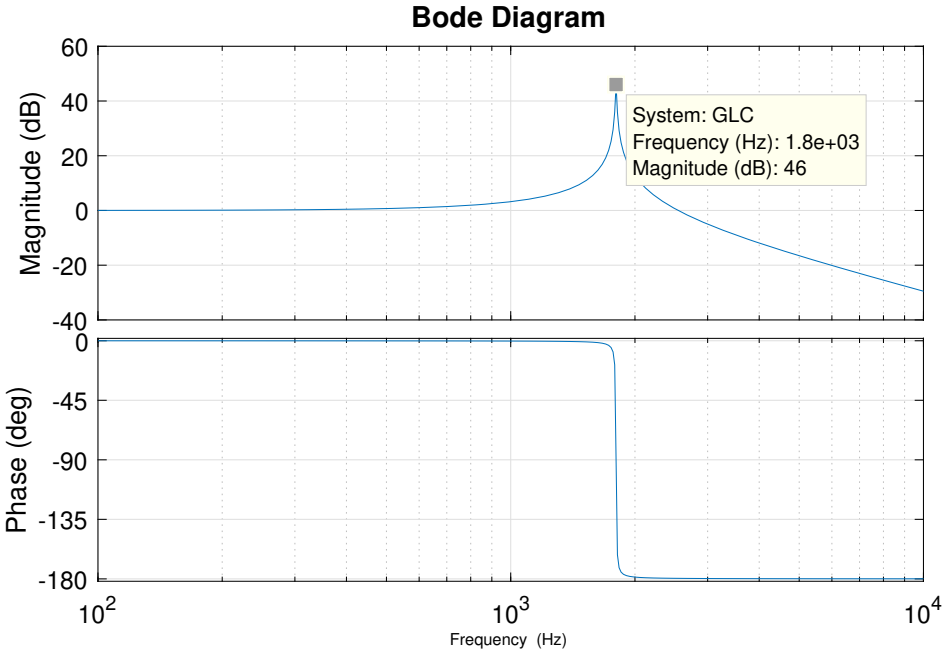
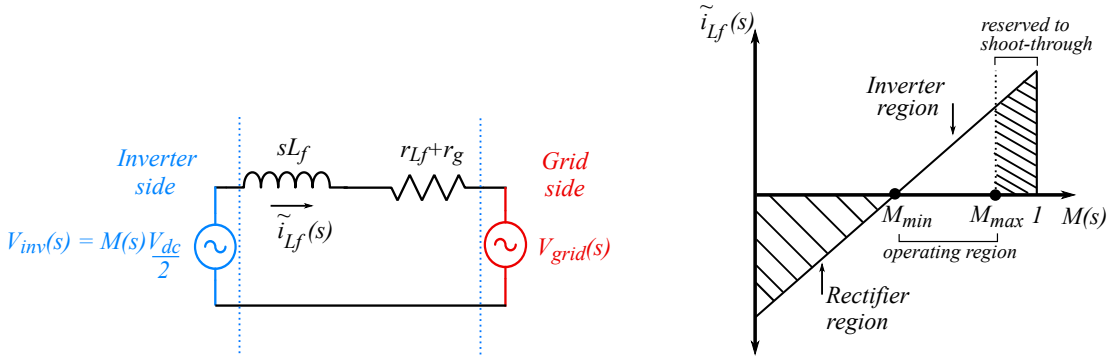


Figure 5.2 – Designed passive low-pass LC filter frequency response.

connected to the grid, is shown in Figure 5.3a. It can be seen that current $\tilde{i}_{Lf}$, which is integrated into the main grid, can be given by the expression (5.1), where r_{Lf} and r_g are the filter inductance ESR and grid resistance, respectively and $M(s)$ is the AC control signal command. Figure 5.3b shows the behavior of $\tilde{i}_{Lf}$ for different values of $M(s)$. For $M(s) < M_{min}$, the energy flux comes from the grid back to the inverter, which means that the converter is operating in the rectifier mode, which is not desired in the proposed application. However, when $M(s) > M_{min}$ the energy flux goes from the inverter to the grid, which is the inverter operating mode required for the QSY converter.

Therefore, keeping the inverter functioning in the linear operating region, the working range of $M(s)$ is defined as $M_{min} < M(s) < M_{max}$, where M_{max} is the maximum allowable M such that no interference with shoot-through conduction arises. The definition of M_{max} is directly related to the amount of D_{st} required to regulate $V_{DC\,link}$, and regarding the project



(a) (b)

Figure 5.3 – QSY inverter operation mode when grid-connected: a) Per-phase equivalent circuit model; b) Operating regions.

parameters shown in Table 3.3, M_{max} is defined as (5.4), where $D_{st-ctrl}$ is the effective D_{st} used to regulate the $V_{DC\,link}$, which may be slightly higher than D_{st}=0.1944 due to converter losses. Hence, a linear relationship between $\tilde{i}_{Lf}$ and $M(s)$ can be derived as (5.2) when this range of $M(s)$ is respected. Furthermore, the value of M_{min} is defined when $\tilde{i}_{Lf}(s)$=0, hence it is described by (5.3), where $V_{pk-grid}$ is the peak value of V_{grid}.

$$\tilde{i}_{Lf}(s) = M(s)\frac{V_{DC\,link}}{2}\frac{1}{r_{Lf}+r_g+sL_f} - \frac{V_{grid}(s)}{r_{Lf}+r_g+sL_f} \tag{5.1}$$

$$G\frac{\tilde{i}_{Lf}(s)}{M(s)} = \frac{V_{DC\,link}}{2}\frac{1}{r_{Lf}+r_g+sL_f} \tag{5.2}$$

$$M_{min} = \frac{2V_{pk-grid}}{V_{DC\,link}} \tag{5.3}$$

$$M_{max} = 1 - D_{st-ctrl} \tag{5.4}$$

It is required that the inverter injected current must be in phase with grid voltages, to allow a unity power factor operation when only active power is delivered to the grid. Furthermore, having a sinusoidal current reference, in phase with grid voltages, with an amplitude given by M_{min}, it is possible to use this signal as a feed-forward control command to minimize the control effort of the inverter currents controllers [2]. To attain these objectives, a PLL controller is needed, which is the next treated topic.

5.3 PLL design

The PLL algorithm is used to generate a sine-wave reference signal that is in phase with the grid voltage. The algorithm used in this work is based on (PÁDUA; DECKMANN; MARAFÃO, 2005) and its block diagram is shown in Figure 5.4. The main idea of this strategy is to synthesize three sinusoidal variables $u_{a\perp}, u_{b\perp}, u_{c\perp}$ which are orthogonal to the measured

[2] It is considered in this case that the phase voltages are symmetrical, equally displaced in 120° from each other.

grid voltage signals v_a, v_b, v_c in steady state. Due to the orthogonality principle, the product of the synthesized variables and the measured voltage signals should be zero in the steady state (that is d_p=0). The instantaneous angular argument θ used to obtain $u_{a\perp}, u_{b\perp}, u_{c\perp}$ is obtained by the integration of the PI regulator, defined by $\Delta\omega$, added to the nominal grid angular frequency ω_n. The $\Delta\omega$ variable is obtained by the PI regulator control action, which tends to converge the mean cross product $\overline{d_p}$, present at the output of the mean average filter $\sum_0^T \frac{1}{T}$ to zero, which results in the correct determination of angular frequency ω. Lastly, this algorithm also presents satisfactory results for sinusoidal signals with harmonic content, and if an adaptative mean average filter is implemented, the presented scheme can be used for variable frequency signals. In this work, however, it is assumed that the grid frequency is kept constant, which does not require an adaptative mean average filter.

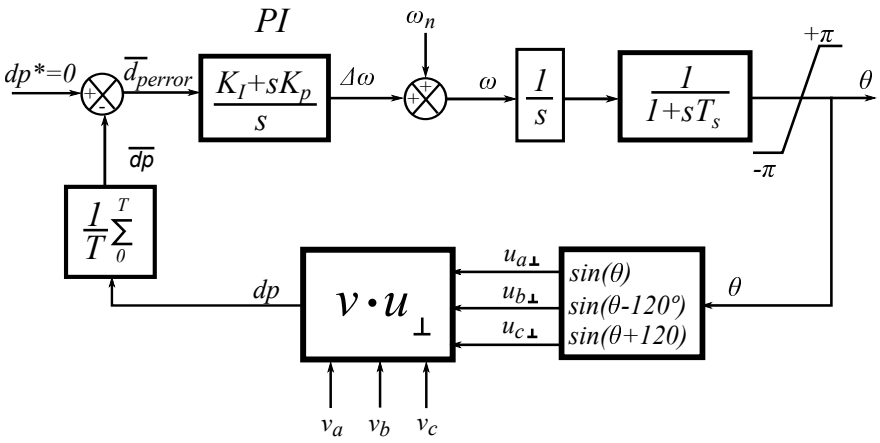


Figure 5.4 – PLL algorithm block diagram.

According to (PÁDUA; DECKMANN; MARAFÃO, 2005), the PI regulator design can be implemented through (5.5)-(5.6), in which ω_{bw} is the cut-off frequency of compensated open-loop transfer function, which should be between 5-10 Hz and ξ is the damping factor (which must be between 0 and 1). In this project, ω_{bw}=10 Hz and ξ=1 to avoid excessive overshoot. Figure 5.5 shows the obtained waveforms after the implementation of the PLL algorithm, in which $PLL_{ph-a}(t)$ and $V_a(t)$ are the reference signal synthesized by the PLL and the phase A voltage, respectively. The variable ω_{PLL} and ω_{ref} represent the instantaneous and reference values for the grid angular frequency. As can be observed, the digital PLL can satisfactorily track the established reference signals.

$$K_P = 2\xi\omega_b w = 125.66 \tag{5.5}$$

$$K_I = \omega_b^2 w = 3947.8 \tag{5.6}$$

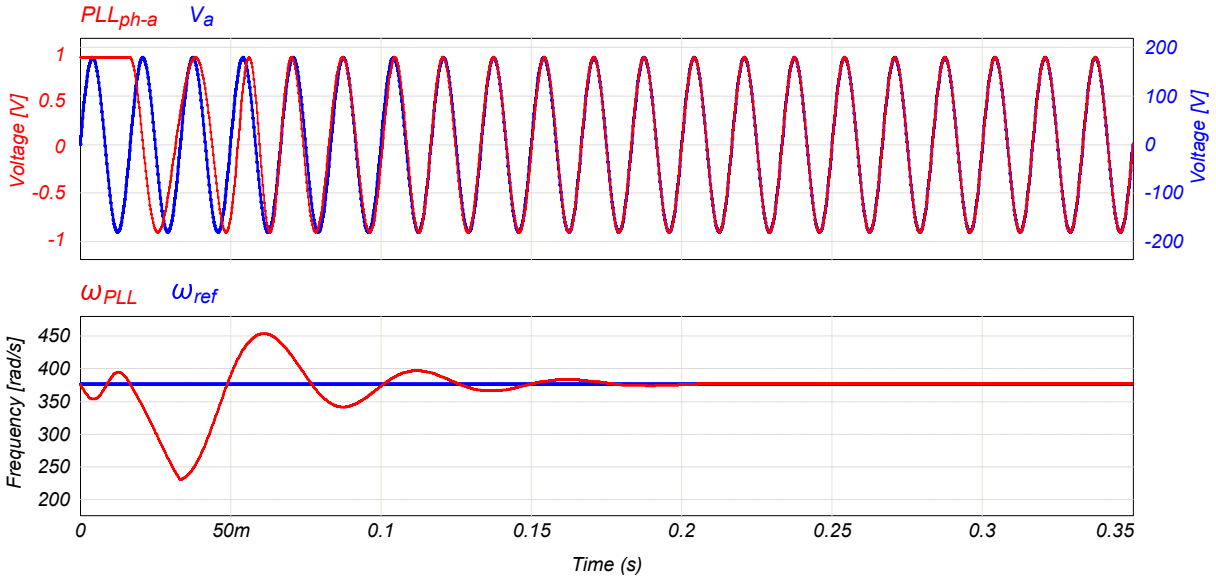


Figure 5.5 – PLL performance.

5.4 Inverter current controller design

The same methodology used to design the $V_{DC\,link}$ controller is adopted to design the inverter current controller $G_{inv}(z)$. Hence, the design process begins with the control requirements, listed below:

1. *Requirement 1*: The inverter current injection should have satisfactory disturbance rejection capability, for perturbations at the inverter input, load, and current signals reading noise. In this sense, the cut-off frequency for the closed-loop compensated system is defined at $f_{bw-ac} = \frac{f_s}{10}$ or 1.8 kHz (TEODORESCU et al., 2006).

2. *Requirement 2*: The current reference tracking should have fast dynamics with minimum overshoot and lower settling times, close to the deadbeat response, for the following current reference harmonic components: a) h_1=60 Hz; b) h_3=180; c)h_5=300 Hz; d)h_7=420 Hz; e)h_9=540 Hz; f) h_{11}=660 Hz and g) h_{13}=780 Hz.

3. *Requirement 3*: For active power injection, the injected current must be in phase with grid voltage, with unity power factor.

The control design is performed at the frequency domain, and the equivalent system block diagram is shown in Figure 5.6. The current controller is first designed in the s domain and afterward, it is discretized to the z domain, as in the case of $G_{C-link}(s)$. The design methodology is briefly presented in the following steps:

- *Step 1: Gathering of all the necessary transfer functions*: Table 5.3 summarizes the necessary transfer functions to design $G_{inv}(s)$. To determine $G\frac{\tilde{i}_{Lf}(s)}{M(s)}$ it is necessary to define the line impedance r_g. Considering that the QSY inverter is located 50 meters away

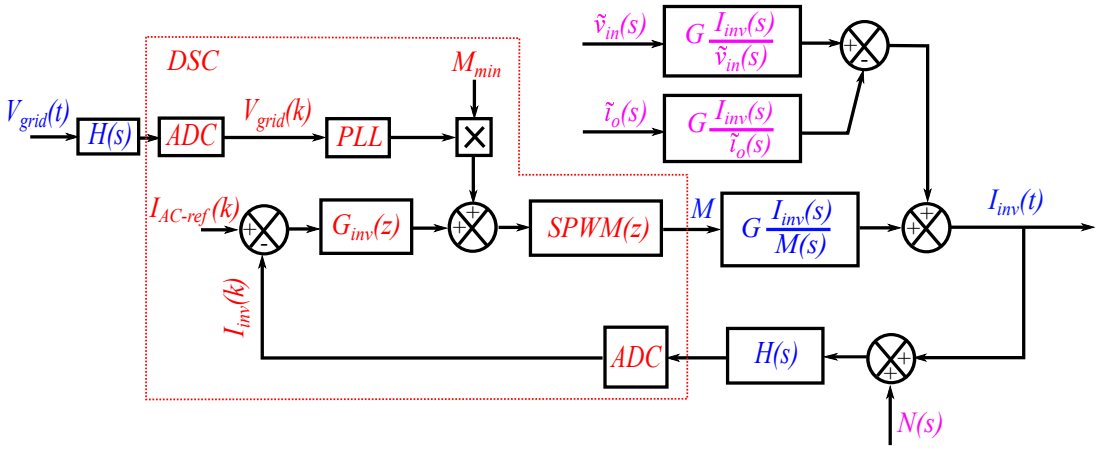


Figure 5.6 – Inverter per-phase current control loop block diagram.

from PCC, and it is connected with a 2.5 mm^2 cable with a resistivity of 17.241 $\frac{\Omega \cdot mm^2}{km}$ the equivalent line resistance is defined as r_g=0.345 Ω, according to (SANTOS, 2005).

Table 5.3 – Variables required for the inverter current control design.

Variable	**Value**
$G\frac{\tilde{i}_{Lf}(s)}{M(s)}$	$\frac{300}{0.684 + s \cdot 6 \cdot 10^{-3}}$
$SPWM(s)$	$\frac{1 - \frac{s}{72 \cdot 10^3}}{1 + \frac{s}{72 \cdot 10^3}}$
$H_{ADC}(s)$	$\frac{1}{1 + 33 \cdot 10^{-6} s}$
f_s, f_{bw-ac}	18 kHz, 1.8 kHz

- *Step 2: Design of Proportional-resonant controller*: In many DC-AC applications, the utilization of proportional-resonant (PRes) controllers are found, due to its inherent simplicity and flexibility to tune specific resonant frequencies. The formulation of the PRes controller is given by (5.7), where h stands for the syntonized harmonic orders, w_o is the fundamental grid angular frequency, K_{ih} is the resonant gain for each harmonic frequency and K_{Pi} is the proportional gain. The K_{Pi} factor is calculated such that the desired phase and gain margins are achieved (AYAD et al., 2016). To design the PRes controller, it is necessary to know the inverter current-control open-loop gain $T_{INV}(s)$, calculated as (5.8). Using the values shown in Table 5.3, the first step is to calculate K_{Pi}, given by (5.9), where ω_{LFbw} is the cut-off frequency of the anti-alias $H_{ADC}(s)$ low-pass filter. The objective of calculating K_{Pi} is to set $T_{INV}(s)$ bandwidth to $\omega_{ci} = 2\pi\frac{f_s}{10}$. With K_{Pi} calculated, the resonant gain K_{ih} is calculated by (5.10), where $\frac{f_{AC}}{n_{oh}}$ represents the desired transient response in relation to the fundamental frequency, whose range varies from 0-1 (BUSO; MATTAVELLI, 2015) and here arbitrarily defined as 0.9. Now, each

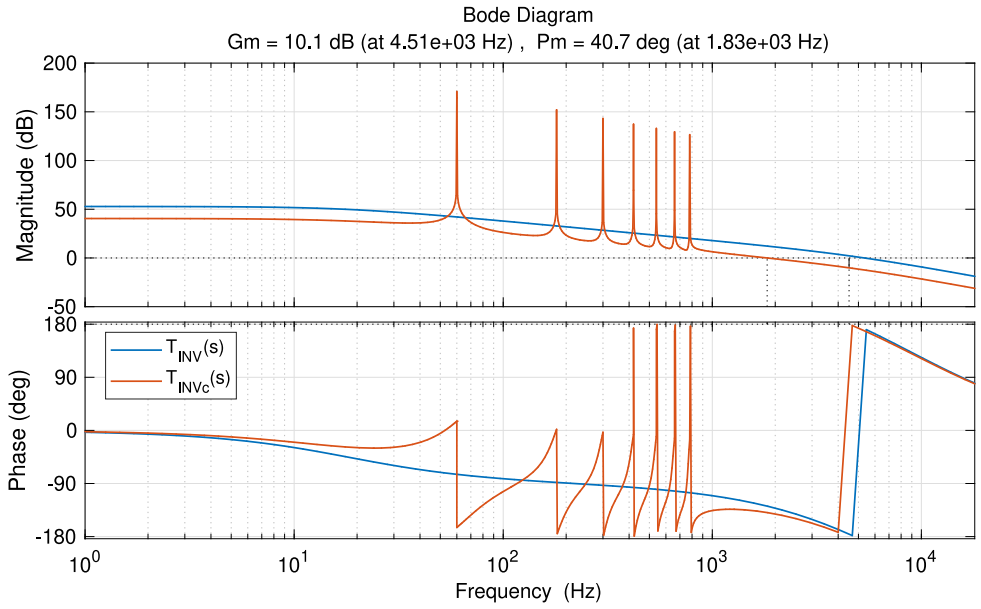


Figure 5.7 – Uncompensated and compensated open-loop gain $T_{INV}(s)$ comparison.

resonant term is calculated according to (5.7). The bode plots of the uncompensated and compensated inverter current-control open-loop gains, $T_{INVu}(s)$ and $T_{INVc}(s)$, respectively, are shown in Figure 5.7. It can be seen that $T_{INV}(s)$ bandwidth is defined at 1830 Hz, which is slightly higher than 1800 Hz. This difference occurs due to the addition of the resonant terms but is still tolerable, considering that ω_{ci} can vary from up to $2\pi\frac{f_s}{6}$ (TEODORESCU et al., 2006). A high gain is noticeable for the following harmonics h_1, h_3, h_5, h_7, h_9, h_{11} and h_{13} (> 100 dB), which allows fast-reference tracking capability. The relatively low phase margin of 40.7° would present a ringing response with a non-desirable overshoot. To compensate for this problem, as can be seen in Figure 5.6, a feed-forward modulation sinusoidal reference with an amplitude of M_{min}=0.6 is summed with the resonant controller output, since this value is the minimum required to maintain inverter current injection to the grid, as can be seen in 5.3b.

$$G_{inv}(s) = K_{Pi} + \sum_{h=1,3,5,\ldots}^{K_h} \frac{2K_{ih}s}{s^2 + (hw_o)^2} \tag{5.7}$$

$$T_{INV}(s) = G_{inv}(s) \cdot SPWM(s) \cdot G\frac{\tilde{i}_{Lf}(s)}{M(s)} \cdot H_{ADC}(s) \tag{5.8}$$

$$K_{Pi} = \frac{2\sqrt{(r_{Lf}+r_g)^2 + (\omega_{ci}L_f)^2}\sqrt{1+\left(\frac{\omega_{ci}}{\omega_{LFbw}}\right)^2}}{V_{DC\,link}} = \frac{2\sqrt{0.684^2 + (2\pi\cdot 1800\cdot 0.006)^2}\sqrt{1+\left(\frac{1800}{4823}\right)^2}}{600} = 0.24145 \tag{5.9}$$

$$K_{ih} = \frac{2.2 \cdot K_{Pi} \cdot f_{AC}}{n_{oh}} = \frac{2.2 \cdot 0.241 \cdot 60}{0.9} = 35.41 \tag{5.10}$$

- *Step 3: Evaluation of controller performance*: With the PRes controller designed, an evaluation of its performance is needed, regarding compliance with the control

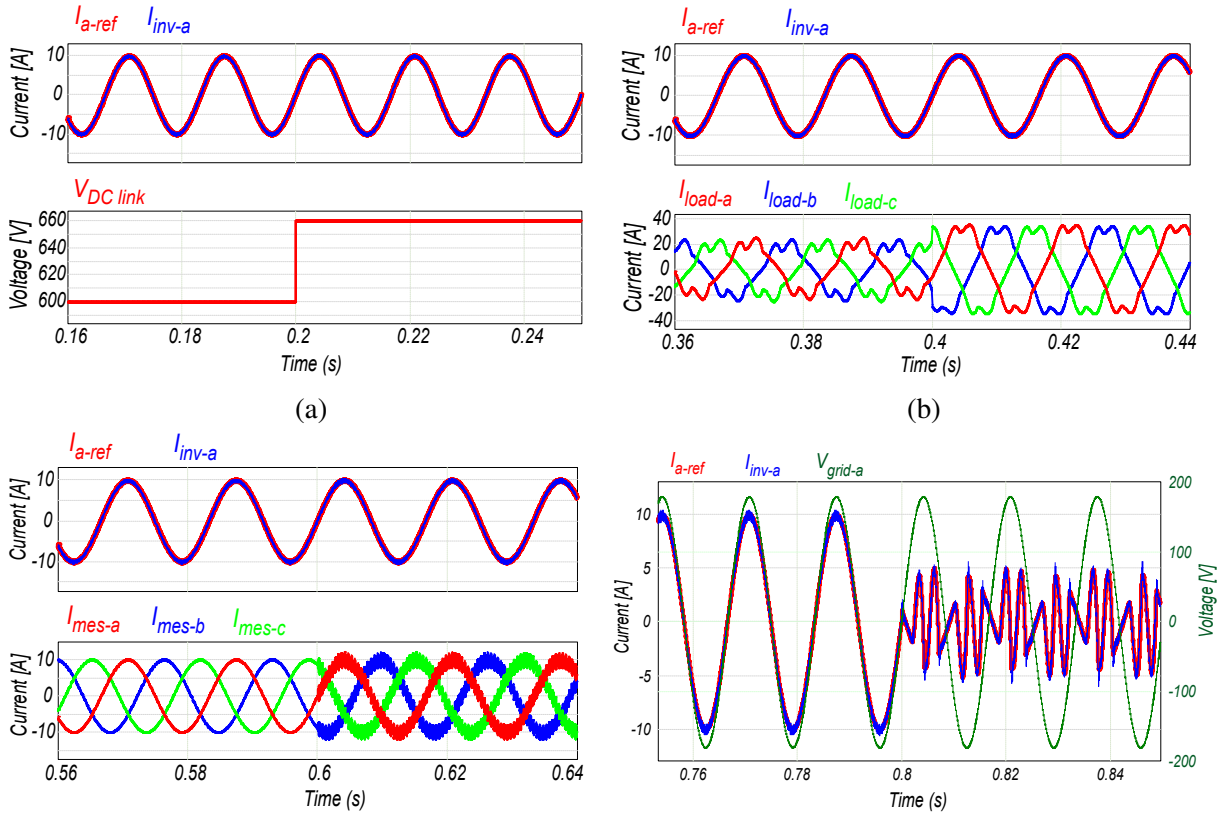


Figure 5.8 – PRes controller performance under external disturbances: a)DC link voltage variation; b) Load current increase; c) Current measurement high-frequency noise; d) Reference tracking change (active to non-active current injection).

requirements. Figure 5.8 shows the current reference capability of the designed controller under the different external disturbances. It is considered in the simulation system a standard VSI inverter, with constant DC link voltage, and resistive and inductive linear and non-linear loads (three-phase diode bridge rectifier) connected to the PCC bus. The purpose of this simulation is to evaluate the performance of the PRes controller, and in the next sections, the integration with other controllers is made. The shown results indicate only phase A, for simplicity, since phases B and C present the same behavior. It can be seen that the controller has satisfactory disturbance rejection capability, for input (Figure 5.8a), load (Figure 5.8b), and current measurement high-frequency noise (Figure 5.8c), keeping the reference tracking capability even in the presence of external perturbations, satisfying control requirement 1. In Figure 5.8d it can be seen that before 0.8 s, the injected current (active current injection) is in phase with grid voltage V_{grid-a}, with unity power factor, satisfying control requirement 3. After 0.8 s, load non-active current components are injected with satisfactory current reference tracking, satisfying control requirement 2.

- *Step 4: Controller discretization*: Lastly, the digital controller formulation is obtained using the bilinear transform, according to Table 4.4. The $G_{inv}(z)$ controller is divided

Table 5.4 – Digital coefficients of the PRes transfer functions.

Transfer function	a_0	a_1	a_2	b_1	b_2
$P_{ress\,1}(z)$	241.446545245404·10^{-3}	70.8243199386519	34.3149391523788·10^{3}	0	142.122303375687·10^{3}
$P_{ress\,3}(z)$	1.96540244605492·10^{-3}	444.089209850063·10^{-18}	-1.96540244605548·10^{-3}	-1.99605605076144	1
$P_{ress\,5}(z)$	1.96196338649746·10^{-3}	0	-1.96196338649757·10^{-3}	-1.98906375522367	1
$P_{ress\,7}(z)$	1.95682730432511·10^{-3}	0	-1.95682730432511·10^{-3}	-1.97862107348003	1
$P_{ress\,9}(z)$	1.95002087933049·10^{-3}	222.044604925031·10^{-18}	-1.95002087933072·10^{-3}	-1.96478225088260	1
$P_{ress\,11}(z)$	1.94157914510540·10^{-3}	0	-1.94157914510529·10^{-3}	-1.94761851772599	1
$P_{ress\,13}(z)$	1.93154504337467·10^{-3}	222.044604925031·10^{-18}	-1.93154504337456·10^{-3}	-1.92721718312131	1

into seven z domain transfer functions, each one being a second-order function, namely $Press_1(z)$-$Press_7(z)$. The $P_{ress\,1}(z)$ corresponds to the discretization of $K_{pi} + \frac{2K_{1h}s}{s^2+\omega_o^2}$, and the remaining transfer functions are related to the discretization of the third to eleventh harmonic terms, respectively. This procedure was done to avoid instability due to the discretization of the ideal PRes formulation. Hence, the a_0, a_1, a_2 and b_0, b_1, b_2 coefficients of each transfer function are given in Table 5.4.

5.5 Summary

In this chapter the inverter current controller was designed. To obtain the required transfer functions, the inverter low-pass output filter was defined and a PLL strategy was selected and explained. The inverter current to control transfer function was obtained and the permissible operating region as inverter was defined, based on the minimum and maximum values allowable to the modulation index M.

With all the transfer functions properly established, the design methodology of $G_{inv}(z)$ was derived, and the controller performance is evaluated in terms of robustness against DC link, load current, and feed-back signal noise disturbances, including current reference modification. The simulated results confirmed the validity of the control methodology, with satisfactory results. With the DC link and inverter current controller designed, the methodology adopted to determine the MPPT controller is discussed in the next chapter.

6 MPPT control

With the DC link and inverter current controllers already defined, it is now necessary to define the MPPT control, which is responsible to extract the maximum power available from the PV panel. In this sense, the solar panel parameters and a proper design methodology must be established considering the specific characteristics of the QSY inverter, which is the scope of the present chapter.

6.1 Solar PV panel model

There are many PV models available in the literature and the one adopted in this work is based on the circuital method (VEERACHARY; KHAS, 2006), as it can be easily applied in a circuit simulation environment. Since the focus of this work does not intend to propose a model design methodology for the PV panel, a standard PV block available at PSIM is used to model the PV characteristics. In this work, the PSIM block used to represent the solar PV panel is based on the functional model, in which the solar PV panel is modeled by four parameters: a) Maximum power voltage V_m, defined as 250 V; b) Maximum power current I_m = 12 A, such that the maximum power available is 3 kW; c) Open-circuit voltage V_{oc} defined as 20% higher than V_m (V_{oc}=300 V); iv) Short-circuit current I_{sc}, defined as 8% higher than I_m (I_{sc}=13 A). As can be seen in Figure 6.1, the maximum power occurs at 250 V and 12 A, such that 3 kW is obtained, which matches the specified parameters and is sufficient for the conduction of further simulations.

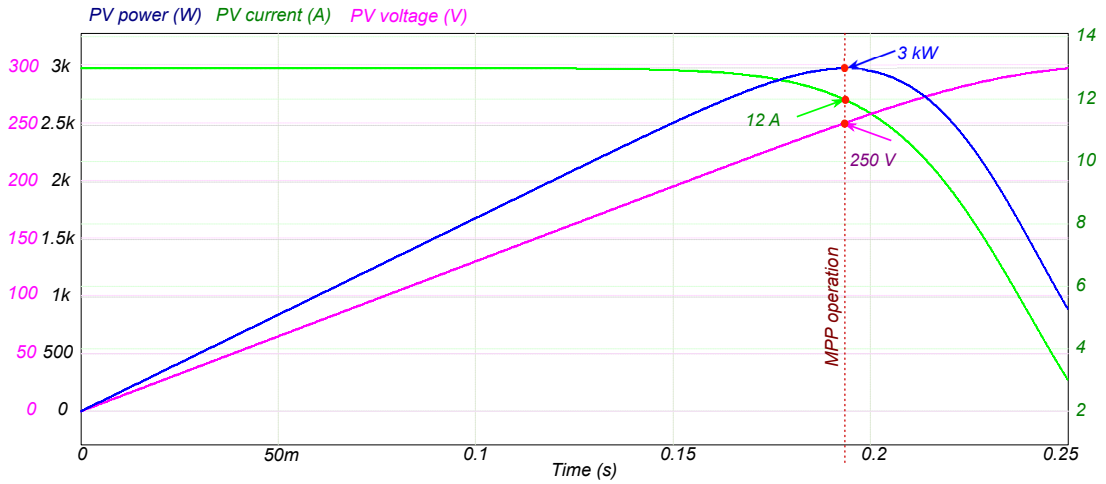


Figure 6.1 – Performance of equivalent 3 kW PV arrangement.

6.2 MPPT strategy with QSY inverter

In this work the Perturb and Observe (PO) method is adopted as an MPPT strategy. The PO method operates by increasing or decreasing the PV array's output terminal voltage based on comparing the instantaneous and previously calculated power. If the voltage varies and the power increases, the control system changes the operating point in that direction; otherwise, it changes the operation point in the opposite direction. Once the direction for the change of voltage is known, the voltage is varied at a constant rate. This rate is a parameter that should be adjusted to allow the balance between faster response and less fluctuation in the steady state (BRITO et al., 2012). Figure 6.2 shows the flowchart of the PO MPPT method.

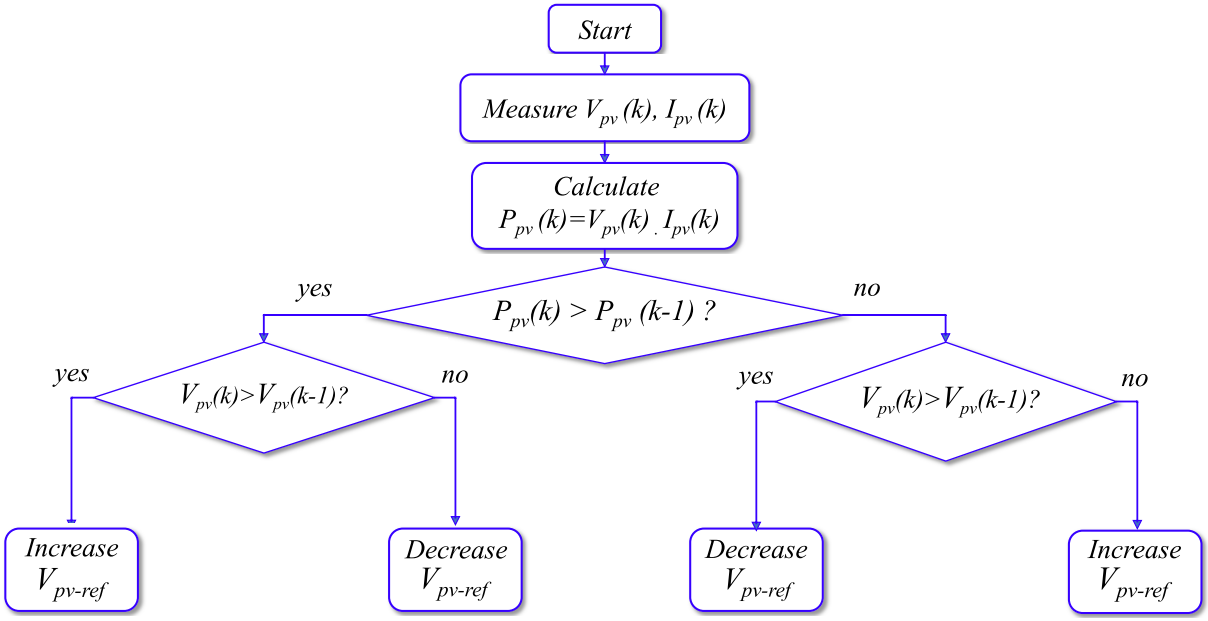


Figure 6.2 – PO MPPT method flowchart.

Figure 6.3 shows the block diagram of the MPPT closed-loop control system. Through the measurement of PV panel's current I_{pv} and voltage V_{pv}, the MPPT PO determines the PV panel voltage reference $V_{pv}^{*}(k)$ which is compared to the instantaneous reading of $V_{pv}(k)$. Based on the error between these readings, the MPPT controller $G_{mppt}(z)$ determines the amplitude of the inverter output current $I_{mppt-ref}(k)$. It is worth mentioning that during the practical implementation the voltage reference $V_{pv}^{*}(k)$ is subtracted from V_{pv}, since the input voltage increases as the inverter output current decreases, and vice-versa. The value of $I_{mppt-ref}(k)$ is then multiplied by the sine wave generated by the PLL algorithm, such that the reference current $I_{AC-ref}(k)$ of the inverter is in phase with grid voltage $V_{grid}(t)$. The inverter current reference is then compared with the instantaneous measurement of the inverter current $I_{inv}(k)$ and the inverter current controller $G_{inv}(z)$ determines a modulation index M for the inverter, such that inverter current follows the reference.

However, since the MPPT controller bandwidth is lower than the inverter current controller, there is a dynamic decoupling between these two control loops. In this sense, the

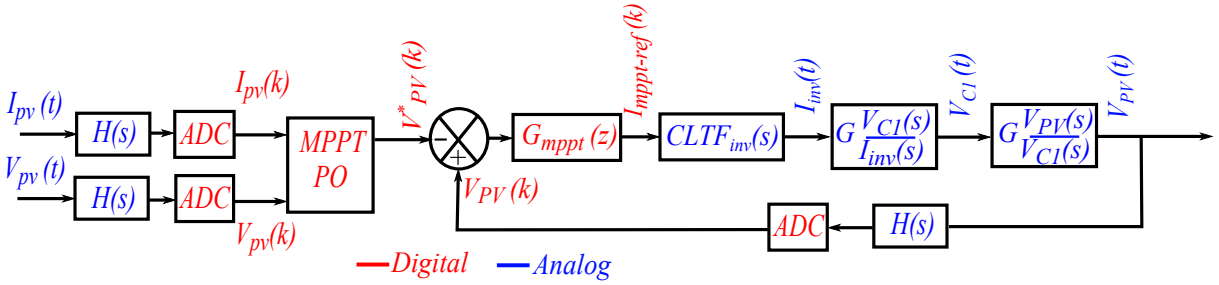


Figure 6.3 – Block diagram used to design $G_{mppt}(z)$.

inverter current control closed-loop system is represented by $CLTF_{inv}(s)$. As in the case of the DC link voltage control, the goal is that the MPPT closed-loop system remains immune to most external disturbances, which is achieved by the design of $G_{mppt}(z)$. Before the controller design, it is necessary to define the required transfer function in the s domain, since the control design will be made on the s domain with a further discretization to the z domain, as done in the previous chapters.

6.3 MPPT controller design considerations

To implement the MPPT algorithm, shown in Figure 6.2, three control options are available for the QSY inverter: a) The control of the input current $I_{Lin}(t)$, since the QSY inverter has a continuous current input nature; b) The control of the DC link voltage $V_{DC\,link}$, using the control scheme presented in Chapter 4; c) The control of the modulation index M, such that the inverter current is controlled to extract the maximum power. In the first two options, the QSY network will be controlled to extract the maximum power from PV arrays, while the inverter bridge is controlled to inject current into the grid and maintain the DC link voltage at the desired level.

The first two control schemes are similar to the conventional control strategies for most PV inverters found in the literature. In the third option, however, the QSY network is controlled to regulate the DC link voltage while the inverter is commanded to extract the maximum power from PV arrays. In this work, the third option will be used, since the control of both I_{Lin} or $V_{DC\,link}$ variables depends on the regulation of D_{st}, which is challenging due to the non-minimum phase characteristics of the converter and restricted control bandwidth. However, the regulation of $V_{DC\,link}$ is easier to attain, while the inverter current control has faster dynamics, as shown in the previous chapter. That is why the MPPT tracking is more conveniently obtained with the third strategy, considering the inherent characteristics of the QSY inverter.

To design $G_{mppt}(z)$, the block diagram shown in Figure 6.3 is used, where: a) $CLTF_{inv}(s)$ is the closed-loop transfer function of the inverter current control loop; b) $G\frac{V_{VC1}}{I_{inv}(s)}$ is the V_{C1} to inverter current $I_{inv}(s)$ transfer function; c) $G\frac{V_{PV}(s)}{V_{C1}(s)}$ is the input voltage, in this case, the PV array voltage V_{PV} to V_{C1} transfer function. The $CLTF_{inv}(s)$ transfer function is

straightforwardly obtained by (6.1), by inspecting Figure 5.6. The $G\frac{V_{PV}}{V_{C1}(s)}$ is also promptly obtained considering that when $V_{DC\,link}$ is regulated at the desired value, the relationship between V_{C1} and V_{PV} is given by (6.2). With these two transfer functions obtained, the discussion can be forwarded to the calculation of $G\frac{V_{VC1}(s)}{I_{inv}(s)}$.

$$CLTF_{inv}(s) = \frac{T_{INV}(s)}{H_{ADC}(s)(1 + T_{INV}(s))} \tag{6.1}$$

$$G\frac{V_{PV}(s)}{V_{C1}(s)} = \frac{1}{B(1 - D_{st})} \tag{6.2}$$

6.4 Determination of $G\frac{V_{VC1}(s)}{I_{inv}(s)}$

Through the power conservation principle and neglecting power losses, one can write (6.3), where $\overline{V_{PV}}$ and $\overline{I_{Lin}}$ are the average value of PV array voltage and QSY network input current, respectively, and $\overline{V_{DC\,link}}$ and $\overline{I_{DC\,link}}$ are the average values of voltage and current at the DC link, respectively. Since $\overline{V_{DC}} = B\overline{V_{PV}}(1 - D_{st})$, (6.3) can be further developed such that (6.4) is obtained.

$$\overline{V_{PV}} \cdot \overline{I_{Lin}} = \overline{V_{DC\,link}} \cdot \overline{I_{DC\,link}} \tag{6.3}$$

$$\overline{I_{DC\,link}} = \frac{\overline{I_{Lin}}}{B(1 - D_{st})} \tag{6.4}$$

Now, evaluating the inverter side, one can write (6.5) using the power conservation principle, again not considering power losses, where V_{ll-rms} and $I_{inv-rms}$ are the inverter line-to-line voltage and phase current rms values, respectively. Moreover, PF is the power factor observed at the inverter output. Considering that the inverter is only injecting active power into the grid, the PF value is 1, as demonstrated in Figure 5.8. Now, V_{ll-rms} can be written as (6.6) and $V_{DC\,link}$ can be described as (6.7). Now, with the Simple Boost Control modulation, the linear modulation index M is defined as $M = 1 - D_{st}$, as shown in Table 4.1. Therefore, substituting (6.6) and (6.7) in (6.5) one obtain (6.8), which represents the relationship between the DC link and AC phase rms current.

$$\overline{V_{DC\,link}} \cdot \overline{I_{DC\,link}} = \sqrt{3} \cdot V_{ll-rms} \cdot I_{inv-rms} \cdot PF \tag{6.5}$$

$$V_{ll-rms} = \frac{MV_{DC\,link}\sqrt{3}}{2\sqrt{2}} \tag{6.6}$$

$$V_{DC\,link} = \frac{\overline{V_{DC\,link}}}{1 - D_{st}} \tag{6.7}$$

$$\overline{I_{DC\,link}} = \frac{3I_{inv-rms}}{2\sqrt{2}} \tag{6.8}$$

Yet, considering a low ripple content at the input current, it can be stated that $\overline{I_{Lin}} \approx I_{Lin-rms}$. Moreover, I_{C1-rms} can be ideally described as $I_{Lin-rms}(\delta - 1)$ and $\overline{I_{Lin}}$ can be written as (6.9). Hence, substituting (6.9) in (6.4), and the resulting expression in (6.8), one can obtain (6.10). Applying Laplace transform in (6.10) and manipulating the terms, one obtain the $G\frac{V_{VC1}}{I_{inv}(s)}$ transfer function, given by (6.11).

$$\overline{I_{Lin}} = \frac{I_{C1rms}}{\delta - 1} \tag{6.9}$$

$$\frac{I_{C1rms}}{B(\delta - 1)(1 - D_{st})} = \frac{3I_{inv-rms}}{2\sqrt{2}} \tag{6.10}$$

$$G\frac{V_{VC1}(s)}{I_{inv}(s)} = \frac{3(\delta - 1)(1 - D_{st})B}{2\sqrt{2}C_1 s} \tag{6.11}$$

With all the transfer functions obtained, it is now possible to determine the design methodology of the MPPT controller $G_{mmpt}(z)$

6.5 Design of $G_{mppt}(z)$

Using the same controller design methodology adopted for DC link and inverter current control, the requirements for the MPPT controller are given below:

1. *Requirement 1*: The controller dynamics must allow a low overshoot ($\leq$ 10 %) with a settling time lower than five grid frequency cycles ($\leq$ 80 ms), such that a smooth MPP tracking is obtained.

2. *Requirement 2*: The $G_{mppt}(z)$ controller bandwidth should be lower than $G_{inv}(s)$, to allow controller dynamics decoupling. In this sense, the $G_{mppt}(z)$ bandwidth should be lower than $\frac{f_s}{100}$=180 Hz.

3. *Requirement 3*: Since the dynamics of solar PV panel reference voltage definition, as the MPPT PO algorithm is executed, is similar to a ramp, it is desired that the steady-state error for ramp control reference input should be null.

The controller design is again performed at the frequency domain, using the system block diagram shown in Figure 6.3. The design methodology is briefly presented in the following steps:

- *Step 1: Gathering of all the necessary transfer functions*: Table 6.1 presents the necessary transfer functions, given numerically. It is worth mentioning that, due to the dynamic decoupling, $CLTF_{inv}(s)$ is seen by the closed-loop control as a constant value of 0.99.

Table 6.1 – Variables required for the MPPT controller design.

Variable	**Value**
$CLTF_{inv}(s)$	0.99
$G\frac{V_{VC1}(s)}{I_{inv}(s)}$	$\frac{11.6}{758 \cdot 10^{-6}s}$
$G\frac{V_{PV}(s)}{V_{C1}(s)}$	$517.2128 \cdot 10^{-3}$
$H_{ADC}(s)$	$\frac{1}{1+33 \cdot 10^{-6}}$
$f_{bw-mppt}$	$\leq$ 180 Hz

- *Step 2: Open-loop gain $T_{mppt}(s)$ analysis*: The open-loop gain transfer function for the MPPT controller design $T_{mppt}(s)$ is defined as (6.12). For the uncompensated case, $G_{mppt}(s)$=1, and the bode-plot for this condition is shown in Figure 6.4, given by the trace $T_{mppt-u}(s)$. It can be seen that the system bandwidth is higher than desired (f_{bw}=1.25 kHz) and the uncompensated $T_{mppt}(s)$ is a type 1 system, with non-zero error for ramp input. In this sense, the adoption of $G_{mppt}(z)$ as a PI controller, such that the compensated system overshoot value if lower than 10% is a solution for this control problem.

$$T_{mppt}(s) = G_{mppt}(s) \cdot CLTF_{inv}(s) \cdot G\frac{V_{VC1}(s)}{I_{inv}(s)} \cdot G\frac{V_{VC1}}{I_{inv}(s)} = \frac{5.94}{758 \cdot 10^{-6}s} \tag{6.12}$$

- *Step 3: $G_{mppt}(s)$ design*: The design of $G_{mppt}(z)$ is made using MATLAB Control System Designer utility. Using the PID Tunning method, and choosing the frequency domain design method, with f_{bw}=90 Hz and phase-margin of 90º, the $G_{mppt}(z)$ controller is derived with a formulation given by (6.13). The bode-plot for the compensated system is shown in Figure 6.4, looking at the $T_{mppt-c}(s)$ trace, and it can be seen that f_{bw} ≈90 Hz with a phase-margin close to 90 °, which is acceptable considering the control requirements.

$$G_{mppt}(s) = 0.71422\frac{1+0.1s}{s} \tag{6.13}$$

- *Step 4: $G_{mppt}(s)$ performance evaluation*: Figure 6.5 shows the simulation results obtained with the implementation of the $G_{mppt}(s)$ controller designed in Step 3. This simulation case represents the conventional operation of a PV inverter, that is, only active power is delivered to the grid. At first, the QSY inverter is initialized without the DC link and inverter current control loops, with a three-phase resistive load of 70 Ω connected at its output. At this moment, the QSY inverter is not connected to the grid, and the purpose

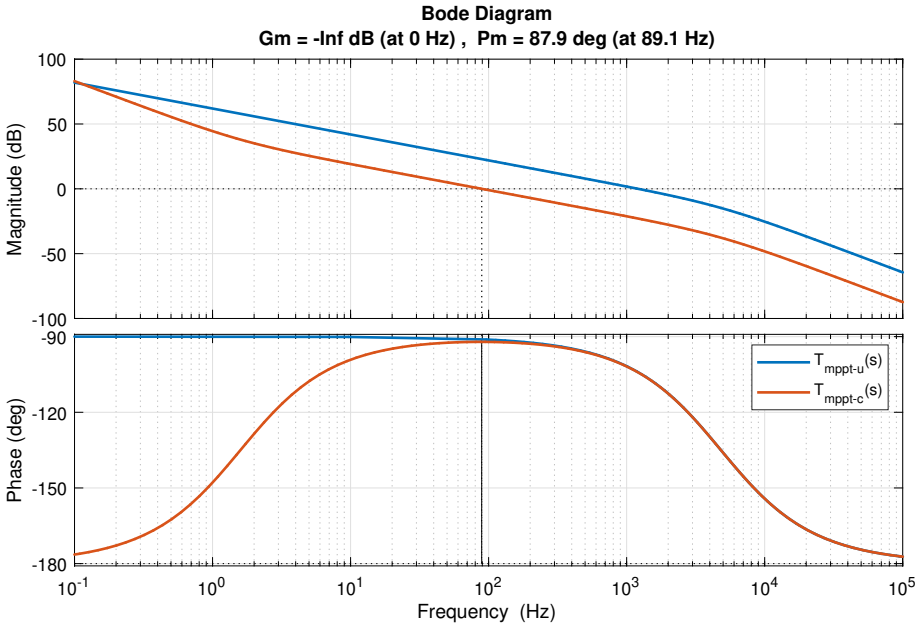


Figure 6.4 – Uncompensated $T_{mppt-u}(s)$ and compensated open-loop gain $T_{mppt-c}(s)$ bode-plots.

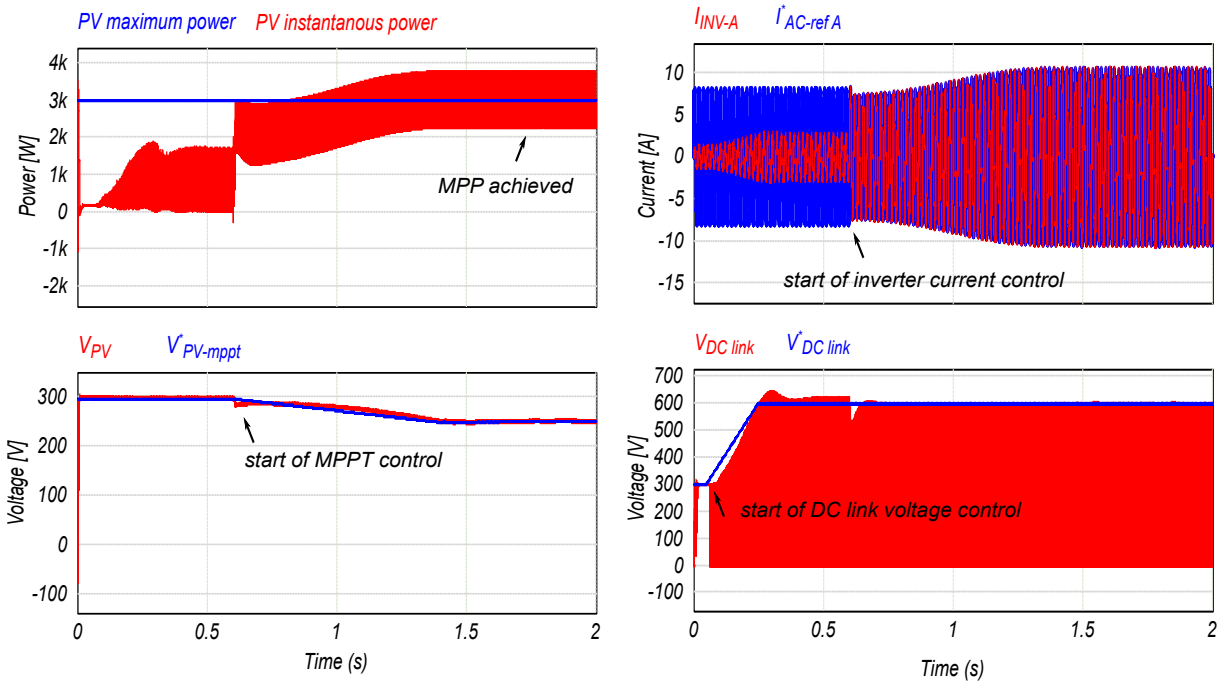


Figure 6.5 – MPPT controller simulation results.

of adopting the resistive load is to properly initialize the DC link and inverter current controllers before the inverter grid connection, besides allowing continuous conduction mode at the converter input [1]. The DC link control loop is initialized at 0.05s, with a voltage reference increasing with ramp dynamics. Once the DC link is regulated at 600 V, then the

[1] This initialization procedure is adopted for the cases analyzed in current chapter and chapter 7. It is beyond the scope of this work to evaluate different scenarios, such as those where the initialization occurs under different irradiation levels.

inverter output current controller is started at 0.6 s, and the inverter is connected to the grid. At this same time, the resistive load is disconnected from the inverter output, and the MPPT controller loop is initialized, such that the current reference for the inverter output current is gradually increased, to extract more power from the PV array. Before 0.6 s, the MPPT current reference tracking is not enabled, which is why I_{INV-A} is not following $I^*_{AC-ref-A}$ before 0.6 s. It can be seen that the PV instantaneous power reaches the maximum power available for the PV at 1.5 s approximately. This is achieved through the regulation of inverter output current I_{inv}, which is gradually increased when following its reference current I^*_{AC-ref}. As the PV array output power increases, the solar PV panel voltage V_{PV} slowly decreases, following the MPPT PO reference voltage $V^*_{PV-mppt}$. Moreover, the DC link voltage remains regulated and tracks $V^*_{DC\,link}$ along the entire process. The simulation results show that all the MPPT controller design objectives are satisfactorily met.

- *Step 5: Controller discretization*: Finally, the digital formulation of $G_{mppt}(s)$ is obtained using the bilinear transform (see Table 4.4). Expression (6.14) shows the z domain expression for the $G_{mppt}(z)$, with digital coefficients given by b_0=71.4418394444445 $\cdot 10^{-3}$, b_1=-71.4021605555556 $\cdot 10^{-3}$, a_0=1; a_1=-1, respectively.

$$G_{mppt}(z) = \frac{0.07144z - 0.0714}{z - 1} \tag{6.14}$$

6.6 Summary

In this chapter the MPPT controller design methodology was presented. The solar PV panel specifications and model approach, using PSIM, were specified. The justification for the MPPT strategy using the QSY inverter was presented, such that the MPPT was executed by the inverter, and the QSY network is controlled to regulate the DC link at the desired value. The required transfer functions for the MPPT controller were found and a methodology for the controller design, including dynamics requirements definitions was given.

The obtained simulation results confirmed the validity of the proposed control approach. In the next chapter, a simulation case is carried out, with all the designed control loops of the previous chapter being executed simultaneously considering the intended application for the QSY inverter.

7 Simulation results

In this chapter the multifunctional QSY PV inverter is tested considering the system depicted in Figure 7.1, which represents a typical commercial or small-scale industry environment. As can be seen in Figure 7.1a, connected to the point of common coupling (PCC) there are reactive, non-linear, and resistive loads. These loads may represent induction machines, capacitive banks for power-factor compensation, welding machines, and industrial ovens or heaters, respectively. All load currents are measured at phases A and C, respectively, with phase B current obtained mathematically. This same procedure to obtain phase B current is done at the grid and inverter sides.

The PCC line voltages V_{AB} and V_{BC} are measured and V_{CA} is obtained mathematically. The QSY inverter is connected with the PCC when the breaker B_1 is switched on. All voltages and current measurements are sent to the digital controller system, which determines the inverter switching pattern $S_1 - S_6$. All closed-loop control systems analyzed and designed in the previous sections are shown together and interconnected, with power quality indexes measurement for the inverter and grid sides, respectively.

Figure 7.1b also shows the digital control architecture, which employs all the closed-loop systems designed in the previous chapters, clearly indicating the connections among the different loops. Furthermore, to allow the realization of ancillary services and enable the multifunctional operation of the QSY PV inverter, the Conservative Power Theory (CPT) is employed. CPT theory presents several advantages for ancillary services execution, such as selectivity, flexibility, and currents reference synthetization without the need to make transfers of coordinates or implement any algorithms of synchronization, and it has been used for this purpose in several works in the literature (BRANDAO et al., 2016), (PAREDES et al., 2021), (ALONSO et al., 2020).

A CPT-based current decomposition algorithm is represented by the block labeled as 'CPT' in Figure 7.1b, and it delivers at its output several current references, different power parcel measurements, and power quality indexes. Due to the CPT selectivity capability, load three-phase active unbalanced $I_{act-unbal-a,b,c}$, reactive unbalanced and balanced - given by $I_{re-unbal-a,b,c}$ and $I_{re-bal-a,b,c}$, respectively - and void $I_{void-a,b,c}$ current references are provided by CPT block. Each current reference can be adjusted by a respective gain factor, which can vary from 0-1, such that the inverter can partially or totally compensate for a certain current reference component. In this case, k_{au} is used to regulate active unbalanced reference current, k_r and k_{ru} for reactive balanced and unbalanced current references, and k_v for void current reference. Moreover, to evaluate the different power parcels measurements values along the system execution, two CPT blocks are used, which can deliver the readings of the grid (subscript g) and inverter (subscript

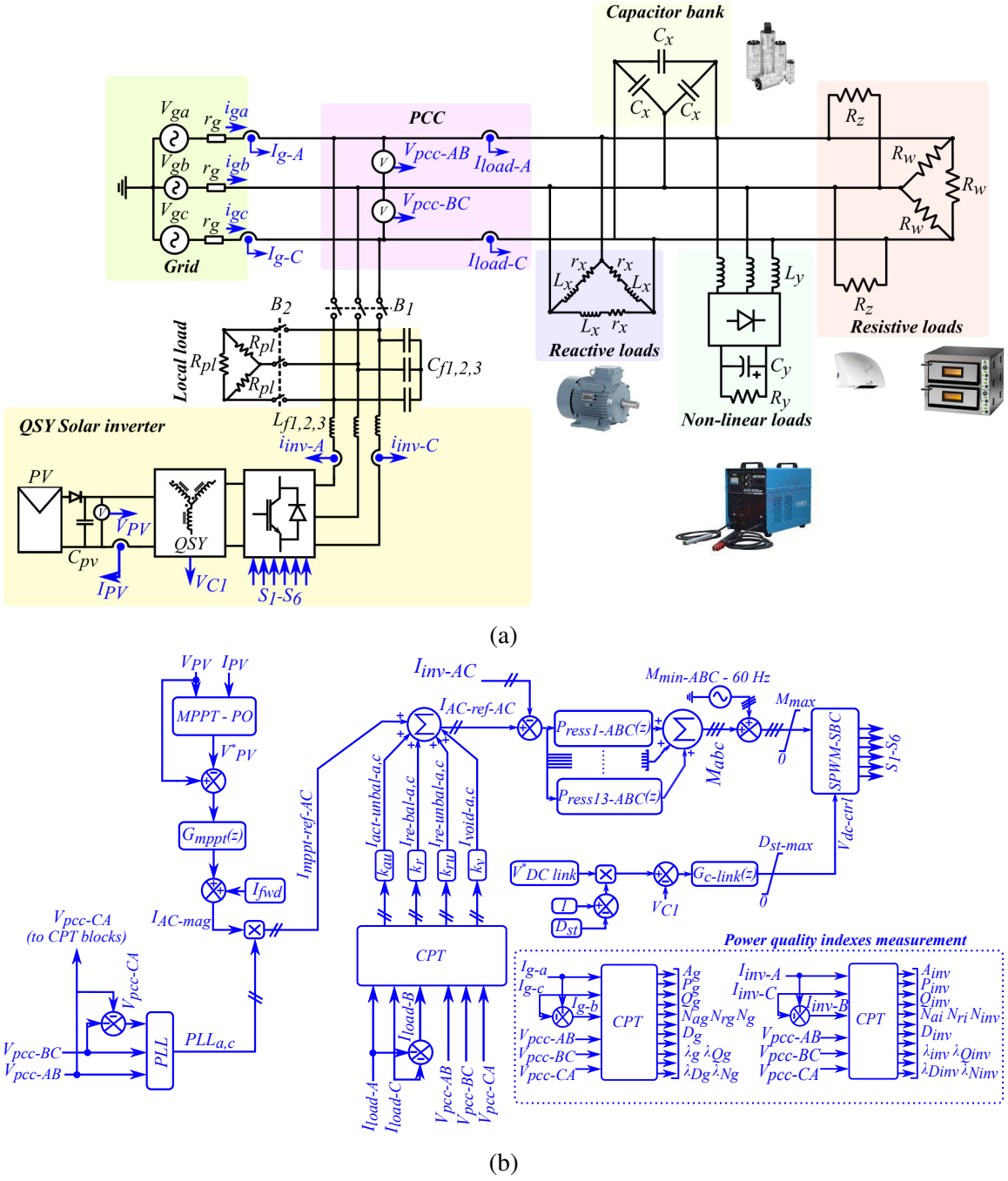


Figure 7.1 – Simulation case system configuration: a) Power system; b) Digital control system.

inv) sides. In this case, apparent (A_g, A_{inv}), active (P_g, P_{inv}), reactive (Q_g, Q_{inv}), unbalanced active (N_{ag}, N_{ainv}) and reactive (N_{rg}, N_{ri}) - including the total unbalance value (N_g, N_{inv}) - and residual (D_g, D_{inv}) power parcels measurements are available. Finally, the following power quality indexes, for grid and inverter sides, respectively, are informed by CPT blocks: power factor λ_g, λ_{inv}, reactivity factor λ_{Qg}, λ_{Qinv}; asymmetry factor λ_{Ng}, λ_{Ninv} and non-linearity factor λ_{Dg}, λ_{Dinv}. Additional details about the CPT definitions can be found in (PAREDES, 2011). The QSY PV inverter operates with the solar PV panel modeled in section 6.1, at nominal irradiation conditions with 3 kW power delivery capability.

The PCC loads configuration is shown in Table 7.1. Furthermore, the grid voltages are assumed to be balanced, with each phase having a peak value of 180 V and a frequency of 60 Hz. The line impedance is modeled as a resistance with vale r_g = 0.345 Ω. The QSY PV inverter parameters are the same as shown in Tables 3.3, 2.2 and 5.1, with the coupled-inductors core's leakage inductance represented at the tertiary winding with a value of L_k=1.08 μH.

To suppress the DC link peak voltages, an LCD snubber with L_s=250 μH and C_s=1 μF is used. The C_{pv} capacitor, which is connected across PV array terminals, is chosen to be 4.7 μ F since this allows a good compromise between ripple voltage suppression and MPPT tracking in this application. To avoid MPPT unstable response, due to noise in PV current and voltage measurements, and to obtain smooth MPP tracking, the PV voltage and current measurement sampling frequency was defined as 120 Hz [1]. Furthermore, the DC link, resonant, and MPPT controllers have the same parameters defined in the previous chapters.

Table 7.1 – PCC loads configuration.

Variable	**Value**	**Variable**	**Value**
r_x	1 Ω	L_y	1 mH
L_x	100 mH	C_y	470 μF
R_w	50 Ω	R_z	100 Ω
R_y	300 Ω	R_{pl}	300 Ω
L_y	1 mH	C_x	15 μF

Lastly, the goals of the simulations carried out in this chapter are: a) To propose a start-up methodology to properly initialize all the control loops of the QSY inverter, to allow the execution of ancillary services and MPPT; b) Evaluate the impact of the multifunctional operation on the QSY inverter, including the impacts of the execution of ancillary services and shoot-through on its components and MPPT performance. Therefore, the operational scenario depicted in Figure 7.1a, with the load parameters given in Table 7.1 were set such that the maximum apparent power capability of the inverter (3.75 kVA) and maximum modulation index M_{max} were respected. A more generic scenario study would demand the definition of a hierarchical architecture defined by layers, in which the QSY inverter would be contained in the most low-level layer (or primary layer), under the orientation of control commands coming from a secondary layer (BRANDAO et al., 2019), (ALONSO et al., 2022). This secondary layer is based on pre-established power quality and energy generation goals, and therefore it would send to the QSY inverter the appropriate current-references control commands, by properly adjusting the values of k_{au}, k_r, k_{ru}, k_v, while respecting the converter power capability, maximum modulation index, and MPPT constraints. However, the definition of this second layer and its associated control strategies are beyond the scope of this thesis.

[1] In practice, the utilization of additional low-pass digital filters, processing the measurements of I_{PV} and V_{PV}, are also useful to obtain a smooth and stable MPPT. Nonetheless, in the simulation environment, this is not necessary.

7.1 Control events

Prior to being connected with PCC, a predefined sequence of events is triggered, such that the converter control loops are executed correctly. This sequence of events is briefly described below:

1. *Stage I: t<0.1 s - open loop operation*: In this period, the QSY inverter is disconnected from the PCC, and the local load is connected to the inverter output. None of the control closed-loops are being executed, and the value of D_{st}=0.1944 and $V_{a,b,c}$=0.6. The purpose of this stage is to prepare the converter for the DC link voltage control.

2. *Stage II: t>0.1 s - DC link voltage control*: At 0.1 s, the DC link voltage control loop is turned on, and the DC link voltage is controlled until it reaches 600 V in steady-state. Only when the DC link voltage is regulated at the desired value, the inverter current control loop is initialized. It is necessary that the local load remain connected to the inverter output, otherwise, the DC link voltage will become excessively high and unstable since the stored energy in the impedance-source network has nowhere to flow.

3. *Stage III: t>0.4 s - Inverter current control*: With the DC link regulated, the inverter output current control loop is turned on at 0.4 s. A current of the amplitude of 2 A and 60 Hz is maintained as the inverter current control reference. The value of this reference current could be further adjusted such that the PV voltage becomes closer to an expected V_{mpp} value, which will increase the MPPT tracking response, but this is an optional adjustment and does not change the effectiveness of the proposed control strategy.

4. *Stage IV: t>0.5 s - PCC connection*: At this moment, both DC link and inverter current control loops are operating correctly. Hence, breaker B_1 is turned-on and the inverter is connected with the PCC. Breaker B_2 can be turned off if desired, to allow maximum power delivery at the PCC. Simultaneously, the MPPT control loop is turned on, hence the inverter current will gradually increase until the maximum power from the PV is extracted.

5. *Stage V: t>1.0 s - CPT-based current compensation*: After 1.0 s, the CPT algorithm is used to determine current components references for compensation. In this simulation, the active unbalanced, reactive (balanced and unbalanced), and void load current components are used as current references for the QSY PV inverter, that is $k_{au} = k_r = k_{ru} = k_v$ = 1, as shown in Figure 7.1. Naturally, the active current component at the inverter output is due to the MPPT tracking, thus the active balanced component from the CPT is not used.

7.2 Simulation results

Figure 7.2 shows the simulation results for the impedance-network side, particularly looking at the V_{C1}, $V_{DC\,link}$ and V_{PV} dynamics. It can be seen that along all stages, the DC link

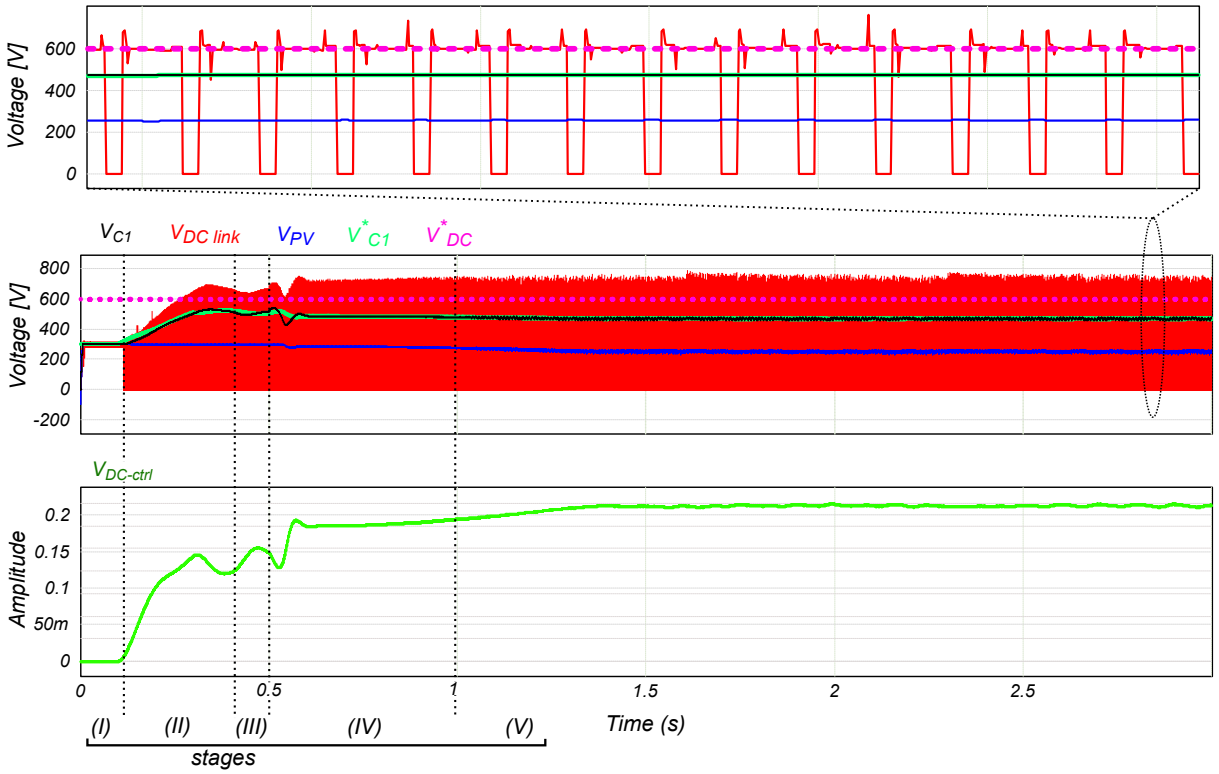


Figure 7.2 – Obtained V_{C1}, $V_{DC\,link}$ and V_{in} waveforms.

remains regulated at 600 V, as desired. At stage I, there is no shoot-through and the DC link regulation control signal $V_{DC-ctrl}$ remains equal to 0. Therefore, $V_{DC\,link} \approx V_{PV}$. In stage 2, V_{C1}^{*} increases linearly, and $V_{DC-ctrl}$ smoothly and gradually increases to regulate $V_{DC\,link}$. At stage III, since the inverter output current control loop is turned on, the output power processed by the inverter increases, and a reduction in the value of $V_{DC\,link}$ is noticed. At stage IV the inverter is fully connected with PCC, and the DC link voltage remains regulated until the end of the simulation. Due to the coupled-inductor leakage inductance, it can be noticed the presence of voltage spikes in the DC link, which however do not compromise the functionality of the closed-loop control system. Moreover, D_{st} remains practically constant, as expected, with a value that oscillates around 0.2130. The stabilization of D_{st} is an important characteristic in this application since the maximum modulation index M_{max} is directly related to D_{st}. If D_{st} remains constant, the available modulation range remains unchanged and thus multifunctional strategies based on this available range can be derived, as can be seen in the next sections.

Figure 7.3 shows the behavior of the MPPT controller and the extraction of maximum PV power. It can be seen that previously to stage (III), the $I_{mppt-ref-ABC}$ is defined as 8 A, which is the value of feed-forward value I_{fwd}, which is not sent to the resonant controller since the MPPT control loop is disabled. After 0.5 s, the MPPT controller is turned on, and it can be noticed that the input panel voltage V_{PV} gradually moves towards V_{PV}^{*}, since the current reference $I_{mppt-ref-ABC}$ gradually increases.

Therefore, the instantaneous PV power average value moves closer to PV maximum

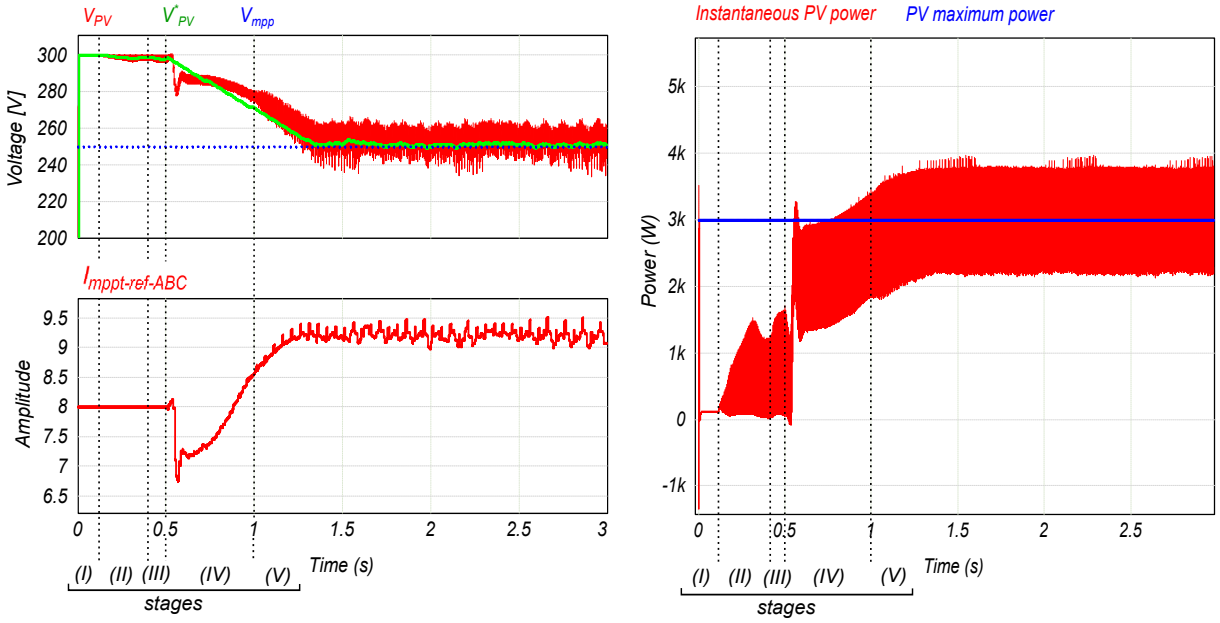


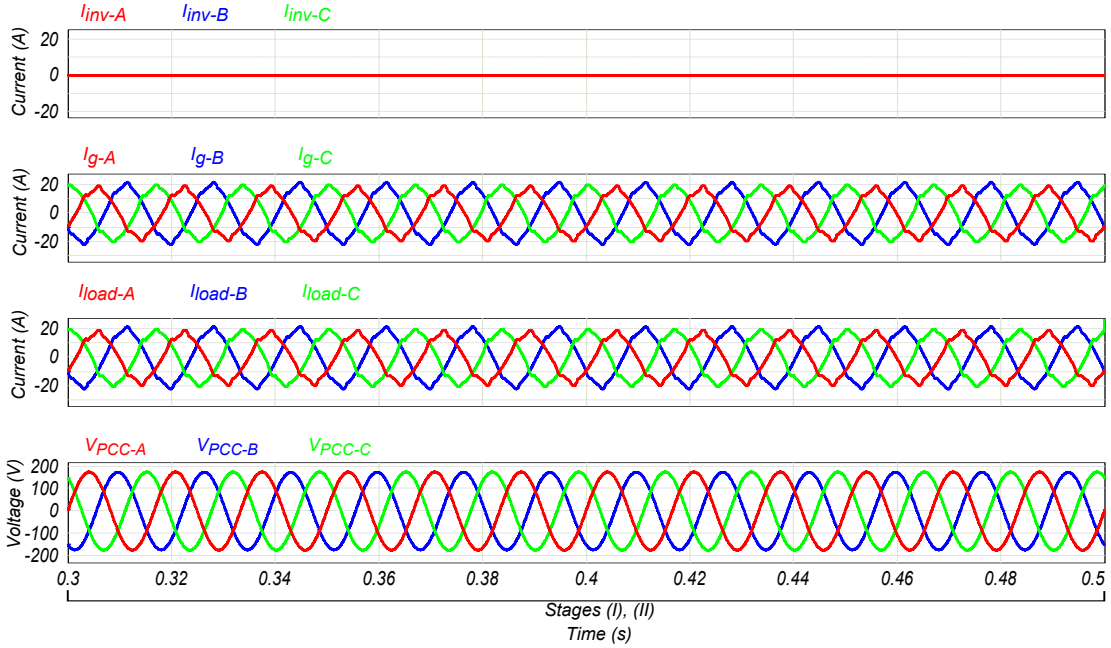
Figure 7.3 – Obtained V_{PV}, $I_{mppt-ref-ABC}$ and instantaneous PV power waveforms.

power. After 1.5 s, the MPPT algorithm reaches its equilibrium, with V^*_{PV} oscillating around PV maximum power voltage V_{mpp}=250 V. In Figure 7.4 it is shown the inverter output current for different operational stages. It can be seen in Figure 7.4a that during stages I and II, the inverter is not connected with PCC and grid current is non-sinusoidal, with a THD = 7.71 % [2]. Moreover, grid currents $I_{g-A,B,C}$ are not balanced and are not in phase with phase voltages.

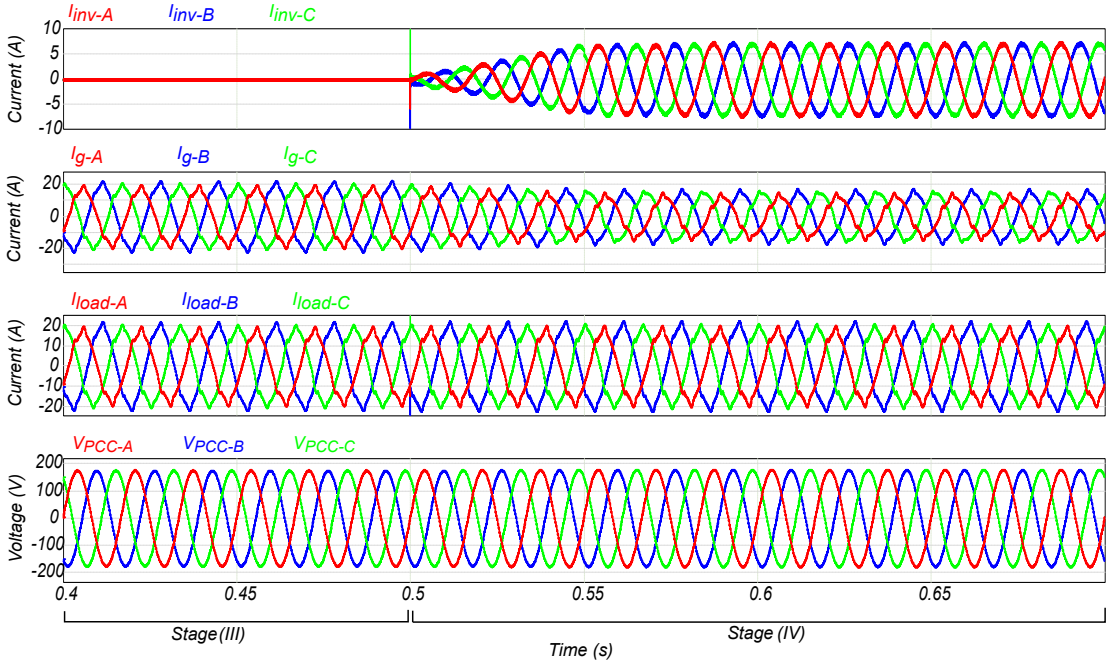
In Figure 7.4b it can be noticed that the inverter is connected with PCC at 0.5 s, gradually injecting current in phase with PCC voltages $V_{PCC-A,B,C}$. As the inverter current injection increases, the current demand from the grid side decreases, while the load currents remain practically the same. In Figure 7.5 shows the inverter current with compensation components delivered by the CPT. It is clear that, as the inverter synthesizes the current compensation components, the grid currents $I_{g-A,B,C}$ becomes balanced, almost sinusoidal - with a THD of 4.9% - and in phase with PCC voltages. Therefore, the QSY PV inverter is injecting active power, extracting maximum power from PV, and realizing current components compensation at the same time, which validates the concept of multifuncionality for this type of converter.

Lastly, Figure 7.6 shows the dynamic values of several power quality indexes for the grid and inverter sides, respectively. From Figure 7.6, the readings for the inverter-related indexes must be considered only after 0.5 s, which is when the inverter is connected to the PCC. In this period, the inverter only injects active power P_{inv}. As the MPPT algorithm runs, P_{inv} comes closer to 3 kW, which is the maximum power available at PV.

[2] In this chapter, the THD indexes are obtained directly within PSIM Simview, according to the following procedure: The THD is calculated as $THD = \frac{\sqrt{V^2_{rms} - V^2_1}}{V_1}$, where V_1 is the fundamental component and V_{RMS} is the overall rms value of the waveform. Inside the THD algorithm, there is a second-order band-pass filter to extract the fundamental component. The center frequency (fundamental frequency) of the band-pass filter is previously specified by the user (POWERSIM, 2020) - in this case this frequency was defined as 60 Hz.



(a)



(b)

Figure 7.4 – Inverter, grid and load currents at PCC at different stages: a) Stages I and II; b) Stages II and III.

Simultaneously, the active power delivered from the grid is reduced, while the other power quantities remain practically the same. After 1.0 s, the inverter apparent power A_{inv} remains practically constant, while Q_{inv}, $N_{a,r-inv}$ and D_{inv} increases since unbalanced and reactive grid current terms are being compensated by the inverter. This can also be observed by the increasing distortion, unbalance, and reactive factors λ_{D-inv}, λ_{N-inv}, and λ_{Q-inv}. On the other hand, the grid, after compensation, practically only delivers active power with a close to unity power factor, as can be seen by the factor λ_g. Table 7.2 shows the values of power indexes

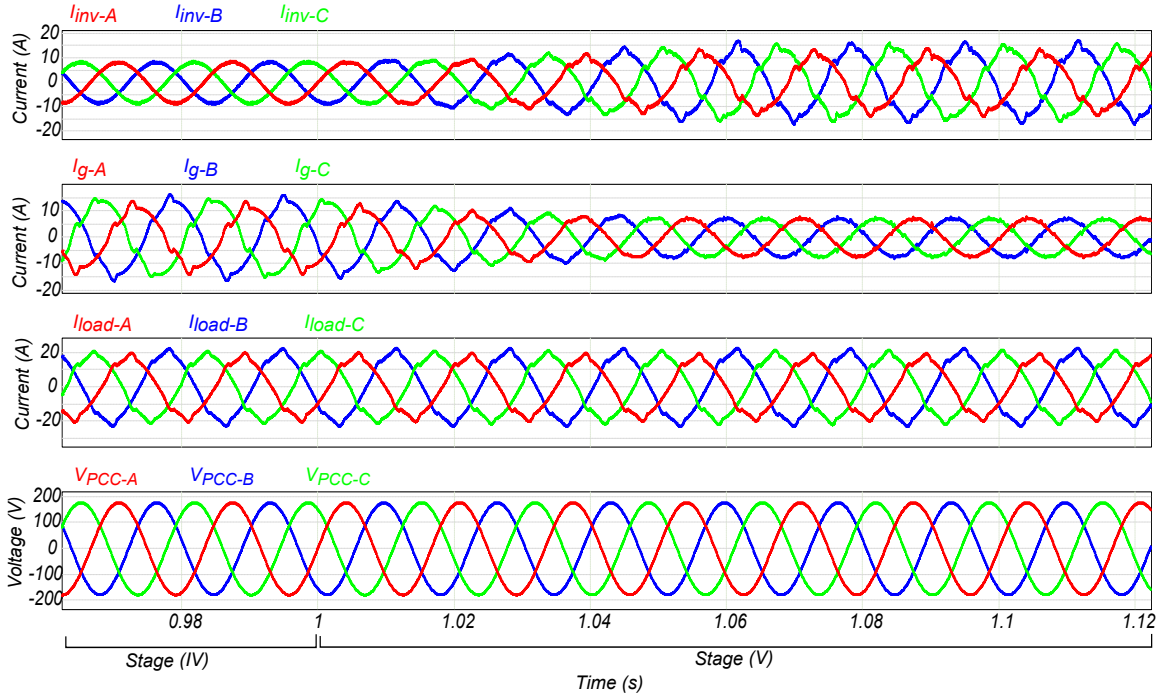


Figure 7.5 – Inverter, grid and load current at Stage V.

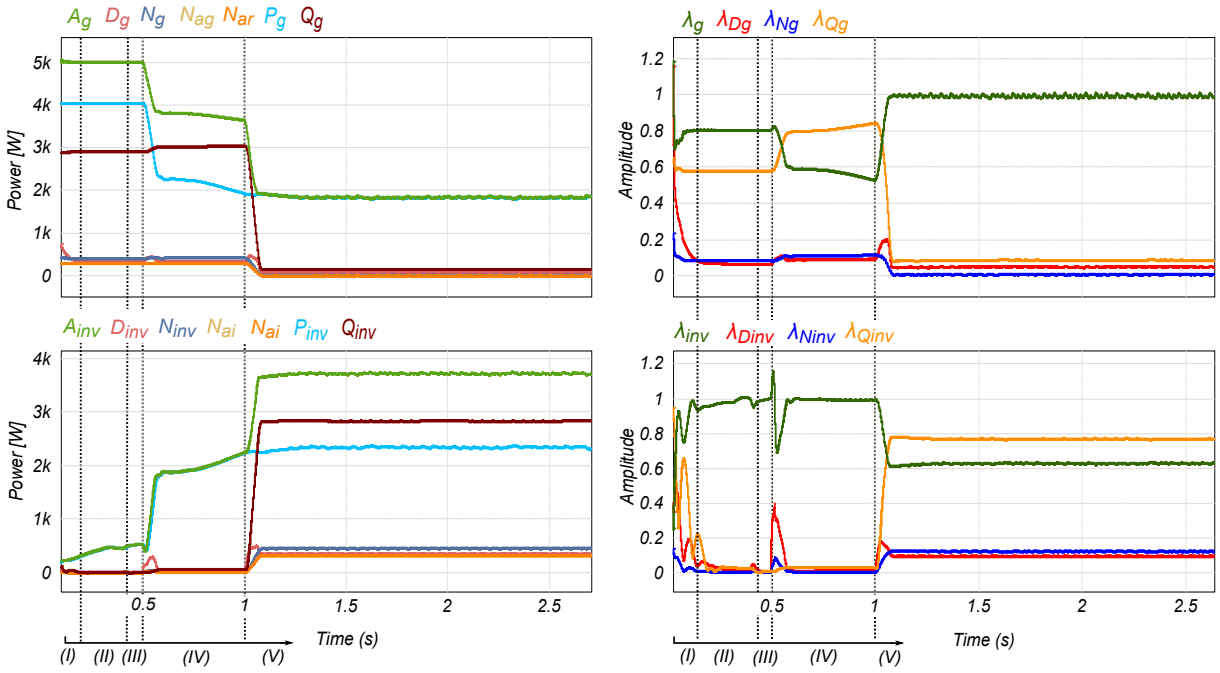


Figure 7.6 – Power quality indexes measurement.

for the grid side, both before and after compensation performed by the QSY PV inverter. Except for the power factor λ_g, all other power indexes are lowered, which confirms the compensation capability of the QSY inverter to improve power quality terms at the grid side.

Table 7.2 – Power quality indexes measured before and after compensation.

Index	Before compensation	After compensation	Difference
A_g [VA]	5008	1853	-63%
D_g [VA]	335	95	-72%
N_g [VA]	416	17	-96%
N_{ag} [VA]	295	12	-96%
N_{rg} [VA]	294	12	-96%
P_g [W]	4044	1844	-54%
Q_g [VA]	2905	159	-95%
THD_{Iag}	7.71%	4.91%	-36%
THD_{Ibg}	5.45%	5.17%	-5%
THD_{Icg}	6.58%	5.64%	-14%
THD_{VPCC-A}	0.27%	0.07%	-75%
THD_{VPCC-B}	0.22%	0.07%	-67%
THD_{VPCC-C}	0.25%	0.08%	-69%
λ	0.8075	0.9950	+23%
λ_D	0.0670	0.0510	-24%
λ_N	0.0833	0.0090	-89%
λ_Q	0.5834	0.0859	-85%

7.3 Ancillary services impact on the QSY inverter

In the last section, it was demonstrated the capability of the QSY inverter to execute ancillary services while it delivers active power extracted from the PV panels. However, when such ancillary services are executed, the general operation of the converter is affected. The objective of this section is to analyze the main impacts of the execution of the ancillary services on the QSY network components, inverter switches, and MPPT performance. In the next paragraphs, a comparison with two mission profiles is given, with the first one being the QSY inverter operating only with active power injection to the grid, and the second one considering the same ancillary services execution approach exposed in Section 7.2. In both cases, the QSY inverter extracts maximum PV power from MPPT.

7.3.1 Voltages and currents on the QSY network components

Figure 7.7 shows the peak voltages, including the rms and peak current variation on the QSY components, before and after the execution of the ancillary services.

It can be seen in Figures 7.7a and 7.7c that there is a significant increase in the voltage and current peak values, after the execution of ancillary services. Among the components of the QSY network, the capacitor C_2 was the one with the highest voltage spike increase (+32%), while the other components had less significant variations, all below 7%. On the other hand, the capacitor C_1 had the highest current spike increase (+19%), followed by diode current I_D (+12%) and coupled-inductor winding I_{N3} (+12%). Now, regarding the rms current, there is a less expressive variation in all the components, with a small reduction in all device currents. The

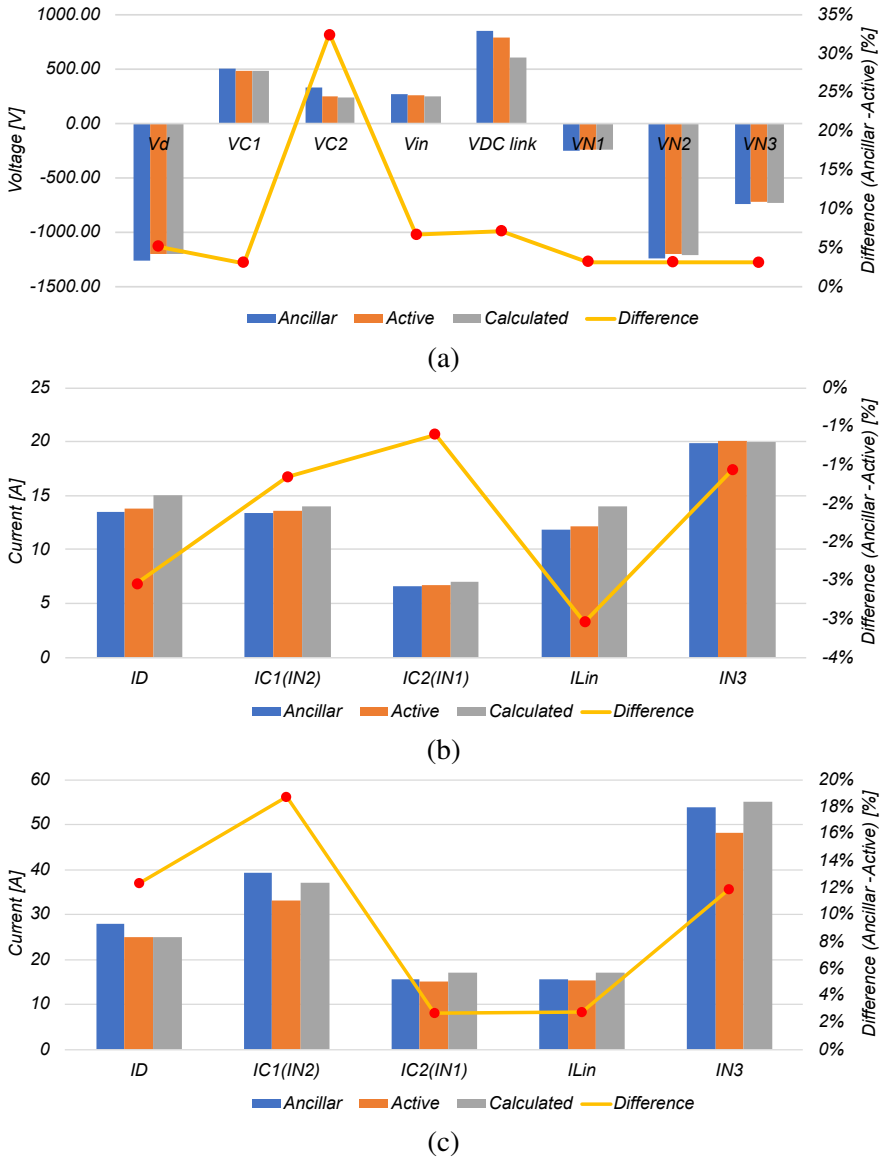


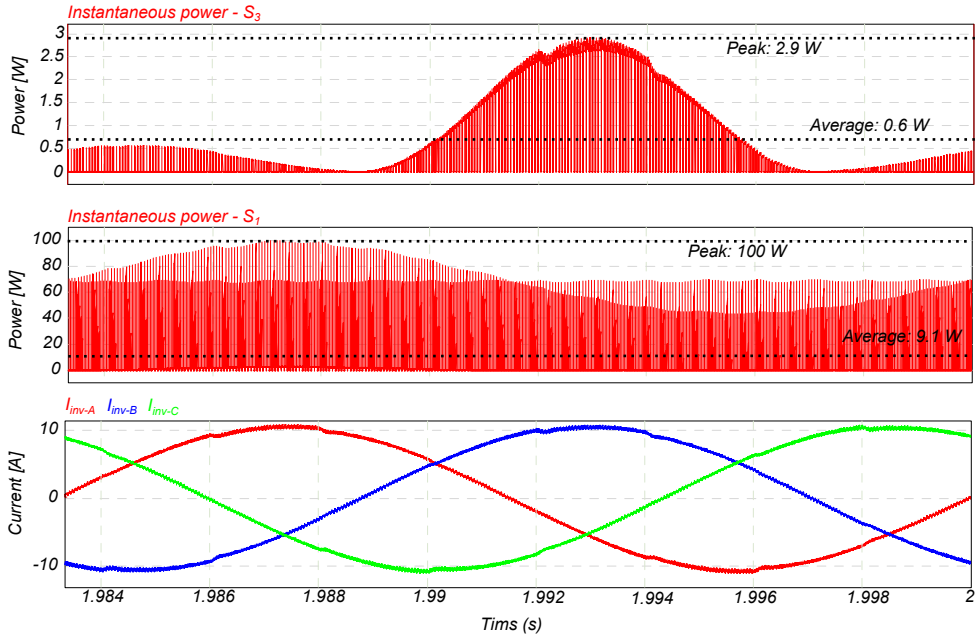
Figure 7.7 – Measurements of the QSY network voltages and currents, before and after compensation, including the calculated values: a) Peak voltages; b) RMS currents; c) Peak currents.

cause for this behavior is explained by the execution of the ancillary service on the MPPT, which will be explained in the following paragraphs.

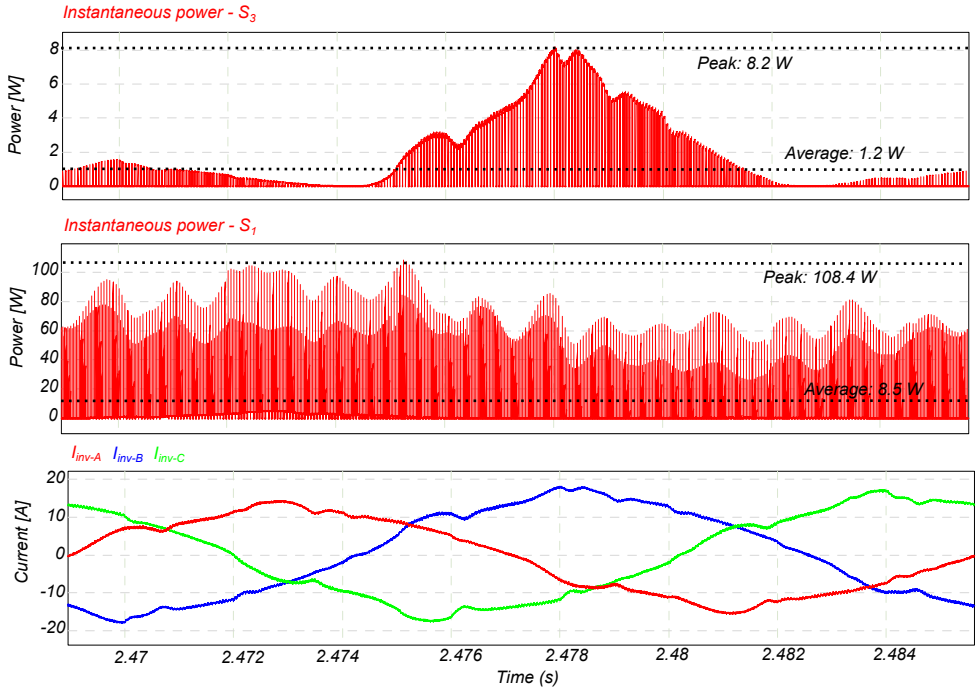
It can be observed, however, that many of the calculated values for peak voltages, including rms and peak current values remained relatively valid even after the execution of the ancillary services. In most cases, the calculated values are higher than the measured ones, which is not an issue since it is desired to have safety margins in the QSY components specifications. Those differences are more critical for D peak current and reverse voltage blocking, respectively, C_1 peak current and peak voltage value for C_2, since the calculated values deviate significantly from the measured ones. Therefore, the designer should take additional care of the specification of these components at the design stage, considering additional safety margins.

7.3.2 Switching power loss

Figure 7.8 shows the instantaneous power at two different switches located in the inverter: S_1, which performs shoot-through conduction, and S_3 which does not operate with shoot-through conduction. The analysis of these two switches is carried out to understand how the shoot-through conduction affects the power dissipation at the inverter. Moreover, another objective is to analyze the effect of ancillary services in this scenario.



(a)



(b)

Figure 7.8 – Instantaneous power at S_1 and S_3 switches over a one inverter output current cycle.

Figure 7.8a shows the instantaneous power profile in the case where the QSY inverter only injects active power at PCC. As can be seen, the shoot-through conduction increases the average power dissipation to almost 15x (0.6 W to 9.1 W) and peak power to 34x (2.9 W to 100 W), which can be observed by comparing the average and peak power values for S_1 and S_3 switches. In the same way, when ancillary services are executed, the increase in average and peak power at switches S_1 and S_3 is measured as 7.1x (1.2 W to 8.5 W) and 13.2x (8.2 W to 108.4 W), respectively. In this last case, it can be noticed that power dissipation at S_3 switch increased when compared with the case when only active power is delivered to the grid.

The results shown in Figure 7.8a indicate that the execution of ancillary services alone is prone to increase switching power loss at the inverter transistors that do not realize shoot-through conduction. This conclusion can also be verified in recent works in the literature (LIU et al., 2020), (CALLEGARI et al., 2019). Nonetheless, the execution of ancillary services does not change the considerable power loss increase in the switches that realize shoot-through conduction. In this sense, it is clear that the definition of strategies that can handle the modification of the inverter legs in which the shoot-through conduction occurs would be helpful to alleviate the inherent increase in switching power loss in the QSY inverter. Additionally, during the design stage, it is advisable to properly select the QSY inverter transistors, heat sinks, and cooling systems that can take into consideration the specific characteristics of switching power dissipation that exists in the QSY inverter.

7.3.3 MPPT performance

The MPPT is also affected by the execution of the ancillary services and in this section this situation is explored. In Figures 7.9 and 7.10 it is shown the PV panel voltage V_{PV}, input current I_{Lin} and the MPPT controller current reference I^*_{AC-ref} for the pure active and ancillary services execution scenarios.

It can be seen in Figure 7.9 that when the QSY inverter only injects active current to the PCC, the MPP tracking dynamic is smoother, and the oscillations of the instantaneous values of V_{PV} around V_{mpp} is between +5 V and -5 V, approximately, that is $\pm 2\%$ deviation from the maximum power voltage. The input current I_{Lin} is almost constant, with average value of 12 A. Regarding the MPPT controller, it can be seen that the inverter current reference amplitude value varies from 10.4 A to 10.9 A, which is a variation of 0.5 A.

Now, analyzing Figure 7.10, one can note that the V_{PV} variation around V_{mpp} is the range of +20 V and -20 V, approximately, that is a deviation of $\pm 8\%$, which is 4x higher than the pure active injection case. It can be noticed the presence of high-frequency current components at I_{Lin}, which is a reflection of the harmonic current injection made by the QSY inverter when executing ancillary services. Nonetheless, I_{Lin} average value does not change significantly from 12 A. The MPPT controller's current reference changes from 9.8 A to 11 A, which is a variation of 1.2 A, 1.4x more than the pure active case.

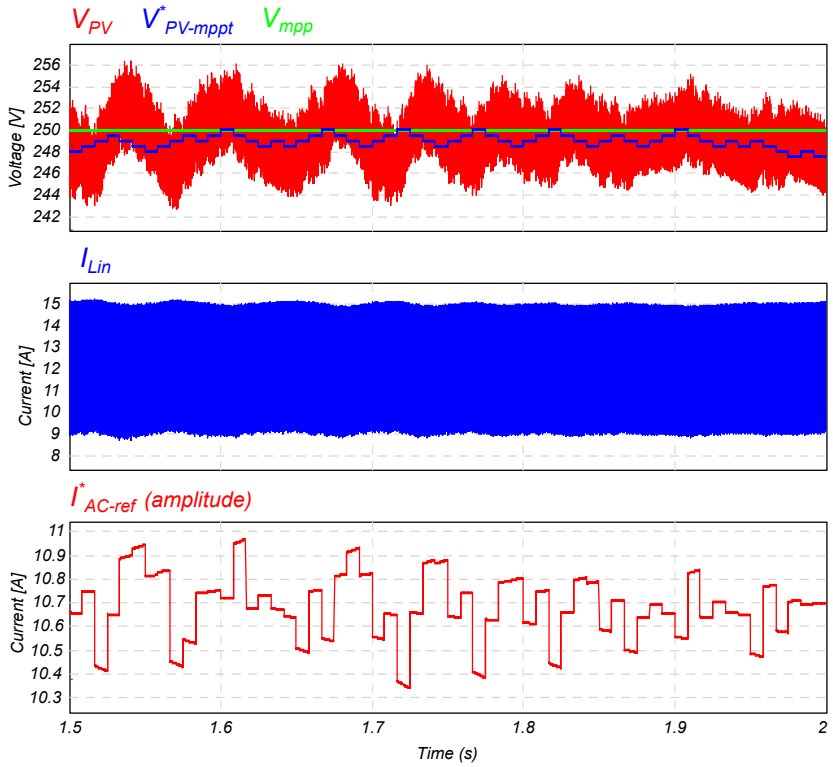


Figure 7.9 – MPPT controller and PV voltage and current waveforms for the pure active power injection case.

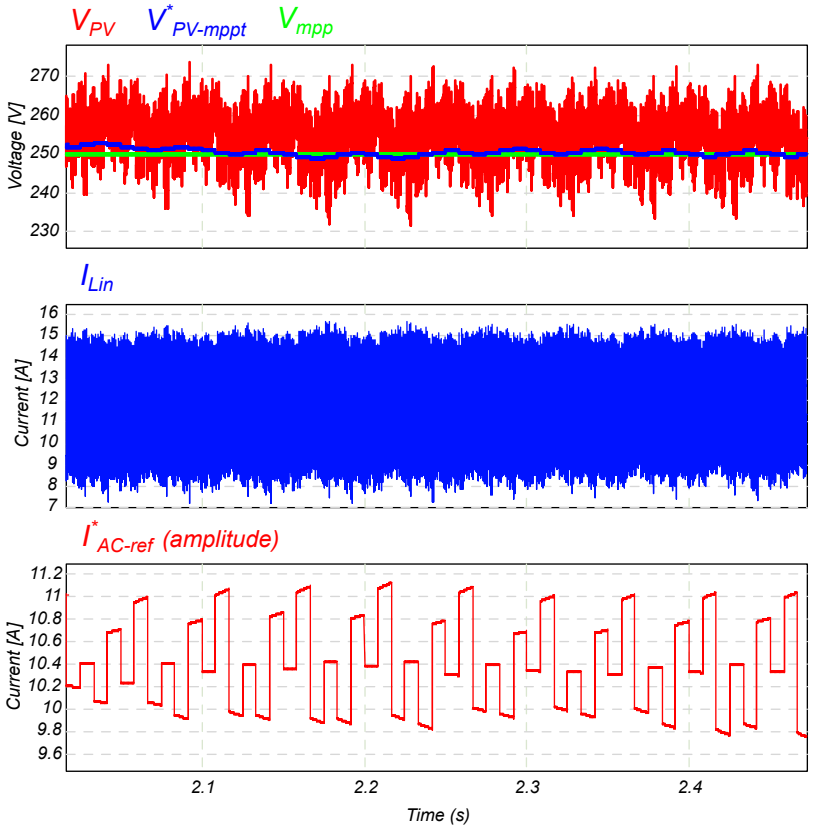


Figure 7.10 – MPPT controller and PV voltage and current waveforms when ancillary services are executed.

The results shown in Figures 7.9 and 7.10 suggest that the MPP tracking when ancillary services are executed presents a more oscillatory behavior, meaning that the power values extracted from the PV array present a pulsating dynamics around the maximum power. As a result, the average active power delivered from the QSY inverter is slightly lower when compared with pure active cases. This can be inferred from the efficiency calculations made in both cases. In the simulations carried out, when only active power is injected into the PCC, the QSY inverter calculated efficiency was defined as 94%, whereas in the case of ancillary services execution, the stipulated efficiency was calculated as 92 %, there is, 2% lower than the first case. In the literature, the study carried out by (JESUS et al., 2019) presents similar conclusions, studying the impact of harmonic compensation made by three-phase PV inverters on the MPPT performance.

7.4 Summary

This chapter presented a simulation case, considering the QSY inverter with all the control loops designed in the previous chapters operating simultaneously. The simulated case considers different types of linear and non-linear loads, for a typical commercial or small-factory environment. The connection of the QSY inverter to the grid is made considering a sequence of control events, which were described in detail.

The obtained simulation results demonstrated the effectiveness of the derived methodology to implement the QSY inverter as a multifunctional PV inverter, through the evaluation of the impedance network and inverter output waveforms. Additionally, the impacts of the ancillary execution on the QSY network components, inverter switches, and MPPT performance were also analyzed.

8 Experimental results

In this chapter, some of the obtained experimental results are shown. Initially, the prototype characteristics are described, including details about the built QSY network, the DSC, and the code upload strategy based on the PSIM SimCoder feature and information about the snubber circuits. Prior to the connection of the QSY inverter with the grid [1], many challenges need to be overcome. Among them, there is the issue of DC link overvoltages caused by the coupled-inductor leakage inductances. The experimental waveforms for this case are shown in Section 8.2, illustrating the importance of the LCD snubber to allow the operation of the converter at nominal grid voltage values.

With the LCD snubber properly designed, another challenge that needed to be solved was to validate the DC link voltage regulation strategy, exposed in Chapter 4. In Section 8.3 it is shown how this was accomplished, indicating how the DC link remains robust against external perturbations at the converter voltage input stage and load output stage. The experimental tests were conducted in Sections 8.2 and 8.3 are based on an off-grid scenario, with the objective of connecting the QSY converter with the grid only when the DC link overvoltages damping through the LCD snubber and DC link regulation strategy control objectives were satisfactorily met.

Additionally, experimental tests were done connecting the QSY inverter with the grid, including the execution of ancillary services using the CPT. The results of these tests are shown in Section 8.4, in which it is successfully confirmed the concept of using the QSY inverter with multifunctional features. At the end of this chapter, preliminary MPPT controller implementation results are shown, in a simplified case considering the QSY network applied in a DC-DC converter. It is the author objective to concretize the MPPT implementation in the QSY inverter in future works. It is worth mentioning that most of the oscilloscope waveforms were obtained using the Tektronix 'TekScope Ultimate' software, used to join the .csv files obtained with the oscilloscopes MDO34, MDO3014, and MDO3034 available in the laboratory [2]. When it was necessary, external trigger signals were used to synchronize multiple oscilloscopes, such that multiple waveforms could be acquired simultaneously, with negligible time delay.

8.1 Experimental prototype

Figure 8.1 shows the laboratory prototype implemented to validate the QSY inverter. Table 8.1 shows the parameters of the prototype, which are different from Table 3.3 due to

[1] The term 'grid' refers to the laboratory grid emulator power source used during the experimental tests.

[2] The experimental THD indices were obtained using the MDO34, MDO3014, and MDO3034 oscilloscopes, taking into account harmonics in the waveform including components up to the 40^{th} order.

the lower power scale capability and components limitations. The parameters shown in Table 8.1 were employed in the computer simulation using PSIM, with F28379D blocks for ADC and PWM peripherals configuration, and the SimCoder package for automatic code generation. The code generator tool from PSIM was used to create the controller C code, whereas Code Composer studio was used to upload the code to DSC F28379D. In the prototype shown in Figure 8.1, the coupled inductors were built on a toroidal core of sendust (μ_r = 60 H/m) with a winding turns ratio of 37:112:186, and 2x22 AWG and 3x20 AWG Litz wires. The capacitors C_1 and C_2 are implemented with the A511EJ68M450F and the 15 μ F, 500 V film capacitor model C4AQLLU5150A19K. The IRG4PF50WD IGBT and GC2X5MPS12 26 A and 1200 V SiC Schottky diode were used as S_{1-6} and D. Furthermore, to relieve voltage spikes at the DC link, the LCD snubber was implemented with L_s = 235 μH, C_s = 1.05 μF, and RHRG30120 diode, based on the work developed in (FOROUZESH et al., 2018). In the same way, an RC snubber was used in parallel with D with a resistance value of 270 Ω and a capacitance of 4 nF, with a design methodology inspired in (RIDLEY, 2005a). During the grid-connected tests, the inverter output passive filter is comprised of three inductors with 10 mH, being a first-order low-pass filter. Now, in off-grid tests, an LC low-pass passive filter is used, with an inductance of 10 mH and capacitance of 15 μF.

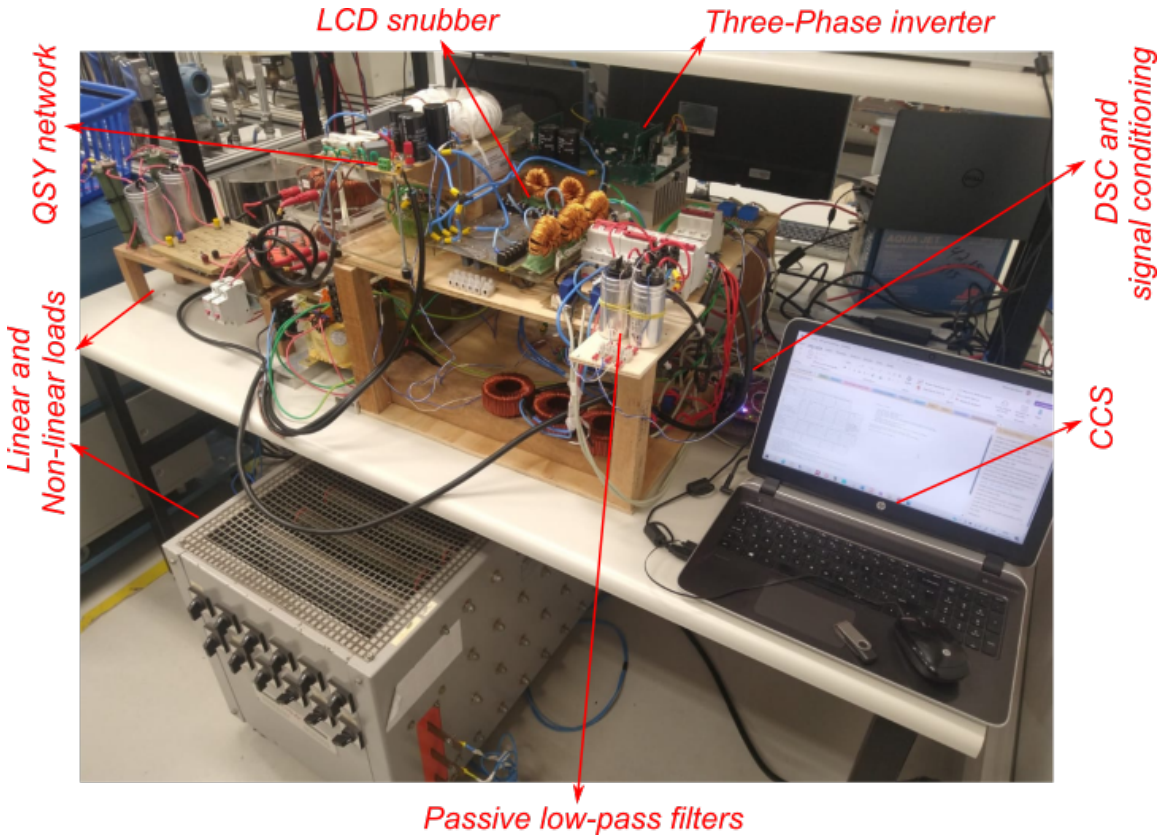


Figure 8.1 – QSY inverter developed prototype.

Table 8.1 – QSY converter circuit parameters - laboratory prototype.

Component	**Value**	**Component**	**Value**
L_{in}	4.24 mH	r_{Lin}	0.85 Ω
C_2	15 μF	r_{C2}	29.33 mΩ
C_1	2040 μF	r_{C1}	142.68 mΩ
r_D	25 mΩ	r_S	25 mΩ
L_m	0.222 mH	N_1:N_2:N_3	37:186:112
R_o	149.27 Ω	L_o	10 mH
V_{in}	250 V	f_{st}	18 kHz
δ	3.0135	D_{st}	$155.328689 \cdot 10^{-3}$

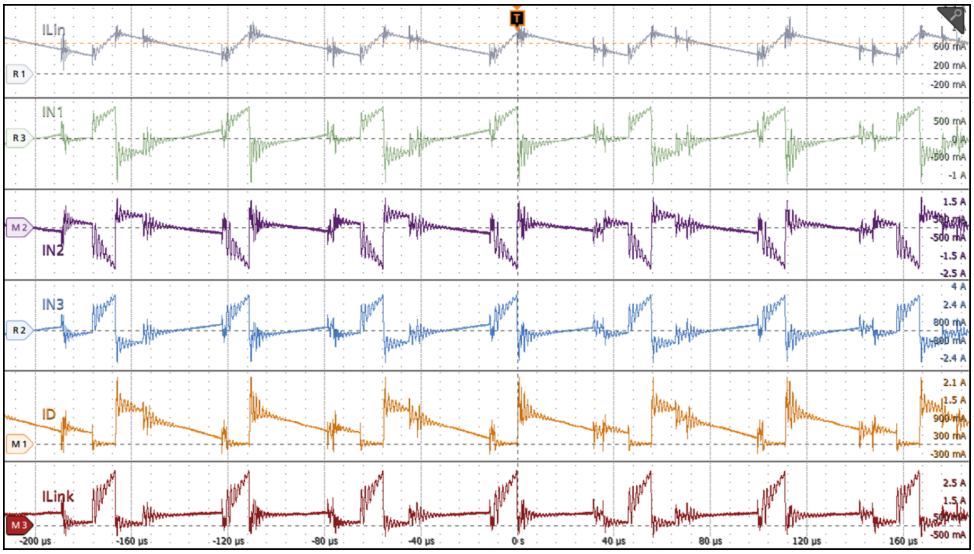
8.2 QSY network components experimental waveforms

One of the main challenges of the QSY inverter is the peak values of current and voltage that are resultant from the presence of leakage inductances. In this Section, it is shown how this issue was treated, and it is commented on the particular behavior of current and voltage waveforms obtained in the practical laboratory setup. Figures 8.2a and 8.2b show the currents and voltage waveforms at different components of the QSY network, without the presence of an LCD snubber. In order to demonstrate the effect of the leakage inductance on the DC link, without the presence of the LCD snubber, the TT 13500-5 core was used (see Appendix A), with V_{in}=50V, D_{st}=0.1666.

Moreover, the QSY inverter was tested in off-grid operation, with a fixed output load of R_o=72.2 Ω. Figure 8.2a shows the main currents and voltage waveforms at the QSY network. It can be clearly seen in Figure 8.2b that $V_{DC\,link}$ peak voltages can reach up to 235 V, which is 261% higher than the steady-state value. Obviously, as the input voltage increases, such values become higher and eventually could damage the inverter IGBTs - that is why V_{in}=50 V was used. In all waveforms, as discussed earlier, it can be noticed the presence of an undamped ringing current or voltage components, indicating the presence of stray inductances.

A second test was conducted, now using an LCD snubber with L_s=312 μH and C_s=1 μF. Figure 8.3 shows the main current and voltage waveforms for the QSY network, considering the presence of the LCD snubber.

In this second case, V_{in}=200 V with $V_{DC-link}$ regulated at 470 V. The inverter output phase voltage was set at 127 V_{rms} - this is now possible due to the presence of the LCD snubber. The peak voltage value at $V_{DC-link}$ is 634.5 V, which is around 40% greater than the steady value. As can be seen in Figure 8.3a the ringing components, which were damped due to the LCD snubber, did not affect substantially the inverter output voltages and currents. In fact, a 0.42% THD was measured at the inverter output line voltage, and a THD of 1.1% was measured at the inverter output current. The results shown in Figure 8.3 demonstrated the operation of the QSY inverter with higher DC link voltage values. In the next Section, it is shown the DC link voltage regulation results obtained in the laboratory.



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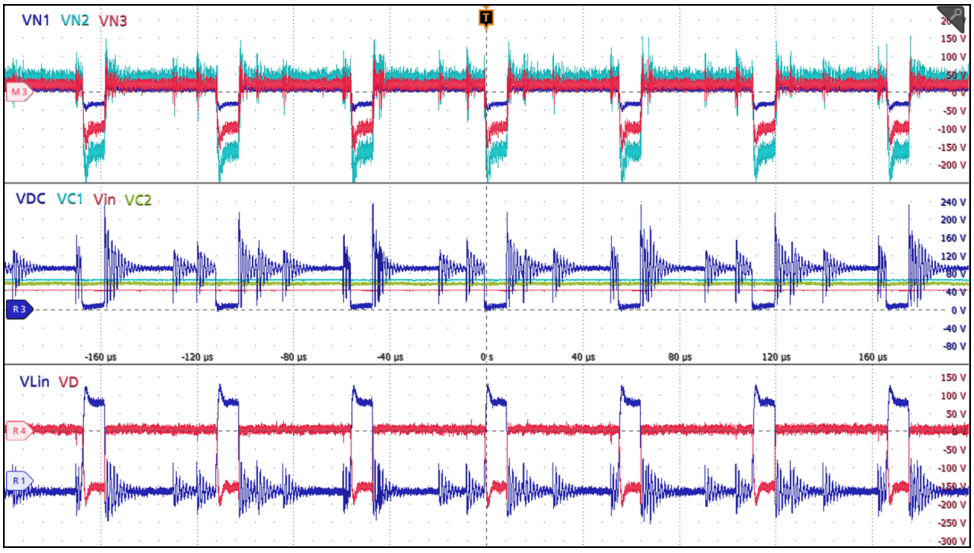


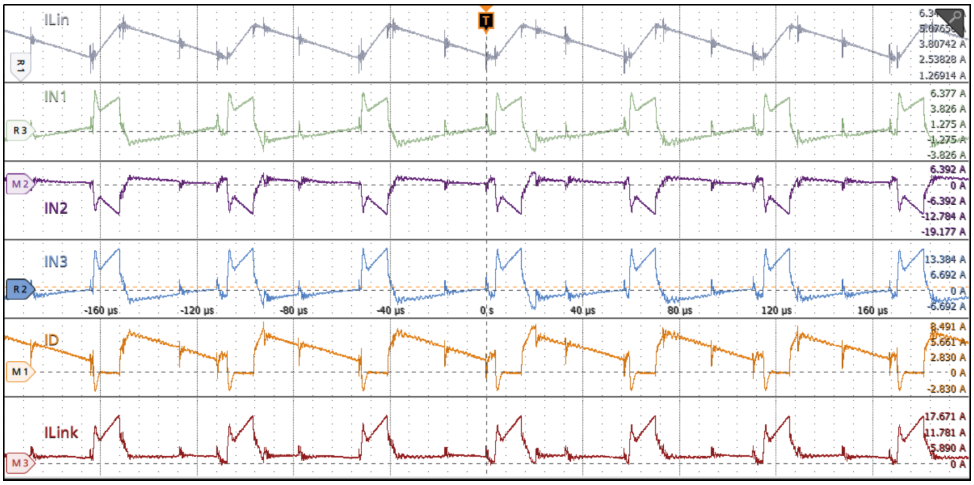
(b)

Figure 8.2 – QSY network experimental waveforms, without the LCD snubber, showing its components: a) Currents waveforms; b) Voltage waveforms

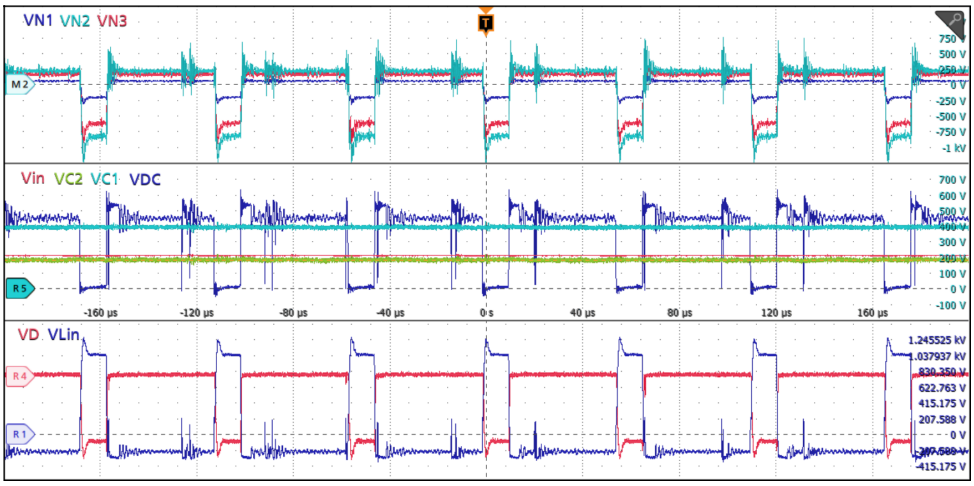
8.3 DC link voltage regulation

Figure 8.4 shows the experimental waveforms obtained with the developed prototype, in an off-grid application where the $V_{DC\,link}$ (indicated by V_{out}) is controlled (SANTOS et al., 2023) to be regulated at 470 V. In Figure 8.4a in the experimental test with constant input voltage V_{in} = 250 V and a load step resistance increase of 50%, it can be observed that before and after the load step, $V_{DC\,link}$ remains regulated at 470 V, as desired. As can be seen, the transient dynamics are overdamped with a settling time greater than 80 ms. This was expected due to the voltage control loop bandwidth set at 10 Hz and phase margin defined at 70° in this practical experimental test, which configures a slow dynamic response to the voltage regulation controller.

As shown in Figure 8.4e, as the inverter output line voltage V_{AB} is directly related to



(a)



(b)

Figure 8.3 – Experimental waveforms with LCD snubber (L_s=312 μH, C_s=1 μF), with TT 13500-5 core: a) QSY components currents; b) QSY components voltages.

$V_{DC\,link}$, V_{AB} also remains regulated, before and after the load transient. In Figure 8.4c, which shows the QSY converter waveforms for steady-state operation, after the load transient, it is verified that $V_{DC\,link}$ remains at the desired voltage level (470 V) and stable, with minimum steady-state error. Now, considering the input voltage variation, as shown in Figure 8.4b, the converter load remains constant, and there is an input voltage ramp variation from 200 V to 250 V (25% increase); the $V_{DC\,link}$ voltage remains regulated at 470 V, with a similar dynamic characteristic present in the input voltage variation test.

As depicted in Figure 8.4f, V_{AB} remains constant before and after the input voltage variation. In Figure 8.4d, which shows the converter waveforms for steady-state operation after the input voltage variation, it can be observed that $V_{DC\,link}$ remains regulated at 470 V. In general, both in the cases of load transient or input voltage ramp variation, it can be noticed that the controller action compensates the $V_{DC\,link}$ disturbances in an adequate manner, maintaining the voltage level at the desired values, which consequently validates the dynamic model used to design the controller.

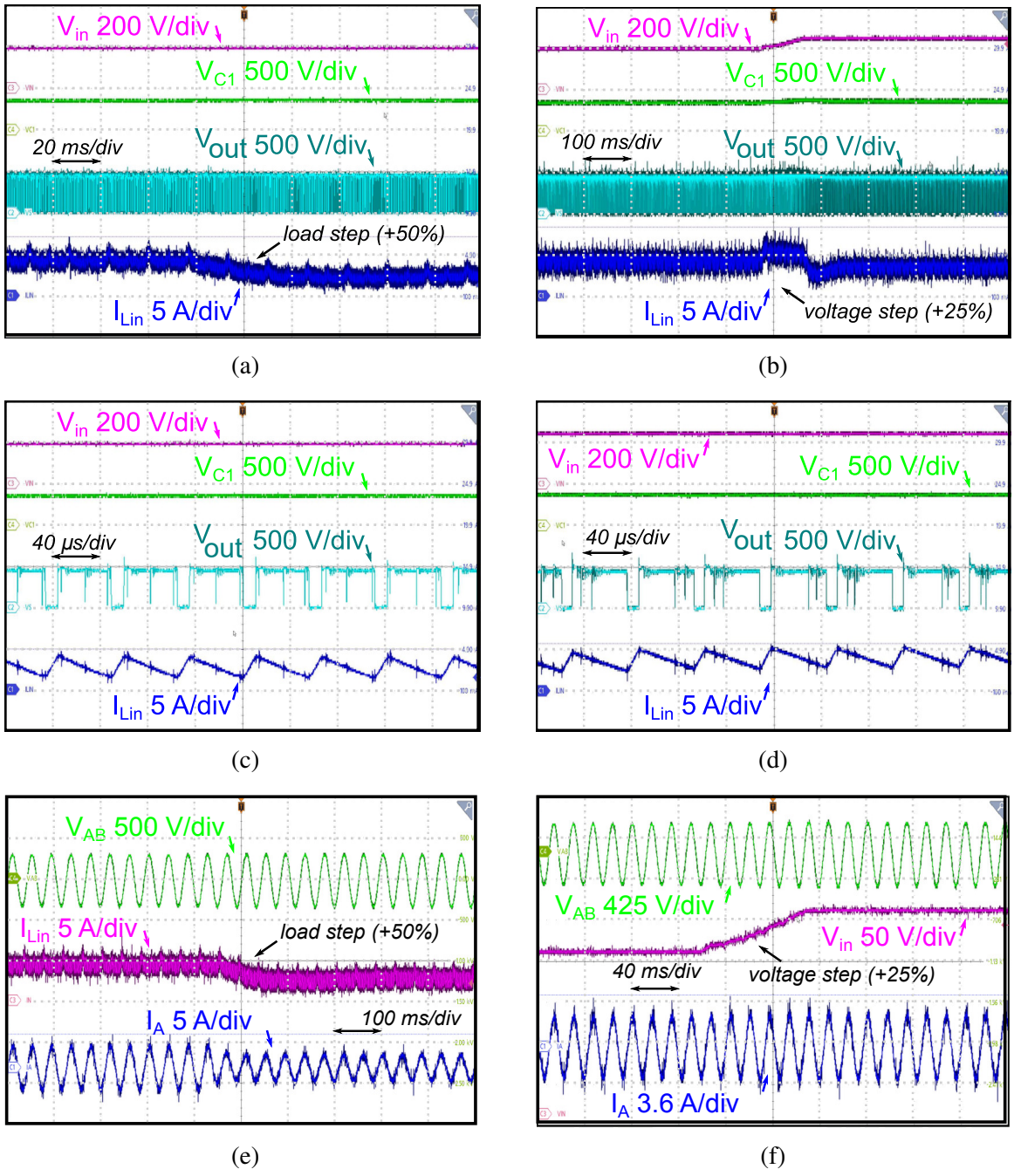
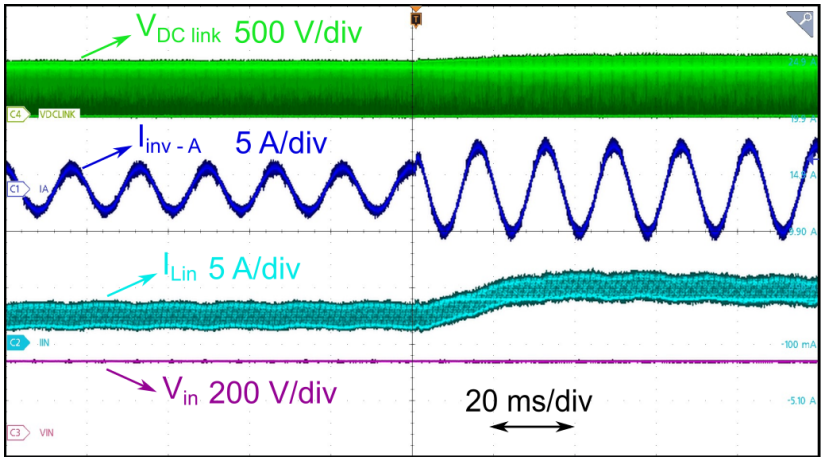


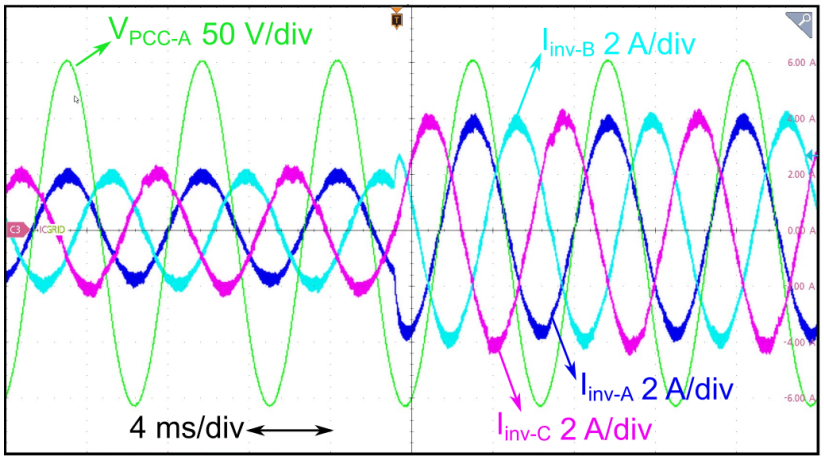
Figure 8.4 – QSY inverter experimental waveforms for load step change and input voltage ramp variation in off-grid application: 1) Load step change: (a), (c), (e); 2) Input ramp variation: (b), (d), (f).

8.4 Grid connection and ancillary services execution

Before realizing ancillary services, it is critical to validate the capability of the inverter to inject power into the grid. In this sense, Figure 8.5 shows experimental results for an on-grid application, where the QSY inverter only injects active current into the PCC. It can be seen in Figure 8.5a that the $V_{DC\,link}$ voltage remains regulated around 470 V, reaching a peak value of 560 V after the amplitude step reference change in I_{inv-A}, from 2 A to 4 A. It can be observed the fast reference tracking capability due to the PRes controller.



(a)



(b)

Figure 8.5 – QSY inverter experimental waveforms for on-grid application: a) QSY network characteristics waveforms ($V_{DC\,link}$, I_{Lin}, V_{in}) and I_{inv-A}; b) Inverter currents injected at the PCC (I_{inv-A}, I_{inv-B}, I_{inv-C}), and PCC phase-A voltage V_{PCC-A}.

Additionally the QSY inverter input current I_{Lin} remains in CCM mode along all the operations, with a mean value varying from 2.5 A to 4.5 A, approximately. The input voltage V_{in} remains at 250 V. Regarding the inverter currents injected into PCC, Figure 8.5b shows the three inverter output currents, I_{inv-A}, I_{inv-B} and I_{inv-C} waveforms, including the PCC phase A voltage V_{PCC-A}. It is clear by comparing the angular displacement of I_{inv-A} with V_{PCC-A} that the inverter currents are injected with a close-to-unity power factor PF, which is mandatory for a grid-connected inverter. This was confirmed by the measured PF value of 0.997, obtained after the current step reference change.

8.4.1 Multifunctional operation

With the active current injection capability confirmed, additional tests exploiting the inverter capability of executing ancillary services were conducted. Figure 8.6 shows the obtained results with the QSY inverter executing ancillary services, while simultaneously injecting active current to the PCC.

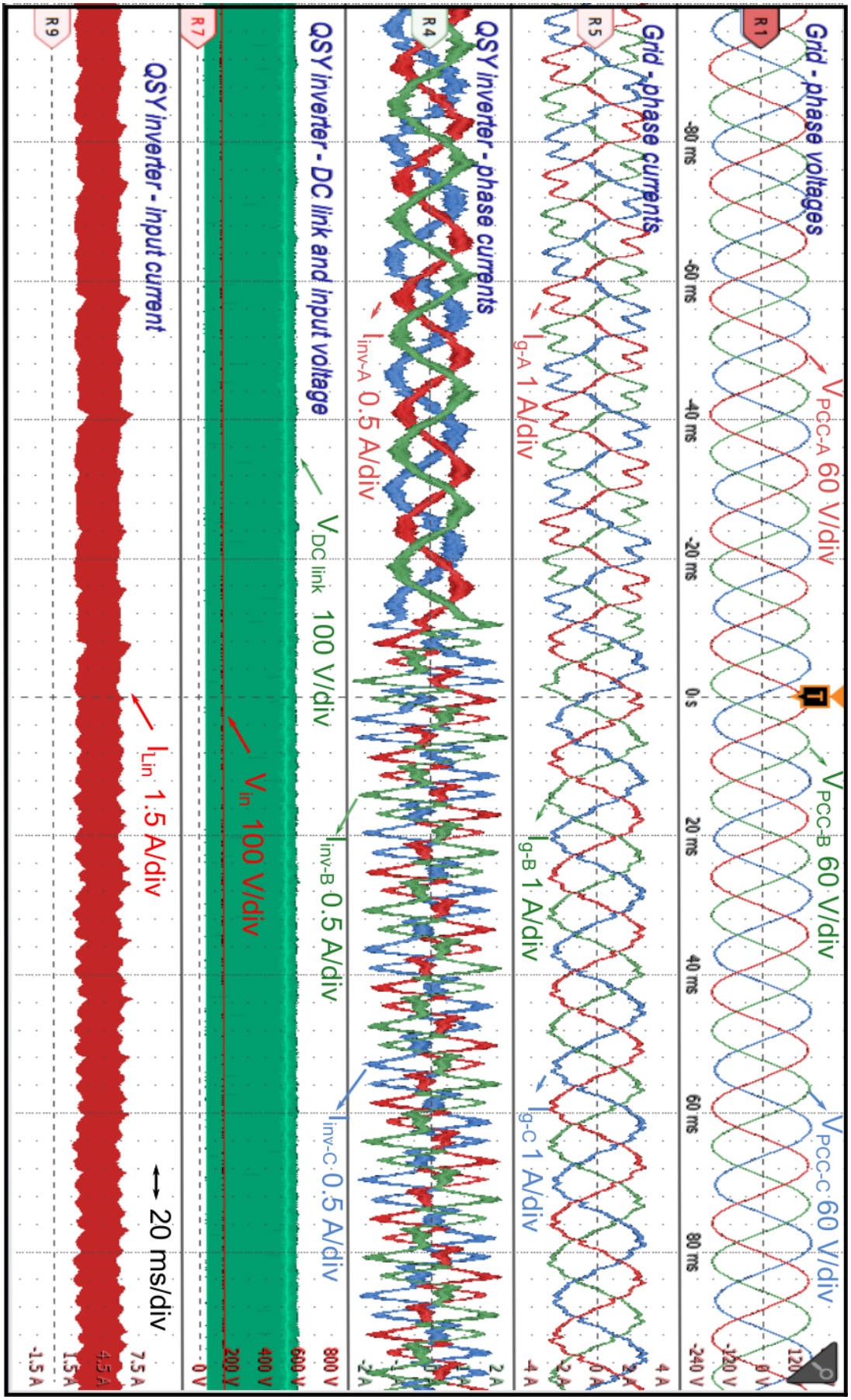


Figure 8.6 – QSY inverter executing ancillary services, with compensation of non-active current terms with simultaneous active current injection.

In this test, the QSY inverter was controlled to inject all the non-active current terms (reactive and void current terms), besides the active current components. The converter processed power was lower in this case. The reasons for this are: a) The author's objective was to show the voltage gain capability and the flexibility of the QSY inverter, with the possibility of executing ancillary services even when lower input voltages are present (V_{in}= 145 V); b) Due to hardware limitations on the prototype, particularly the current capability of the coupled inductors, the processed power at higher voltage gains needed to be reduced, to preserve the coupled-inductors. Connected at the PCC, there are a three-phase resistive load of 147 Ω and a three-phase rectifier, with an input filter of 5 mH, DC output capacitance of 4700 μF and a resistance of 83 Ω. To simulate the grid, it was used the Regatron TopCon TC.LAE 4-Quadrant Grid Simulator power source. The phase voltages V_{PCC-A}, V_{PCC-B}, and V_{PCC-C} were defined with a rms value of 127 V and frequency of 60 Hz. The inverter local load, used during the converter start-up period, was defined as R_{pl} = 72 Ω. It should be noted that during the start-up procedure, the QSY inverter remains disconnected from the grid.

The QSY converter input voltage was obtained with the DC voltage source Chroma 62050H-600 s. During the initialization of the DC link voltage closed-loop control, the input voltage magnitude V_{in} was set to 200 V, and $V_{DC\,link}$ voltage reference was gradually increased until the value of 480 V. Afterward, the inverter output current controller was initialized, with a peak current reference of 1 A. After verifying the correct operation of the DC link and inverter current controllers, the QSY inverter was connected with PCC, through the manual activation of a circuit breaker.

Along the experimental test, the Code Composer Studio (CCS) "Graph" tool was used to compare the instantaneous values of the sinusoidal modulation signals M_a, M_b and M_c with the maximum modulation M_{max}. This was done such the active current reference for the inverter could be adjusted to respect the maximum modulation limit of the converter. To explore the voltage gain capability of the QSY inverter, V_{in} was reduced from 200 V to 145 V, and $V_{DC\,link}$ voltage reference was gradually increased to 545 V. In this sense, the voltage gain B increased from 2.4 to 3.76. It was in this final setup that the results shown in Figure 8.6 were obtained.

It can be seen in Figure 8.6 that after 0 s, the grid phase currents I_{g-A}, I_{g-B} and I_{g-C} present a shape that is more similar to a sinusoidal waveform, in phase with grid phase voltages V_{PCC-A}, V_{PCC-B} and V_{PCC-C}, respectively. This happens because the reactive and void current terms are being compensated by the QSY inverter, as can be seen by the change in the current references sent to the QSY inverter when observing the waveforms related to I_{inv-A}, I_{inv-B} and I_{inv-C}.

Table 8.2 presents some power quality indexes measured with the oscilloscope waveforms. The phase voltage RMS values remained almost constant, before and after the compensation. However, a decrease of the grid side rms currents was noticed, with a reduction of 27% in phase A (2.6 A to 1.9 A), 27% in phase B (2.6 A to 1.9 A), and 31% in phase C (2.6 A to 1.8 A). Hence,

a reduction in line losses was obtained after the compensation made by the QSY inverter.

The active power delivered by the QSY inverter remained almost constant, both before and after the compensation, hence a negligible change in the active power delivered by the grid was detected. This happened because the QSY inverter's active current reference was not modified. However, because of harmonics and reactive current terms compensation by the QSY inverter, a reduction in the reactive power and apparent power was measured in all grid phases. For the reactive power case, a reduction of 43% (65 VAr to 37 VAr), 55% (62 VAr to 28 VAr), and 43% (67 VAr to 38 VAr) was calculated for phases A, B and C respectively. For the apparent power case, the reduction was 2% (242 VA to 237 VA), 1.6% (244 VA to 240 VA), and 2.5% (242 VA to 236 VA) for phases A, B, and C, respectively. Therefore, the QSY inverter helped to reduce grid non-active power terms, as expected, but in an adverse scenario, that is, with lower input voltage, which represents a low solar irradiation case. Hence, the capability of the ancillary service execution when higher input voltages are presented would be higher than the ones demonstrated in this critical scenario, since lower values of D_{st} would be required, and hence, higher values for M would be possible.

Yet, with the aid of the QSY inverter, the THD$_i$ of grid sides currents were lowered from 21.2% to 6% for phase A, 20.92% to 6.27% in phase B and 21.45% to 5.74% in phase C. Moreover, the final power factor of grid side currents moved closer to unity, changing from 0.96 to 0.99, 0.97 to 0.99, and 0.91 to 0.99 for phases A, B, and C respectively.

Regarding the QSY inverter DC side, the DC link voltage $V_{DC\,link}$ remained regulated around 545 V, with peak voltages reaching the value of 614 V, due to voltage spikes caused by stray inductances. The input voltage V_{in} remained constant, with an average value of 144.3 V. The input current I_{Lin} remained with a practically constant average value of 4.023 A.

Table 8.2 – Power quality indexes for the grid side, before and after QSY inverter compensation.

	Before compensation			*After compensation*		
Term	**Phase A**	**Phase B**	**Phase C**	**Phase A**	**Phase B**	**Phase C**
Frequency (Hz)		60			60	
RMS Voltage (V)	125.4	126.9	126.2	125.5	126.9	126.2
RMS Current (A)	2.6	2.6	2.6	1.9	1.9	1.8
Active Power (W)	233	236	232	234	239	233
Reactive Power (VAr)	65	62	67	37	28	38
Apparent Power (VA)	242	244	242	237	240	236
Power factor (PF)	0.96	0.97	0.96	0.99	0.99	0.99
THD$_i$ (%)	21.20	20.92	21.45	6.00	6.27	5.74

8.5 MPPT implantation - DC-DC case

To validate the MPPT P&O control strategy, it was considered a simplified case, where the QSY network was used in a DC-DC converter. In this case, the MPPT controller tracks the maximum power point through the control of the input current I_{Lin}, and a resistive load of 23 Ω is connected at the DC-DC converter output. The PV panel was emulated with the Keysight N8900APV Series power source, with a maximum power of 100 W and maximum voltage and current of V_m = 30.7 V, I_m = 3.27 A, respectively, open-circuit voltage V_{oc} = 37.3 V and short-circuit current of I_{sc} = 3.56 A. The C_{pv} capacitance value was defined as 1 μF and an ADC sampling frequency of 120 Hz was used to acquire I_{PV} and V_{PV}, respectively. Since the input current is controlled to realize the MPPT, a fixed step of 0.05 A was used to update the I^*_{Lin} current reference. Moreover, to obtain smooth MPP tracking, a digital first-order low-pass filter of 100 Hz was used.

The MPPT controller was designed using the frequency response method, based on a system block diagram similar to the one shown in Figure 6.3, but now using the $\frac{I_{Lin}}{D_{st}}$ transfer function, using the small-signal model derived in Chapter 4. Furthermore, it was adopted a 12 Hz cut-off frequency and a phase margin of 80 ° as dynamic requirements to design the MPPT controller. Figure 8.7 shows the performance of the MPPT controller under different irradiation levels, in which the maximum power levels vary to 60 W and 45 W. It can be seen that the implemented MPPT controller was successfully able to track the different maximum power points, with a small oscillation around the maximum power point in steady-state, for the different cases under analysis.

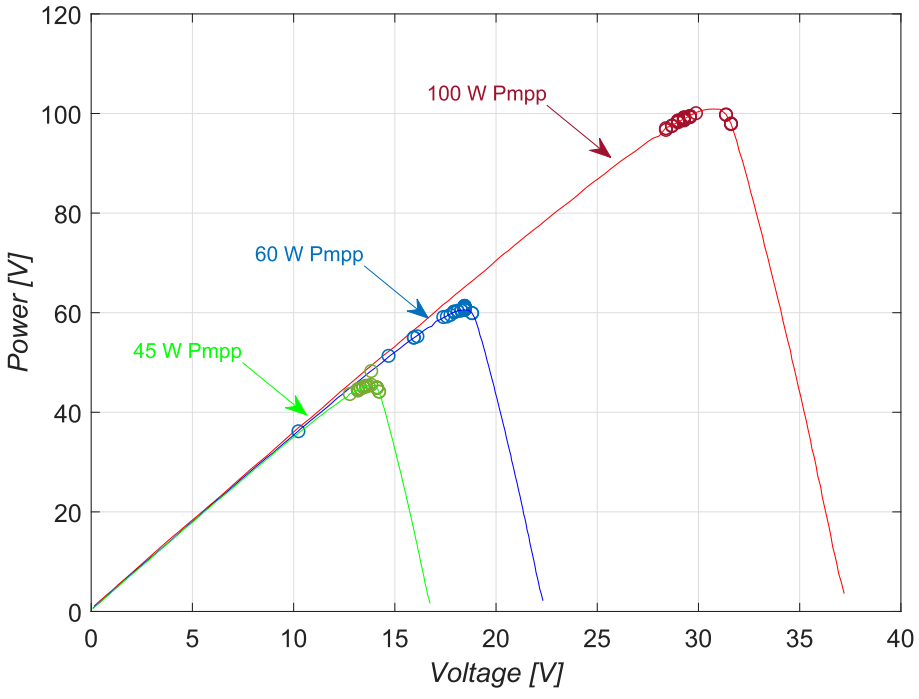


Figure 8.7 – Experimental MPPT results for the QSY DC-DC converter case – The marks represent the measured power values.

Figure 8.8 shows the obtained practical results, now through the Keysight SAS control user interface. As can be seen, the instantaneous PV power and maximum power point ratio reach 99.91 %, extracting 100.44 W from the power source, with V_{PV} =30.5 V and I_{PV} = 3.29 A, which also demonstrates the effectiveness of the MPPT controller implemented with QSY network DC-DC converter.

Figure 8.8 – Experimental MPPT results for the QSY DC-DC converter case - Keysight SAS control user interface.

The results shown in Figures 8.7 and 8.8 confirmed the MPPT control methodology and is the objective of future works to implement the MPPT control scheme in the QSY inverter, considering the simultaneous execution of ancillary services, using the CPT, as done in the previous chapter.

8.6 Summary

This chapter presented the experimental results obtained with a QSY inverter prototype in the laboratory. It was shown how the challenges that needed to be overcome were treated before allowing the connection of the inverter with the grid. At first, it was demonstrated how the voltage and current spikes caused by stray inductances were solved with the insertion of the LCD snubber. Then, the control methodology and the DC link voltage regulation controller effectiveness were confirmed experimentally, considering input voltage and output load disturbances.

After the solution of the DC link voltage control and the validation of the LCD snubber design, it was shown the performance of the QSY inverter when connected to the grid, with a close to unity power factor. The multifunctional capability of the QSY inverter was demonstrated with experimental results, showing the improvement of many power quality indexes related to

the grid side after the execution of the ancillary services with the inverter. All the experimental results confirmed the validity of the methodologies proposed along the previous chapters.

Finally, the MPPT controller was implemented, using the QSY network in a DC-DC converter. Satisfactory results were obtained using the P&O MPPT method, and future works will be conducted to implement this MPPT controller in the QSY inverter.

9 Conclusions

After all the work conducted during this research, this Chapter presents the author's conclusions about the QSY inverter. Beginning with the concept of using impedance-source networks in DC-AC applications, it can be concluded that INIs present many interesting characteristics and advantages, that fostered the research in this field in the last years. Due to the single-stage architecture, such inverters need less power transistors and other components to allow the converter operation as a buck-boost type, when compared to multiple-stages PV inverter topologies. Moreover, impedance-source networks are practically comprised of passive elements, which can be easily replaced and facilitates maintenance, besides presenting a lower cost, when compared to the alternative of having a secondary voltage step-up dedicated power converter. Nonetheless, due to the extended and flexible range of applications in which impedance-source networks can be used (AC-AC, AC-DC, DC-DC, DC-AC), the same impedance-source part could be manufactured to attend different types of converters, which would lead to a lower production cost due to flexible applications fields.

Another aspect that can be pointed-out is that the integration of the impedance-source network in an existing voltage-source inverter (VSI) does not present significant challenges. As demonstrated in Chapter 5, the inclusion of simple additional digital circuitry based on OR logic is sufficient to allow the correct control of the converter, properly integrating the shoot-through pulses. Additionally, a modification on the transistor drivers' firmware/hardware is also needed, particularly to disable voltage and current protections that were set to preserve the inverter from shoot-through conduction. Among these protections, there is the dead-time feature, which is not necessary for INI. Moreover, due to the shoot-through conduction, it is also necessary to remove an eventually present DC link capacitor and replace this capacitor with an impedance-source network. These simple changes are sufficient to transform a conventional VSI into an INI. The experimental results shown in Chapter 8 were obtained with a conventional VSI that was modified following the steps previously described. These observations show that impedance-source networks present a high potential to be employed in existing commercial inverters, with minimal modification or manufacturing additional barriers.

Particularly, in this thesis, the QSY network was studied since it presents additional advantages when compared with other impedance-source networks. Among these advantages, there is the continuous input current feature, the increased design flexibility, and higher voltage gains. The QSY network needs lower D_{st} values when higher values of δ are employed, which increases the M_{max} range. However, as shown in Chapter 3, the correct selection of δ is not straightforward, but the developed mathematical model of the QSY network is helpful in this task. Regarding the capacitor ratings, it was also shown that the C_1 capacitor voltage is lower when compared to the voltage that would be present in a conventional double-stage inverter DC

link capacitor. In the conventional scheme, considering the power ratings adopted in this work, the voltage across this DC link capacitor would be 600 V, whereas, in the QSY inverter, this voltage is 483 V, which is 20% lower. In overall, all these advantages of INI, particularly of the QSY network, exemplify the commercial compelling features of the QSY inverter and motivated the studies carried out in this thesis.

9.1 Thesis contributions

At this moment, the discussion can be forwarded to the contributions of this Ph.D. thesis. In this work, it was demonstrated how to design the QSY inverter to be used as a multifunctional three-phase/three-wire PV inverter. The scope of the work was to propose an alternative solution to the typical PV inverter configuration often found in the literature and market, which is usually based on some sort of multi-stage architecture. Along the chapters, many simplifying assumptions were made, to propose solutions to many of the challenges in the way of accomplishing this goal. In the present literature, there is no equivalent work that employs the QSY network topology in a PV inverter with multifunctional capabilities, considering all the associated control and design methodologies to attend to this objective. According to the content that was exposed in this thesis chapter, one can conclude that this is not a trivial task, and thus, the main contribution of this thesis was to demonstrate, with details and clear methodologies, how to achieve this goal. Specifically, this work's contributions can be listed as follows:

1. **QSY network design methodology –** A comprehensive design methodology for the QSY network was presented. With this methodology, it is possible to design all the components that comprise the QSY network, including the possibility of estimating its main current and voltage rms, average, and peak values through a set of mathematical expressions.

2. **Comprehensive QSY network mathematical model –** Through the derived small-signal model, it is possible to evaluate the voltage stresses on the different converter components, which helps to choose the most interesting values for δ and evaluate the dynamic impact on the converter control. Besides not being carried out in this document, the analysis of the component's current stresses and converter efficiency can also be made with the developed mathematical model and could be used in optimum design-oriented methodologies.

3. **RC and LCD snubber design considerations –** It was presented possible solutions to overvoltage issues caused due to the presence of stray and leakage inductances. Equivalent circuits showing these no ideal elements were presented and a review of DC link overvoltage solutions for Y-source based networks was presented. Besides not being shown in detail in this document, the author developed a design strategy for the design of the LCD snubber, which was essential to allow the execution of experimental tests, at nominal voltage levels.

4. **DC link voltage control methodology –** A DC link voltage regulation control system was proposed for the QSY inverter. Moreover, a detailed description of the equivalent block diagram and transfer functions derivations, considering hardware details and digital control aspects was presented. A small-signal model for the QSY inverter, based on the state-space averaging technique was described, and an equivalent switching circuit configuration was introduced to validate the model. Additionally, indications of control requirements selection and a step-by-step explanation of how to obtain the $G_{c-link}(s)$ voltage controller were given, including the procedure to obtain its digital formulation, such that it can be implemented in a DSC.

5. **Modified SBC-SPWM technique implementation –** To allow the integration of the shoot-through pulses, it was shown how to implement the modified SBC-SPWM technique.

6. **MPPT control methodology –** A MPPT control system was proposed for the QSY inverter. A detailed description of the equivalent block diagram and transfer functions derivations was presented. A definition of dynamic requirements criteria was proposed.

7. **QSY inverter start-up methodology and multifunctional operation –** It was shown how to properly initialize the different closed-loop control systems, such that the multifunctional operation and MPPT run simultaneously and harmonically. Furthermore, it was demonstrated the capability of the QSY inverter to execute ancillary services.

8. **Analysis of the ancillary services impact –** It was analyzed how the execution of the ancillary services affects the QSY network components, in terms of voltage and current stresses and MPPT performance. Regarding the inverter transistors, it was demonstrated how the execution of the ancillary services and shoot-through conduction affects the switching power losses, and an indication of a solution to this issue was given.

9. **Experimental results –** It was demonstrated how to implement the QSY inverter in a laboratory prototype, and considerations regarding the practical operation of the converter were given.

9.2 Drawbacks and possible solutions

As any power converter, the QSY inverter also presents some operational drawbacks and constraints. In this section, a brief discussion of these disadvantages is presented, and possible solutions to tackle these issues are proposed. The following list indicates some of the found problems:

1. **Overvoltage issues –** As can be seen in the practical results shown in Chapter 8, one of the QSY network's most affected components, in terms of voltage stress, is the diode D, input inductor L_{in} and coupled-inductor windings N_2, N_3. In the simulations, as seen in

Chapter 7, the peak voltage value at D reached -1262 V, which is 2.1x greater than the $V_{DC\,link}$ voltage (600 V). At L_{in}, the measured peak voltage value was 1450 V (2.4x greater than $V_{DC\,link}$) and at V_{N2}, V_{N3} the values of peak voltages were -1237 V and -744 V, which are 2x and 1.2x higher than $V_{DC\,link}$, respectively. These voltage values are relatively high, particularly for diode D, which is responsible to disconnect the input voltage source from the inverter transistor, during the shoot-through conduction. Hence, greater concerns are posed on D, since in the case of its failure due to excessive voltage stress, the whole power converter could be damaged. In the experimental setup, as shown in Chapter 8, these voltage peak value concern is even higher, due to the presence of stray inductances, which also contributes to the increase of overvoltage values. To solve the problem of overvoltage across D, it is mandatory to use the RC snubber, at least in the cases where this overvoltage could be greater than the ratings often found at different diode manufacturers. However, RC snubbers contribute to an increase in power loss and generate extra heat at the power board, which is highly undesirable.

Solution alternatives: To solve these problems, one can adopt lower values of δ, particularly between 2 and 3, which is directly related to overvoltage on the QSY network components. Another solution is to adopt lower $V_{DC\,link}$ values, using different control techniques such as MCBC with a third-harmonic injection or the selection of an optimized value of $V_{DC\,link}$ depending on the ancillary services executed by the converter.

2. **EMI issues –** The voltages and currents profile in many branches of the QSY inverter presents a pulsating nature. This is particularly true for the DC link voltage, in which the voltages vary from nearly 0 V to some hundred volts at the double switching frequency, which would cause problems related to electromagnetic interference (EMI). Therefore, the mitigation of EMI-related problems is more challenging in this converter.

   Solution alternatives: To mitigate EMI problems, one can choose to lower the DC link voltage, by choosing one of the possible alternatives described in the previous item. Besides, the adoption of EMI absorbing materials, optimized components, grounding and layout optimization, shielding, filtering, and many other possible solutions could be used to alleviate EMI problems.

3. **Capacitor high current ripple –**: The pulsating current that passes through capacitors C_1 and C_2 generates additional component stresses, besides greater power loss, since these components are series connected in power transfer branches. This problem can lead to a reduction in the converter's lifetime.

   Solution alternatives: One can use capacitors in parallel to reduce the current ripple in each component, thus increasing the life span of the converter. Another solution is to employ film capacitors along with electrolytic capacitors, as they have lower series resistances, higher ripple current capability, and longer lifespan. Moreover, increasing the switching frequency would eventually lead to minimized capacitance values, hence the use of less

critical materials, based on electrolytes, that could be replaced by other materials types that present increased durability in higher current ripple applications. However, the increase in the switching frequency should also consider the DSC PWM resolution capability, specially for higher values of δ, since D_{st} value decreases in this case.

4. **Leakage inductances issues –**: As described in item 1, the presence of the coupled-inductors leakage inductances and other stray inductances, promotes many problems related to overvoltages, in different components. As such, in some cases, the use of RC snubber for diode D and LCD snubber at the DC link is mandatory. The presence of these snubbers decreases the converter efficiency and increases the design complexity.
   Solution alternatives: If lower DC link voltages are used, the voltage spike at the diode D is minimized. Hence, one could employ higher voltage ratings diodes, and dismiss the use of the RC snubber. Regarding the LCD snubber, it employs fewer components with lower power ratings, does not require active switches, and can regenerate the leakage energy back to the QSY network. Using the design methodology that is currently being developed by the author's research group, the use of LCD snubber does not impose greater concerns.

5. **Increased current stress at inverter switches –**: The inverter switches that perform shoot-through conduction suffers higher current stresses and dissipate more switching power, as demonstrated in Chapter 7. Moreover, the peak current value at the shoot-through switches is relatively higher than the peak AC current. For example, in the application studied in Chapter 7, the shoot-through switch peak current was measured as 55 A, almost 4x higher than the inverter AC peak current value (15 A). This demands higher power ratings switches and additional care at the heat sink design, leading to an increase in the inverter cost and a reduction of the transistor lifetime.
   Solution alternatives: One solution to mitigate the increased switching power loss, and facilitate the semiconductor thermal control, relies on the definition of a "shoot-through inverter leg rotation" strategy. In this sense, the thermal stress could be homogeneously distributed among all inverter switches, increasing the lifetime of each individual switch. Considering the current technologies, if power MOSFETs-based switches are used, the shoot-through conduction could be done by all inverter legs at the same time, since MOSFETs can be gated on in parallel without additional concerns. Therefore, this would reduce the peak current value during shoot-through by the number of inverter legs. For example, in the case study in Chapter 7, the peak current during the shoot-through would be 18 A, which is only 1.2x higher than the AC peak current, and 3x lower than the case where the shoot-through is executed only by one inverter leg.

6. **Limitation of the modulation index range –**: Since part of the linear modulation index range is reserved for shoot-through pulse synthesis, there is a reduction in the maximum modulation index range in the QSY inverter. Compared with conventional inverters, this brings additional constraints during the execution of ancillary services and current

synthesis capability, particularly when harmonics currents compensation is required. ***Solution alternatives:*** To extend the modulation index range, one could adopt the utilization of SBC with the addition of third harmonic, which can increase M_{max} in 15%. Another solution is to realize selective harmonic compensation, using the available M range to fully compensate only the harmonic currents components of interest. Lastly, considering single-phase inverters based on the QSY network, there is a better utilization of the DC link, hence the problem of modulation index limitation is minimized when compared with the three-phase case.

As discussed above, the drawback of the QSY inverter cannot be fully eliminated but can be minimized if certain design and control decisions are made.

9.3 Final considerations

The experimental and simulation results demonstrate that the QSY inverter can effectively realize input voltage step-up while simultaneously executing ancillary services, using a single-stage power processing architecture. However, besides the positive characteristics associated with the single-stage power architecture in this converter, there is also a limitation on the maximum modulation index M_{max} range, which is now defined by 1-D_{st}. In this sense, the ancillary services execution capability of the QSY inverter, for the same DC link voltage, is lower when compared with other PV inverter topologies whose modulation index range can vary from 0 to 1. Particularly for harmonic current compensation, this limitation is more expressive, since higher modulation index values are required to inject higher-order frequency harmonic currents at the PCC. Nonetheless, when compared with other INI types, such as the Z-Source or Quasi-Z Source, since the QSY inverter can require lower D_{st} values to obtain the same desired voltage gain, thanks to the flexibility allowed by the δ factor, this difference of the ancillary services execution capability is smaller for the QSY inverter.

Yet, the execution of the shoot-through conduction dismisses the use of the dead-time protection feature in the drivers of transistors. This aspect brings some advantages, mainly related to the absence of distortions on the AC waveforms at the inverter output that can be caused when dead-time protection is enabled. Moreover, since shoot-through conduction is now permitted, an additional reliability degree is obtained in the QSY inverter, particularly against situations that could create unwanted shoot-through conduction in conventional VSI. However, it was demonstrated that additional thermal and switching losses are present due to this conduction type. Nonetheless, in the last section, it was indicated possible alternatives to alleviate this issue.

Besides the fact that the QSY inverter presents a single-stage power processing architecture, with its associated advantages, one must carefully determine the QSY network operational and design parameters, to avoid excessive voltage and current stress on critical components, such as the diode D, input inductor L_{in} and coupled-inductors windings. Among

the most critical design factors selection, there is the coupled-inductors δ factor, $V_{DC\,link}$ voltage, output processed power P_o, and voltage gain B.

Moreover, the coupled-inductors δ factor inserts an additional degree of freedom when determining the voltage gain, which can reduce the required values for D_{st}. This characteristic makes the QSY inverter design more flexible. However, the coupled inductors will unavoidably have leakage inductances, which can create problems related to overvoltages, particularly at the DC link, inverter switches, and diode D. To mitigate these issues, one could use snubber circuits, which need to be carefully designed to avoid unwanted power loss. In this sense, this aspect should be taken into consideration when designing the coupled inductors, such that lower leakage inductance values are obtained.

The capability of the QSY inverter to execute ancillary services, while simultaneously extracting maximum power from the PV array was demonstrated. However, when ancillary services are executed, all the QSY network components are affected, with greater current stresses at C_1, D, and the coupled-inductor winding with N_3 turns ratio. Moreover, additional voltage stresses will be present at C_2. Additionally, the inverter switches that perform shoot-through conduction also will face greater current stress and switching power losses at this condition, and the MPPT performance and efficiency are negatively affected. Therefore, the definition of the multifunctional service's mission profile that is requested from the QSY inverter should take these aspects into consideration, such that the converter's operational constraints are respected.

Furthermore, with the contributions made in this work, it is now possible to begin research studies using the QSY inverter in cooperative control scenarios, where the QSY inverter and other inverters types, present in a microgrid for example, are controlled synergically to achieve global energy generation or power quality goals.

Now, considering the drawbacks of the QSY PV three-phase inverter presented in this work, and despite the fact that a comparative analysis between the single-phase and three-phase QSY inverter was not carried out here, it is expected that some of the issues of the QSY inverter may be minimized in a single-phase micro-PV power generation scenario, due to the reduced values of processed power and required DC link voltages in this context. However, future studies need to be carried out to prove this hypothesis.

In summary, the QSY inverter presents interesting advantages and its main drawbacks can be reduced if the solutions alternatives given in this work are considered. Hence, further research studies in this area are justified. Finally, the present study can aid the conduct of further studies considering the use of the QSY network and other magnetically coupled impedance source inverters in PV power generation applications.

10 Future work

Multiple development paths still needed to be explored considering the application of the QSY inverter in a multifunctional context. Below, there is a non-exhaustive list of possible future work topics.

1. **Single-phase micro-generation scenario**: As discussed in the Conclusion chapter, the utilization of the QSY inverter in a single-phase scenario could present more advantages when compared with the three-phase one. In this sense, the conduction of future research in this area, using the methodologies proposed in this work, is an interesting research path alternative.

2. **Discontinuous conduction mode scenario**: In this work, it was considered that the input current of the QSY inverter operates in continuous conduction mode. However, there is also the possibility of operating the converter in discontinuous conduction, which could bring new possibilities and features for the converter. Future analysis could be done to better explore this situation.

3. **Optimization of coupled-inductors design**: The coupled-inductors design could be improved, with the development of a methodology that results in lower core power losses, equivalent series resistances, and decreased operational temperature.

4. **Inverter shoot-through leg rotation strategy**: To mitigate problems related to switching power loss due to the shoot-through conduction, future studies can develop inverter shoot-through leg rotation strategies, to equally distribute the thermal stresses among the inverter switches.

5. **Multiple MPPT trackers control strategy**: The QSY inverter scheme presented in this work has only one MPP tracker since there is only one connection to the PV array at the input stage. However, it is possible to connect another PV array in parallel with capacitor C_1, and a different MPPT control strategy could be defined to handle this new situation.

6. **Definition of a transformerless galvanic isolation strategy**: There is an increasing trend in using transformerless PV inverters. Regarding the QSY inverter, future studies can propose hardware or control modifications that enable galvanic isolation without the need of inserting transformers, reducing the issues related to PV leakage currents.

7. **Optimal exploitation of ancillary services execution**: Future studies can define different control strategies that enable improved exploitation of the ancillary services capacity of the QSY inverter. To achieve this objective, the definition of optimum DC link voltage values,

selective harmonic compensation control scheme, or the insertion of a third harmonic to increase the M range could be considered as alternatives.

8. **MPPT techniques considering partial shading**: In PV power generation systems, partial shading is a common problem. In this work, the MPPT technique employed did not take care of this issue. Plenty of multiple MPPT techniques can be used in partial shading scenarios. Among these techniques that can be found in the literature, (SAJADIAN; AHMADI; ZARGARZADEH, 2018) proposed an MPC technique that is more suitable for impedance-source network converters. Based on this reference, future studies can be carried out to develop more sophisticated MPPT strategies for the QSY inverter.

9. **Application of the QSY inverter in cooperative control scenarios**: As mentioned in the Conclusion Chapter, with the methodologies developed in this work, it is possible to conduct future studies using the QSY inverter in cooperative control scenarios, exploiting the characteristics of this converter in this new context.

10. **Solutions for EMI issues**: The QSY inverter has pulsating current and voltage waveforms. This characteristic implies a greater concern regarding issues related to electromagnetic interference. Hence, future work can be done to explore solutions to this aspect of the converter.

11. **Non-ideal grid voltage case study**: In this work, the grid voltage is assumed to be balanced and purely sinusoidal. However, in reality, grid voltage imbalance and the presence of harmonic content may occur. Therefore, the behavior of the QSY inverter could be investigated in this case, considering controller stability, MPPT, and PLL tracking performance, and other operational aspects in this adverse scenario.

12. **Further studies of ancillary services execution impact on QSY inverter**: Additional comparative analyses can be undertaken by examining various scenarios in which the QSY inverter provides ancillary services. For example, a comparison can be made between the scenarios in which the QSY inverter injects both active power and ancillary services during the day and the one in which it injects only active power during the day while executing ancillary services exclusively at night. This comparative assessment will provide insights into the operational stresses on the converter.

13. **Control system stability analysis**: The various control loops within the QSY inverter system exhibit a degree of coupling, potentially influencing the relative stability margins of the closed-loop system. Therefore, future studies can be made to assess this situation and determine the operational conditions needed to ensure stability.

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Appendix

APPENDIX A – Coupled-Indutor data

Table A.1 – Coupled inductors data

Core	TT 13500-5
N_1:N_2:N_3	37:112:186 $\approx$ (1:3:5)
Possible δ values - N_1:N_2:N_3	2 - 3:5:1 3 - 1:5:3 4 - 5:3:1
$I_{RMS-max}$ per winding	15 A
I_{pk} per winding	32 A
V_{pk} per winding	900 V
Operational frequency	18 kHz
Geometry	Toroidal
Core material	Sendust S60
Magnetic permeability	60 H/m
Winding type	Litz - 6x20 AWG
L_{k3eq} - N_1:N_2:N_3	5.30 μH - 3:5:1 5.30 μH - 5:3:1 9.08 μH - 1:5:3
L_m - N_1:N_2:N_3	2.09 mH - 3:5:1 5.74 mH - 5:3:1 0.217 mH - 1:5:3
L_{k1}, L_{k2}, L_{k3} - N_1:N_2:N_3	4.04, 14.93, 4.86 μH- 3:5:1 14.93, 4.04, 4.86 μH- 5:3:1 4.86, 14.93, 4.04 μH - 1:5:3
r_{N1}, r_{N2}, r_{N3} - N_1:N_2:N_3	0.45 , 1.04, 0.08 Ω- 3:5:1 1.04, 0.45 , 0.08 Ω- 5:3:1 0.08, 1.04, 0.45 Ω - 1:5:3
Weight	2.4 kg
ϕ_{ext}, ϕ_{int}, height	144, 66, 37 mm

APPENDIX B – LCD snubber flowchart

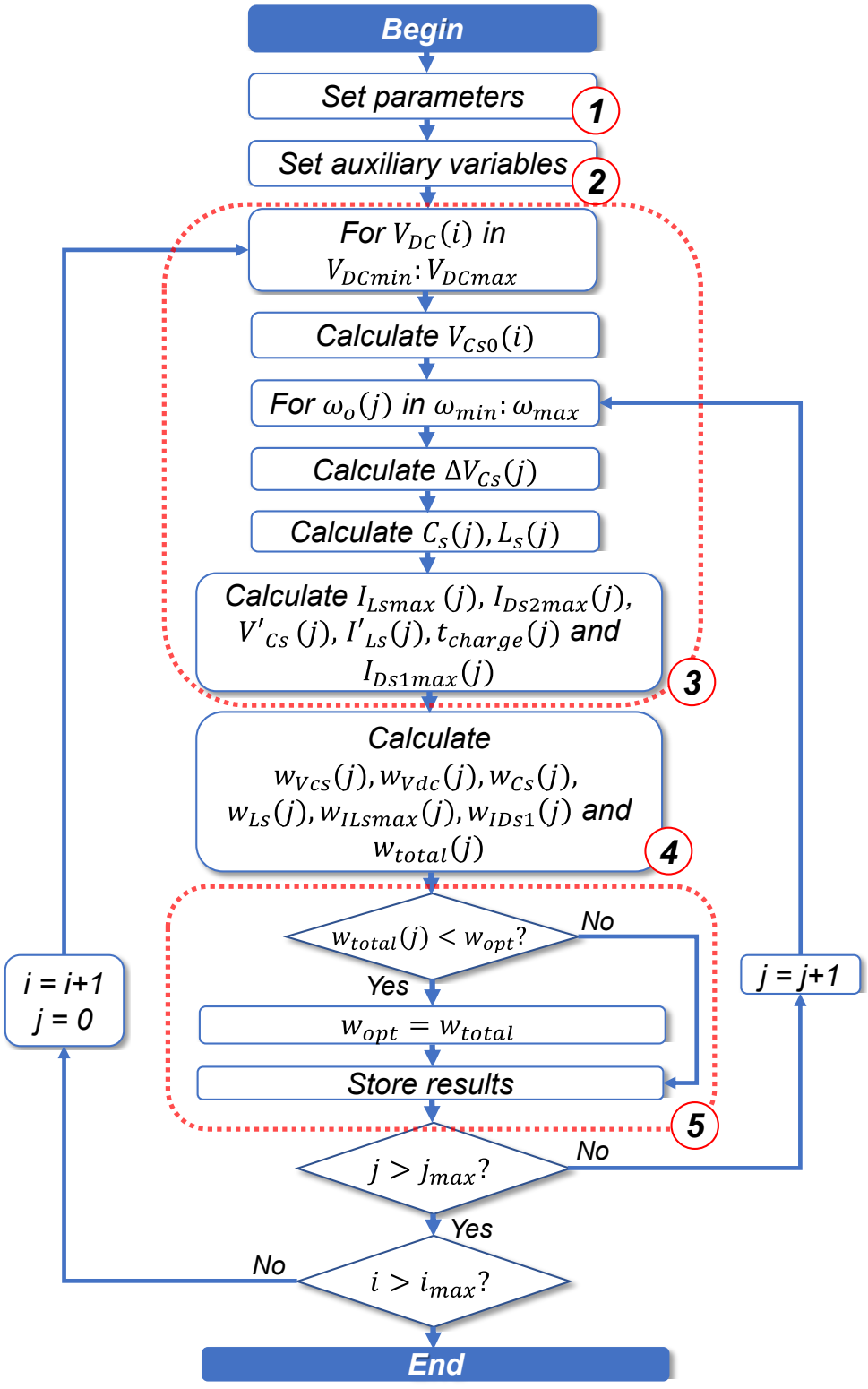

Figure B.1 – Design algorithm flowchart

APPENDIX C – A_1 and A_2 matrices λ factors

$$\lambda_1 = -\frac{r_{Lin} + r_{N1} + r_{C2} + \delta' \left(r_{N2} + r_{C1}\right) + \delta \left(\delta \left(r_{N3} + r_S\right) - \delta' \left(r_{N2} + r_{C1}\right)\right)}{L_{in}} \quad \text{(C.1)}$$

$$\lambda_2 = \frac{N_1 \left(\delta\, r_{N2} - r_{C1} - r_{N2} + \delta\, r_{N3} + \delta\, r_S + \delta\, r_{C1}\right)}{L_{in} \left(N_2 - N_3\right)} \quad \text{(C.2)}$$

$$\lambda_3 = \frac{\delta - 1}{L_{in}} \quad \text{(C.3)}$$

$$\lambda_4 = \frac{1}{L_{in}} \quad \text{(C.4)}$$

$$\lambda_5 = \frac{N_1 \left(\delta \left(r_{N3} + r_S\right) - \delta' \left(r_{N2} + r_{C1}\right)\right)}{L_m \left(N_2 - N_3\right)} \quad \text{(C.5)}$$

$$\lambda_6 = -\frac{{N_1}^2 \left(r_{N2} + r_{N3} + r_S + r_{C1}\right)}{L_m \left(N_2 - N_3\right)^2} \quad \text{(C.6)}$$

$$\lambda_7 = -\frac{N_1}{L_m \left(N_2 - N_3\right)} \quad \text{(C.7)}$$

$$\lambda_8 = \frac{\delta'}{C_1} \quad \text{(C.8)}$$

$$\lambda_9 = \frac{N_1}{C_1 \left(N_2 - N_3\right)} \quad \text{(C.9)}$$

$$\lambda_{10} = -\frac{1}{C_2} \quad \text{(C.10)}$$

$$\lambda_{11} = \frac{-(r_{N1} + r_{C2})}{L_{in}\, \delta'^2} - \frac{(r_{N2} + r_{Lin} + r_{C1})}{L_{in}} + \frac{N_1 + N_2}{L_{in}\, \delta' \left(N_1 + N_3\right)} \delta \left(r_D + r_{N3}\right) \quad \text{(C.11)}$$

$$\lambda_{12} = \frac{r_{N1} + r_{C2}}{L_{in}\, \delta'^2} + \frac{r_{N2} + r_{C1}}{L_{in}} + \left(-\frac{N_1 + N_2}{L_{in}\, \delta' \left(N_1 + N_3\right)}\right) \left(r_{N3}\, \delta + r_D\right) \quad \text{(C.12)}$$

$$\lambda_{13} = \left(\frac{N_1 \left(N_1 + N_2\right)}{\left(N_1 + N_3\right)^2} - \frac{N_1}{\left(N_1 + N_3\right)}\right) \frac{(r_{N1} + r_{C2})}{L_{in}} + \frac{N_1 \left(N_1 + N_2\right)}{\left(N_1 + N_3\right)^2} \frac{(r_{N3} + r_D)}{L_{in}} \quad \text{(C.13)}$$

$$\lambda_{14} = -\frac{1}{L_{in}} \quad \text{(C.14)}$$

$$\lambda_{15} = -\frac{N_2 - N_3}{L_{in} \left(N_1 + N_3\right)} \quad \text{(C.15)}$$

$$\lambda_{16} = -\frac{(r_D\, \delta + r_{N1} + r_{C2})}{L_o\, \delta'^2} + \frac{r_{N2}}{L_o} + \left(-\frac{N_1 + N_2}{L_o\, \delta' \left(N_1 + N_3\right)}\right) r_{N3}\, \delta + \frac{r_{C1}}{L_o} \quad \text{(C.16)}$$

$$\lambda_{17} = -\frac{(r_D + r_{N1} + r_{C2})}{L_o\, \delta'^2} - \frac{(r_{N2} + r_{C1} + R_o)}{L_o} + \frac{N_1 + N_2}{L_o\, \delta' \left(N_1 + N_3\right)} r_{N3}\, \delta \quad \text{(C.17)}$$

$$\lambda_{18} = \left(\frac{N_1}{\left(N_1 + N_3\right)} - \frac{N_1 \left(N_1 + N_2\right)}{\left(N_1 + N_3\right)^2}\right) \frac{(r_D + r_{N1} + r_{C2})}{L_o} - \left(\frac{N_1 \left(N_1 + N_2\right)}{\left(N_1 + N_3\right)^2}\right) \frac{r_{N3}}{L_o} \quad \text{(C.18)}$$

$$\lambda_{19} = \frac{1}{L_o} \quad \text{(C.19)}$$

$$\lambda_{20} = \frac{N_2 - N_3}{L_o\ (N_1 + N_3)} \quad \text{(C.20)}$$

$$\lambda_{21} = -\frac{N_1(\delta(r_D + r_{N3})\ + r_{N1} + r_{C2})}{L_m\,\delta'\ (N_1 + N_3)} \quad \text{(C.21)}$$

$$\lambda_{22} = \frac{N_1(r_D + r_{N1} + r_{N3}\delta + r_{C2})}{L_m\,\delta'\ (N_1 + N_3)} \quad \text{(C.22)}$$

$$\lambda_{23} = -\frac{{N_1}^2(r_D + r_{N1} + r_{N3} + r_{C2})}{L_m\,(N_1 + N_3)^2} \quad \text{(C.23)}$$

$$\lambda_{24} = \frac{N_1}{L_m\ (N_1 + N_3)} \quad \text{(C.24)}$$

$$\lambda_{25} = \frac{1}{C_1} \quad \text{(C.25)}$$

$$\lambda_{26} = -\frac{1}{C_1} \quad \text{(C.26)}$$

$$\lambda_{27} = -\frac{1}{C_2\,\delta'} \quad \text{(C.27)}$$

$$\lambda_{28} = \frac{1}{C_2\,\delta'} \quad \text{(C.28)}$$

$$\lambda_{29} = -\frac{N_1}{C_2\ (N_1 + N_3)} \quad \text{(C.29)}$$