Thickness dependence of leakage current in $BaBi_2Ta_2O_9$ thin films

C. R. Foschini, E. Longo, J. A. Varela, and S. B. Desu

Citation: Applied Physics Letters **75**, 552 (1999); doi: 10.1063/1.124419
View online: http://dx.doi.org/10.1063/1.124419
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/75/4?ver=pdfcov
Published by the AIP Publishing

Thickness dependence of leakage current in $BaBi_2Ta_2O_9$ thin films

C. R. Foschini,[a)] E. Longo, and J. A. Varela
Instituto de Química, Universidade Estadual Paulista-UNESP, 14801-970 Araraquara, SP, Brazil

S. B. Desu
Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, Massachusetts 01003

(Received 4 January 1999; accepted for publication 23 May 1999)

$BaBi_2Ta_2O_9$ thin films having a layered structure were fabricated by metalorganic solution deposition technique. The films exhibited good structural, dielectric, and insulating properties. The room temperature resistivity was found to be in the range of 10^{12}–$10^{14}\,\Omega\,$cm up to 4 V corresponding to a field of 200 kV/cm across the capacitor for films annealed in the temperature range of 500–700 °C. The current-voltage $(I-V)$ characteristics as a function of thickness for films annealed at 700 °C for 1 h, indicated bulk limited conduction and the log(I) vs $V^{1/2}$ characteristics suggested a space-charge-limited conduction mechanism. The capacitance–voltage measurements on films in a metal–insulator–semiconductor configuration indicated good Si/$BaBi_2Ta_2O_9$ interface characteristics and a SiO_2 thickness of ~5 nm was measured and calculated. © *1999 American Institute of Physics.* [S0003-6951(99)00830-X]

In recent years, there has been considerable interest in the ferroelectric Aurivillius compounds, since such materials are widely used in technical devices. $BaBi_2Ta_2O_9$ (BBT) belongs to the layer-perovskite family with a Curie temperature of 110 °C and a dielectric constant of 400, measured in bulk ceramics by Subbarao.[1] BBT thin films is an attractive material for very large scale integrated devices such as dynamic random-access memories (DRAMs) because of its high charge storage capacity, good insulating property, and low leakage current.[2,3] The application of BBT thin films to DRAM capacitors would enable the realization of ultralarge scale integrated DRAMs cells with a simple stacked structure.

An approach to replace the existing SiO_2 based dielectrics is the use of high dielectric constant ϵ_r materials.[4,5] The problem with high dielectric constant materials is that most of them cannot be directly deposited on silicon. Moreover, the integration requires development of high temperature stable barrier-electrode systems, because of the interaction between the components. Among the high dielectric constant materials are Ta_2O_5 ($\epsilon_r=22$) and (Ba, Sr)TiO_3 ($\epsilon_r=400$). However, both have leakage current problems and the later have titanium, which rapidly diffuses into silicon and forms titanium silicide. Apart from this there is a possibility that BBT could be directly deposited onto Si substrate.

This letter describes the preparation of BBT thin films by metalorganic solution deposition (MOSD) technique and its electrical characterization in terms of leakage current. The MOSD process, like almost all chemical methods, is well known in the area of processing thin films because of easier composition control, better homogeneity, low processing temperature (compatible with Si processing), easier fabrication of large area thin films, and low cost.[6]

Thin films of $BaBi_2Ta_2O_9$ were fabricated using barium acetate $(BaOOCCH_3)_2$, bismuth 2-ethylhexanoate $(Bi(C_7H_{15}COO)_3)$, and tantalum ethoxide $(Ta(OC_2H_5)_5)$ as precursors. Acetic acid, 2-ethylhexanoic acid and 2-methoxyethanol were selected as solvents. Bismuth 2-ethylhexanoate and barium acetate precursors were dissolved in 2-ethylhexanoic acid and acetic acid, respectively, under room temperature conditions. These solutions were then added to the solution of tantalum ethoxide in 2-methoxyethanol. The precursors films were deposited onto platinum coated silicon and bare silicon substrates by spin coating operated at 6000 rpm for 40 s. After spinning, films were kept on a hot plate at 350 °C in air for 10 min. After each coating this step was repeated to ensure complete removal of volatile matter. The crystallinity of the films was examined by x-ray diffraction (XRD) and the cross-section silicon interface by transmission electron microscopy. The thickness of the films was measured by variable angle spectroscopy ellipsometry. The electrical properties reported include dielectric, capacitance–voltage, and current–voltage $(I-V)$. The electrical measurements were conducted on films in metal–insulator–metal (MIM) or metal–insulator–semiconductor (MIS) configurations using Pt as the top and bottom (MIM) electrodes. The top electrodes, area$=3.1\times10^{-4}\,cm^2$, were deposited on the surface of films by sputtering through a shadow mask. The dielectric properties were measured with a HP 4192A impedance analyzer at room temperature and the leakage $I-V$ characteristics were measured by means of a Keithley 617 electrometer/source.

The pyrolyzed films (at 350 °C) were found to be amorphous and postdeposition annealing was required to develop crystallinity. The structure of the films was analyzed by a Scintag XDS 2000 diffractometer using Cu K_α radiation at 40 kV. Figure 1 shows the XRD patterns of films annealed in the range of 450–700 °C for 60 min. A well-crystallized orthorhombic phase was attained at 700 °C. The XRD patterns also revealed that films were polycrystalline in nature with no evidence of preferred orientation or secondary phases. The significantly lower processing temperature of

[a)]Electronic mail: foschini@iq.unesp.br

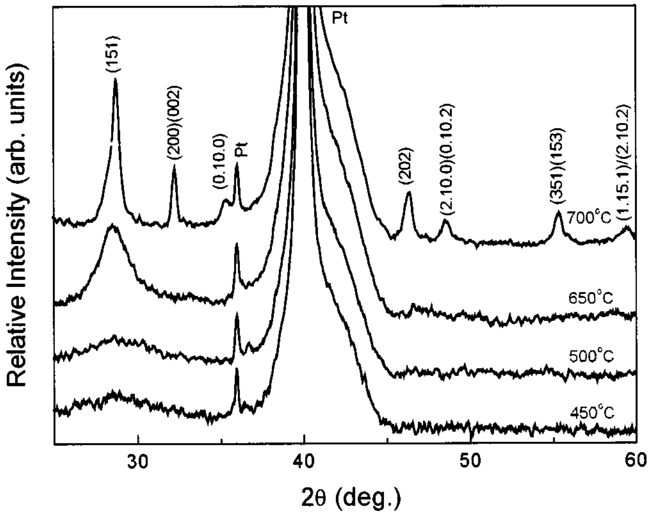

FIG. 1. X-ray diffraction patterns of BBT thin films annealed at different temperatures for 60 min.

BBT thin films compared to bulk sintering temperature shows the possibility of exploiting thin films for microelectronic devices. The films also exhibited a dense microstructure and the grain size was very fine.

The characteristics of electrical conduction were measured using MIM capacitors. The insulating properties of the films were found to be dependent on the temperature of annealing. As shown in Fig. 2, room temperature resistivity and leakage current density were greatly changed by the annealing temperature. The room temperature resistivity was found to be in the range of 10^{12}–$10^{14}\,\Omega$ cm up to 4 V corresponding to a field of 200 kV/cm across the capacitor for films annealed in the temperature range of 500–700 °C. The leakage current density decreased with increase in the annealing temperature. Such reduction in leakage current density with increasing annealing temperature may be attributed to improved crystallinity and oxidation, leading to near perfect stoichiometry and completeness of the phase formation. Typical leakage current densities were lower than 10^{-9} A/cm^2 at an applied electric field of 200 kV/cm for films annealed at 700 °C for 1 h.

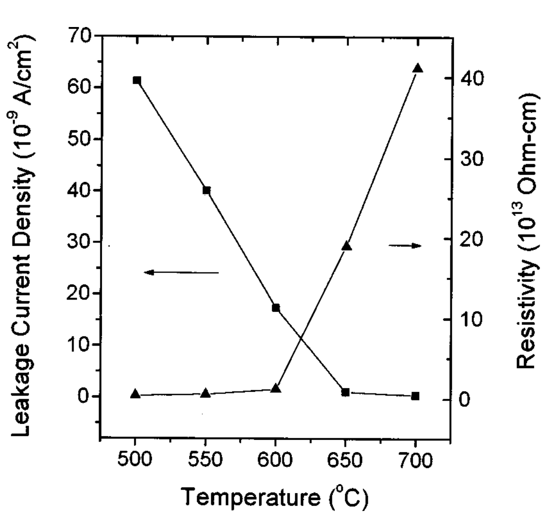

FIG. 2. Room temperature resistivity and leakage current density of $BaBi_2Ta_2O_9$ films as a function of annealing temperature, measured at an applied electric field of 200 kV/cm.

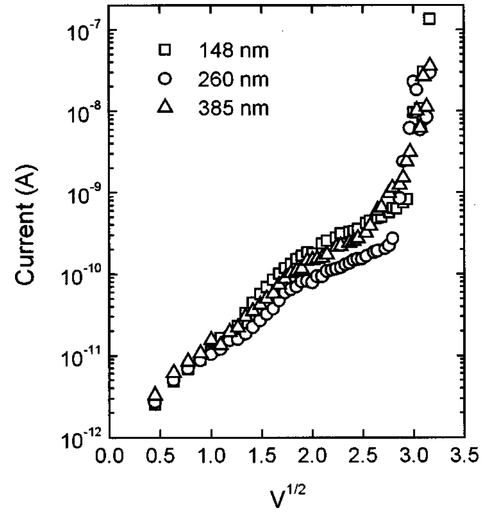

FIG. 3. Log(I) vs $V^{1/2}$. The nonlinearity indicates the absence of the Poole–Frenkel effect.

An understanding of the mechanism of nonlinear conductivity in thin film insulators is pertinent to the development of thin film devices for microelectronics. The steady state field dependent dc conductivity was examined through the measurement of the $I-V$ characteristics in MIM capacitors. Several electrical processes allow electrical charges to move in insulators, leading to sizable current densities. The low field properties are usually ohmic in nature, that is, current I is linear with voltage V. At high fields these behavior can be expressed by the empirical power law $I=KV^{\alpha}$, where K is a proportionality constant. Generally, the high field characteristics cannot be adequately described by a single conduction process; usually at different field strength ranges manifest different electrical phenomena. The thickness dependence of the $I-V$ characteristics indicated bulk limited conduction.[7–9] These films exhibited high resistivities in the range of 10^{12}–$10^{14}\,\Omega$ cm at an applied electric field of 200 kV/cm, for 150–400 nm thick films. In this range of resistivities, the possible dominant conduction mechanisms may be: (a) tunneling, (b) Poole–Frenkel effect, and/or (c) space-charge-limited conduction. As the thickness of the films was above 100 nm, the tunneling process was ruled out. If the non-ohmic conduction is due to Poole–Freenkel flow, then we should get a straight line in log(I) against $V^{1/2}$ plot, which was not found in our case, as can be seen from Fig. 3. So the dominant bulk limited conduction mechanism was expected to be space-charge-limited-current (SCLC) conduction.

From the compatibility point of view, it is important to study the Si/thin film interface. The thickness of the SiO_2 layer was calculated from the capacitance measurements on BBT thin films with 10% excess bismuth annealed at 700 °C/1 h using the MIS configuration, as schematized in Fig. 4. Platinum top electrodes, deposited by sputtering, of 3.1×10^{-4} cm^2 were used to form this structure. The total

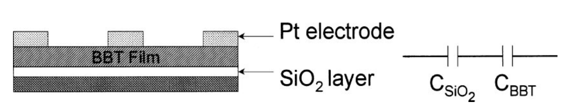

FIG. 4. Schematic MIS structure used to calculate the SiO_2 thickness layer.

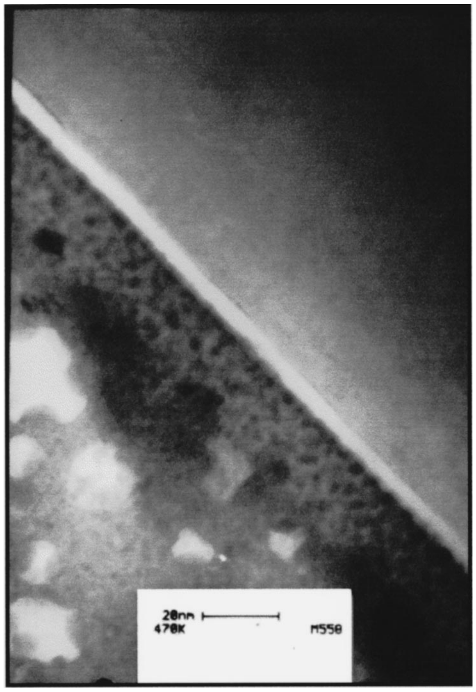

FIG. 5. Cross-sectional transmission electron microscope micrograph showing a 5 nm SiO_2 thickness layer.

capacitance measured in this configuration at 100 kHz was 140 pF.

The total capacitance C_{Tot} is modeled as consisting of two capacitances in series, i.e., those of the BBT layer C_{BBT}, and those of the SiO_2 layer C_{SiO_2}. Therefore, the total capacitance is given by

$$\frac{1}{C_{Tot}}=\frac{1}{C_{SiO_2}}+\frac{1}{C_{BBT}}, \quad (1)$$

where each capacitance is given by

$$C=\frac{\epsilon_0\epsilon_r A}{d}, \quad (2)$$

where ϵ_r and d are the dielectric constant and the thickness of the SiO_2 layer or the BBT layer, ϵ_0 is the permittivity of free space, and A is the area of the electrode spot being tested. Assuming the values of $\epsilon_{r,SiO_2}=3.9$;[5] $\epsilon_{r,BBT}=283$;[3] $d_{BBT}=187$ nm measured by ellipsometry for this particular specimen, and rearranging Eq. (2)

$$d_{SiO_2}=\frac{\epsilon_0\epsilon_{SiO_2}A}{C_{SiO_2}}=5.06\,\text{nm}. \quad (3)$$

The thickness of the SiO_2 layer in this specimen was also measured from cross-sectional transmission electron microscopy. As can be seen in Fig. 5, the measured thickness for the SiO_2 layer is about 5 nm and agrees very well with the calculated value from the capacitance data.

In conclusion, $BaBi_2Ta_2O_9$ thin films with crystalline structure were successfully prepared by the metalorganic solution deposition technique on Pt-coated Si and n^+Si substrates. Very well-crystallized BBT thin films were obtained after annealing at 700 °C for 60 min. The room temperature resistivity was found to be in the range of 10^{12}–10^{14} Ω cm up to 4 V corresponding to a field of 200 kV/cm across the capacitor for films annealed in the temperature range of 500–700 °C. Typical leakage current densities were lower than 10^{-9} A/cm^2 at an applied electric field of 200 kV/cm for films annealed at 700 °C for 1 h. The thickness dependence of the I–V characteristics indicated bulk limited conduction mechanism and the dominant conduction mechanism was expected to be SCLC conduction. The SiO_2 thickness layer ~5 nm indicated good Si/BBT interface characteristics.

The authors are grateful for the support of the FAPESP, CNPq, CAPES, and FINEP/PRONEX agencies from Brazil.

[1] E. C. Subbarao, J. Phys. Chem. Solids **23**, 665 (1962).
[2] C. A-Paz de Araujo, J. D. Cuchiaro, L. D. McMillan, M. C. Scott, and J. F. Scott, Nature (London) **374**, 627 (1995).
[3] C. R. Foschini, P. C. Joshi, J. A. Varela, and S. B. Desu, J. Mater. Res. **14**, 1860 (1999).
[4] P. C. Fazan, H. C. Chan, and V. K. Mathews, Semicond. Int. May, 108 (1992).
[5] M. Anthony, S. Summerfelt, and C. Teng, T. I. Tech. J., Sep–Oct, 30 (1995).
[6] L. C. Klein, *Sol-Gel Technology for Thin Film, Fibers, Performs, Electronics and Specialty Shapes* (Noyes, Park Ridge, NJ, 1988).
[7] M. Stuart, Phys. Status Solidi **23**, 595 (1967).
[8] M. Roth and A. Burger, Appl. Phys. Lett. **52**, 1234 (1988).
[9] A. E. Rakhshani, J. Appl. Phys. **69**, 2365 (1991).