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CARLOS AUGUSTO ZAN MALAGUTI

FABRICATION AND ELECTRICAL CHARACTERIZATION OF NEW MATERIALS FOR METAL-OXIDE-SEMICONDUCTOR TECHNOLOGY

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Undergraduate Thesis presented to Sao Paulo State University "Júlio de Mesquita Filho" as a requirement to obtain the Bachelor's Degree in Electronics and Telecommunication Enginnering.

Advisor: Dr. Paula Ghedini Der Agopian
External Advisor: Dr. Muhammad Mustafa Hussain

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TRABALHO DE CONCLUSÃO DE CURSO

FABRICATION AND ELECTRICAL CHARACTERIZATION OF NEW MATERIALS FOR METAL-OXIDE-SEMICONDUCTOR TECHNOLOGY

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“O sucesso não tem a ver com quanto dinheiro você ganha, mas sim com a diferença que você faz na vida de outras pessoas”

- Michele Obama

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Abstract

The Metal-Oxide-Semiconductor (MOS) technology has played a key role in the IC industry since its inception due to its excellent characteristics in digital applications, high scalability, ease of manufacturing processes, among others [1].

However, as early as the 21st century, MOSFET (Metal Oxide Semiconductor Field Effect Transistor), one of the most important devices of MOS technology, had been suffering some unwanted effects caused by the extreme miniaturization of integrated circuits. This facilitated the rise of another technology, Silicon-On-Insulator (SOI), which was more attractive to some applications, further simplifying manufacturing processes and performing better. Thus, it is now known that high performance SOI substrate-based MOS circuits are critical to any advanced electronic system.

In the evolving context of integrated circuits, alternative semiconductor-based electronic systems (II-VI) can be a watershed, sparking a new revolution in nanoelectronics. Composite semiconductors such as zinc oxide and high dielectric constant insulators such as hafnium oxide have been very attractive in today's applications, due to its interesting physical properties, which can lead to transparent and organic-compatible electronics.

Therefore, in this project, various aspects of manufacturing processes involving silicon-alternative materials will be analyzed, which will require a strong grounding in solid-state device physics and manufacturing processes, as well as study of material and electrical properties.

The impact of this study is of major importance for next generation computing, including big data, cloud computing, IoT, cyber-physical systems and augmented reality, clean and renewable energy, and numerous health and fitness applications.

Keywords: II-VI Semiconductors, MOS Technology, Nanofabrication.

Resumo

A tecnologia Metal-Óxido-Semicondutor (MOS), teve papel fundamental na indústria de CIs desde o início, devido às suas excelentes características em aplicações digitais, alta escalabilidade, facilidade de processos de fabricação, entre outros [1].

No entanto, ainda no início do século XXI, a tecnologia MOSFET vinha sofrendo alguns efeitos indesejados causados pela extrema miniaturização dos circuitos integrados. Isso facilitou a ascensão de uma outra tecnologia, a Silicon-On-Insulator (SOI), tendo sido mais atraente para algumas aplicações, simplificando ainda mais os processos de fabricação e apresentando melhor desempenho. Assim, sabe-se que atualmente circuitos MOS de alto desempenho baseados em substrato SOI são fundamentais para qualquer sistema eletrônico avançado.

No contexto evolutivo de circuitos integrados, sistemas eletrônicos baseados em semicondutores alternativos (II-VI) podem ser um divisor de águas, protagonizando uma nova revolução na nanoeletrônica. Semicondutores composto como o óxido de zinco e isolantes de alta constante dielétrica, como o óxido de háfnio, tem se mostrado muito atraentes em aplicações atuais, inclusive apresentando propriedades físicas interessantes, podendo dar origem a eletrônicos transparentes e com compatibilidade à orgânicos.

Portanto, neste projeto, serão analisados vários aspectos dos processos de fabricação envolvendo materiais alternativos ao silício, o que necessitará de uma forte base em física de dispositivos de estado sólido e processos de fabricação, bem como estudo de propriedades dos materiais e elétrica.

O impacto deste estudo é de grande importância na computação de próxima geração, incluindo *big data*, computação em nuvem, IoT, sistemas ciber-físicos e realidade aumentada, energia limpa e renovável, além de inúmeras aplicações na área da saúde e condicionamento físico.

Palavras-chave: Semicondutores II-VI, Tecnologia MOS, Nanofabricação.

List of Illustrations

List of Acronyms and Abbreviations

KAUST	King Abdullah University of Science and Technolgy
NCL	Nanofabrication Core Labs
INL	Integrated Nanotechnology Laboratory
MOS	Metal – Oxide - Semiconductor
IC	Integrated Circuit
MOSFET	Metal – Oxide – Semiconductor Field Effect Transistor
SOI	Silicon – On - Insulator
IoT	Internet of Things
CMOS	Complementary Metal – Oxide - Semiconductor
SCE	Short Channel Effect
FD	Fully Depleted
PD	Partially Depleted
MOSCAP	Metal – Oxide – Semiconductor Capacitor
CVD	Chemical Vapor Deposition
PECVD	Plasma Enhanced Chemical Vapor Deposition
ALD	Atomic Layer Deposition
TALD	Thermal Atomic Layer Deposition
XRD	X-Ray Diffraction
SEM	Scanning Electron Microscopy
ISO	International Standards Organization
AZO	Aluminum Oxide doped Zinc Oxide
DEZ	Diethylzinc
TMA	Trimethylaluminium
IoE	Internet of Everything
BSE	Backscattered Scanning Electon

List of Symbols

V_G	Gate voltage [V]
V_D	Drain voltage [V]
V_S	Source voltage [V]
L	Channel length [nm]
I_{DS}	Drain current [A]
μ	Carriers mobility [cm^2/Vs]
C_{OX}	Gate oxide capacitance [F]
V_T	Threshold voltage [V]
W	Channel width [nm]
t_{Si}	Channel thickness [nm]
X_{Dmax}	Depletion region length [nm]
R_S	Sheet resistance [Ω/sq]
P	Resistivity [Ω.cm]
τ	Film thickness [nm]
C	Correction factor [a.u.]

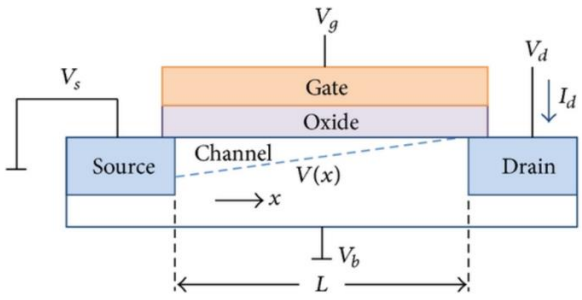
Summary

1. Introduction

In the 1970 decade, Gordon Earl Moore, from Intel, established a concept that later became known as Moore's Law, and it has been driven the semiconductor industry for many years. His Law stated that the processing power of computation should double every 18 months. In other words, the number of transistors in a given area should double almost every two years, which, in thesis, should double the processing performance of a system, keeping the price every year. The role of Silicon became indispensable to the semiconductor industry because this abundant material had the needed properties to the fabrication of the transistors, the most important devices of the electronics world [1].

Transistors can be considered nerve cells of the Information Age, deeply embedded in almost every electronic device. It is a semiconductor device responsible for controlling and accomplishing the vast number of numerical operations and calculations needed for a computer to operate correctly [2]. Silicon devices can be built of different materials and dopant types, depending on the application it will be used. The most common configuration of a transistor is a 3 terminal device, and the technology widely used by the semiconductor and electronics industry over the years was the well-know Metal Oxide Semiconductor technology, shown in the Figure 1.

Figure 1 - Basic MOS device structure cross-section.



(Adapted, David H. K. HoeXiaoyu Jin, 2015)

The Metal-Oxide-Semiconductor Field Effect transistors, in its most used technology (CMOS), had a fundamental role in the ICs industry since it’s invention, due to its excellent characteristics in digital applications, high scalability, simple fabrication processes. As time was passing, the semiconductor industry was running to keep the Moore’s Law valid, and the devices should be smaller and smaller, to allow the fabrication of more transistors per chip. In principle, shrinking the devices wasn’t a problem once the channel length was inversely proportional to the level of ON-state current, as shown in Equation 1, which means that the

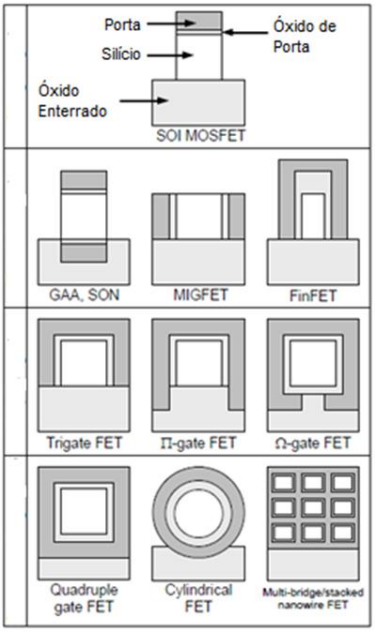
performance of the devices would be better. Nevertheless, after a while, some unwanted and effects caused by the extreme device miniaturization started to degrade the performance of them. The Short Channel Effect (SCE), one of the most known effects, became so important that the industry began to find ways to overcome it [3].

$$I_{DS} = \mu . C_{OX} . \frac{W}{L} . \frac{(V_{GS} - V_T)\,(V_{GS} - V_T)^2}{2} \quad (1)$$

One of the solutions firstly found was the use of a new type of wafer, instead of the Bulk one: The Silicon-On-Insulator (SOI). With the SOI wafer, transistors would be completely isolated from the rest of the substrate, which could reduce or suppress some unwanted effects. The SOI transistors can be classified depending on the silicon film thickness (t_{Si}) and channel doping concentration. The thin silicon film transistor (where $t_{Si} < X_{dmax}$) is classified as a fully depleted device (FD), while for thick Silicon film (where $t_{Si} > 2.X_{dmax}$) is a partially depleted one (PD) [4].

Nonetheless, even devices fabricated in SOI wafers started to suffer from the extreme shrinking, and other solutions were required. In 2011, Intel introduced the revolutionary 22nm Transistor Technology, a Tri-Gate device which had a 3D (Fin) architecture [5]. Other architectures were being investigated mainly by academia, such as nanowire, omega gate, gate all around, etc., as shown in Figure 2.

Figure 2 - Transistors' geometry according to the number of gates

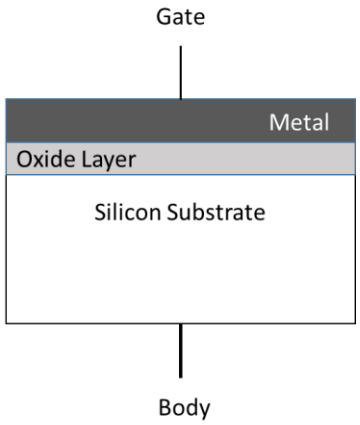


Adapted, J. P. Colinge, 2008

However, the essential and elemental part, commom to any MOS transistor, is its isolating gate that controls the current flow in a channel, regardless of its geometry, as shown

in Figure 2, the working principle is always the same. The basic structure formed by the gate metal material, the gate insulator, and the channel semiconductor, which together forms the MOS capacitor structure, as known as MOSCAP, shown in the figure 3. This structure can be considered the heart of every field effect transistor, and a good understanding and analysis of this structure can show us important parameters of the transistor performance [6].

Figure 3 - MOS Capacitor Structure



(Author)

Nowadays, the needs of using micro and nanoelectronic circuits have been focused on the most diverse areas, to contribute to the development of the "Internet of Everthing" (IoE). Therefore, chips embedded in certain types of sensors and smart devices require, among many other things: small size, high performance, connectivity, and, above all, flexibility and mechanical elasticity [7].

To that end, some techniques have been investigated to turn conventional hard silicon wafers into flexible ones, as it would be possible the use in wearable applications, for example. But the study of new semiconductor materials is also needed. Silicon has its limitations, and the industry is getting problems that different architectures would not solve. Also, to make possible the integration of the devices with the human body, without being rejected by the tissues, materials with organic compatibilities must be considered.

The II-VI compound semiconductors such as Zinc Oxide have been proven important. ZnO is a wide direct-gap (3.37eV) semiconductor that has the wurtzite structure. Its significant applications include varistors, phosphors, surface acoustic wave transducers, and transparent conductors [8], and there are techniques to fabricate it in a way to make it flexible and transparent. [9-10].

All thing considered, the main goal of this work is to find out how extremely thin films made using semiconductors that are not Silicon can still be able to deliver high current levels, as one of the main requirements be a candidate to substitute the doped Silicon as a channel material in MOSFETs.

2. Literature Review

2.2. Compound Semiconductors

In the beginning, some factors limited the growth of compound semiconductors for commercial use and mass production, once these crystals are more difficult to grow than silicon, present a higher number of defects in the crystal, and higher fabrication costs. Compound semiconductors are usually more weak and fragile. Nowadays, however, the cost of fabricating compound semiconductors has decreased. It is still higher than silicon, but even though, the unique properties of these crystals have become more important for specific applications.

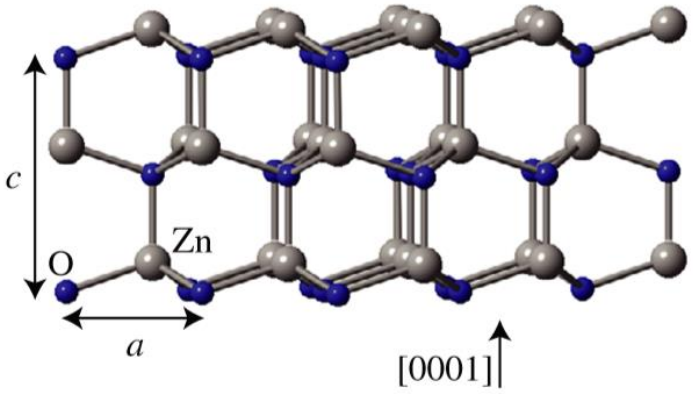
Compound semiconductors is a material made of at least two different elements. As a single element semiconductor, its conduction behavior is between an insulator and a conductor, depending on bias conditions. Most compound semiconductors are combinations of elements from Group III and Group V of the Periodic Table. Other compound semiconductors can also be fabricated from Groups II and VI. This is the case of Zinc Oxide, the semiconductor considered for this work [11].

2.2.1. Zinc Oxide

Currently, metal oxide semiconductor materials have become a crucial research topic because of their breadth in various sectors. ZnO, as an II-VI semiconductor, has the right conditions of ultraviolet and blue emissions due to its unique chemical and physical properties of a huge direct energy gap (around 3.37eV) and a considerable excite binding energy (60meV), which makes it advantageous over many other nanomaterials. [12]

The ZnO usually crystallizes in the wurtzite structure (Figure 4), the same as GaN, and ZnO is available as single bulk crystals. [12]

Figure 4 - Most common crystalline structure of ZnO



Adapted, A. Janotti, C.G. Van De Walle, 2009)

However, using ZnO as a semiconductor in electronic devices has been hampered by the lack of control of electrical conductivity: ZnO crystals are usually n-type, the cause of which has been widely used. Acceptor doping has remained a challenge for p-type, however, and the critical factor that would lead to producing typed and stable doping has not yet been identified. The availability of large single crystals is a significant advantage of ZnO. Epitaxy of ZnO films on native substrates may result in ZnO layers with a reduced concentration of extended defects and, consequently, better performance in electronic and photonic devices [12].

2.3. Nanofabrication Techniques

The fabrication of tiny semiconductor structures (nanometers) requires specific and precise manufacturing techniques for each step of the process. Besides, they require excellent particle flow control that may interfere with the process. Therefore, high purity class cleanrooms are required for the manufacture of high-quality, accurate semiconductor devices. The processes performed in this project were done in an ISO 6 cleanroom (the highest purity that still allows humans inside) in the Nanofabrication Core Lab at KAUST and are described in this section.

2.3.1. Chemical Vapor Deposition.

The Chemical Vapor Deposition (CVD) is a technique that involves chemical reactions in the creation of the material that makes up the film that is being deposited. CVD is used to deposit most dielectrics used in the semiconductor industry but also silicon (either in epitaxial or polysilicon form) and some metals. It is performed in furnaces, like oxidation and diffusion, and also, in more recently single wafer reactor, which enables more flexibility and control in the manufacturing process. This technique differs from others because the film is created by chemical reactions that occur on the wafer surface. It is not merely deposited like in other techniques, as Physical Vapor Deposition, for example, where there is no chemistry involved in the creation of the film. There are two types of CVD, described below.

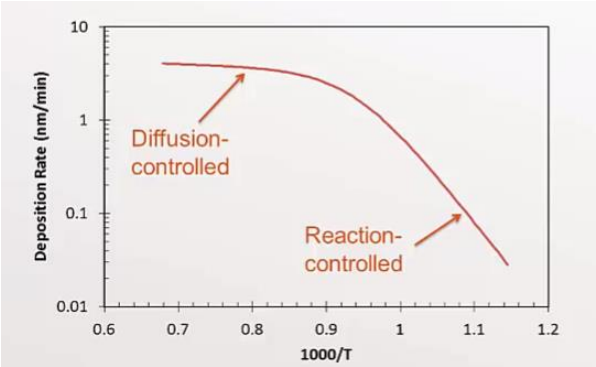
When the reaction for the film creation occurs in the gas phase, it is considered a homogeneous reaction, which means that both reactants are in the gas phase at the moment that they react to each other to create a solid that lands in the wafer surface. This approach is not preferred nowadays, due to poor uniformity and many particles that cause defects in the film. Another type of CVD, mostly used by the industry, is the solid-state reactions, a heterogeneous reaction that takes place on the wafer surface, forming the solid film needed. It shows a better quality in comparison to the previous one.

A simple CVD mechanism can be used to understand the CVD techniques easily. The first step is the transport of reactants to the wafer surface, known as a diffusion step of gas mass

transport operation. Then the reactants are adsorbed onto the surface, and the reaction occurs appropriately. After, the desorption and transport of by-products into the gas stream is required to finish the process.

Moreover, the CVD technique can be performed in two different regimes, the diffusion-controlled and the reaction controlled ones, and the knowledge of each has fundamental importance to figure out the right way to do CVD. At higher temperatures, the surface reaction rate gets very large, and the system is considered a diffusion-limited, making the deposition rate much more sensitive to the variations in the gas flow, and consequently controlled by the mass transfer coefficient. The opposite occurs at lower temperatures, where the deposition rate varies much more with the temperature, and we have a reaction-limited regime where the deposition rate is much more sensitive to temperature, as shown in Figure 5.

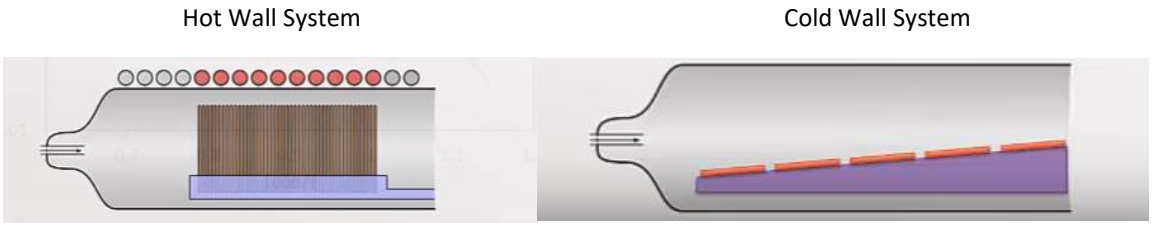
Figure 5 - Deposition Rate relation to the Temperature



(Adapted, Fabrication enginnering at the Micro and Nanoscale, Chapter 13, 4th Edition, Campbell)

In order to attend the requirements of each type of regime, different CVD chambers need to be designed. For a Reaction-Controlled regime, a Hot Wall System is preferred, with an exact control temperature and a weak control of the gas flow, allowing the deposition to occur everywhere inside the chamber. For a diffusion-controlled regime, a Cold Wall System is used, with a poor temperature control but a high gas flow precision. The cross-sections of the chambers can be seen in Figure 6.

Figure 6 - Cross section of the two types of furnace.



(a) (b)

(Adapted, Fabrication enginnering at the Micro and Nanoscale, Chapter 13, 4th Edition, Campbell)

However, some depositions process cannot tolerate high temperatures because some materials can melt of diffusive with the Silicon wafer, as the Aluminum. Then, a technique called Plasma-Enhanced CVD (PECVD) can be used. This technique deals with lower temperatures, but more energy is added to the reactants using RF plasma to compensate for the deposition rates [13].

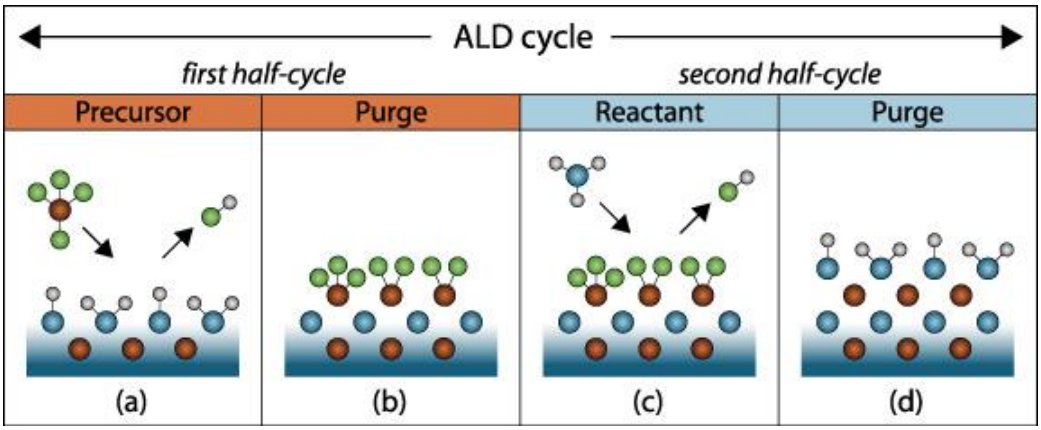
2.3.2. Atomic Layer Deposition.

The Atomic Layer Deposition (ALD) is considered a self-limiting CVD technique, which means that the reaction stops when a single monolayer is deposited, and has an atomic-level precision capable of generating extremely thin films. Miniaturization has produced very high aspect structures that need to be coated conformally, and no other thin film technique can approach the uniformity achieved by ALD on high aspect structures. The necessity for continuous and pinhole-free films onto microstructures substrates has driven the advancement of ALD [14].

Four main steps are involved in the deposition of any material by ALD technique. Each of these steps is needed to form a single atomic layer of the desired thin-film material, and these four steps are considered just one cycle of the whole process.

Two precursors are used, and they vary depending on the material. The first precursor is always thought so that it is chemically absorbed onto a silicon substrate, forming the first step of the cycle (Figure 7 (a)). When the surface is covered with the molecules of this first precursor, an external pump, with an inert gas flow, usually Argon (Figure 7 (b)), purges the residual gas. Next follows exposure of the substrate to a flow of the reactant, chosen so that it reacts with the material of the first gas. Then a monolayer of this second gas is deposited, and the reaction between the first and second gas occur due the high temperature and form the desired material of the thin film (Figure 7 (c)). The gases reactions byproducts of the second reaction are pumped away from de reactor again (Figure 7 (d)). This process is repeated as many times as required for depositing an aimed film thickness [13].

Figure 7 - Chemical reactions of one cycle for the atomic layer deposition process



Adapted from: Fabrication enginnering at the Micro and Nanoscale, Chapter 13, 4th Edition, Campbell

2.4 Thin Films Characterization Techniques

In wafer inspection, metrology, and quality control, it is vital to determine the exact characteristics of deposited thin films. There are several techniques to do this: since electrical, optical, and mechanical techniques, each one for specific cases. The most commom are the optical ones, which are used to measure thin film thickness because it is a non-invasive method, which leads to more trustable and precise results, and does not require patterns in the wafer for the measurement, for example, as some mechanical techniques require.

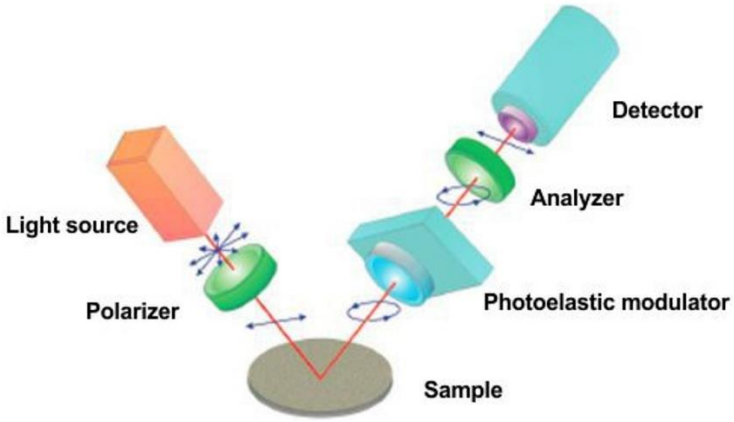
Furthermore, characterize the electrical properties that are equally essential to ensure the quality of semiconductor devices and their performance. In this section, we mention all used metrology and inspection techniques of the samples fabricated.

2.4.1 Spectroscopic Ellipsometer

Spectroscopic ellipsometry is a non-destructive, noncontact, and non-invasive optical technique, which is based on the change in the polarization state of light as it, is reflected obliquely from a thin film sample [15].

Here, the angle of light incident is inclined, which induces a polarization change after the reflection. The linear polarization of the incoming light is changed to elliptical polarization for the reflected light. The wavelengths can be varied between 190 nm and 2000 nm, which allows measuring film thickness from a few Angstroms up to 50 μm thickness. The tool also allows determining to some extent the composition roughness [16]. Figure 8 shows the scheme of an ellipsometer tool.

Figure 8 - Optical setup of the UVISEL serie.



(Adapted, HORIBA, 2019).

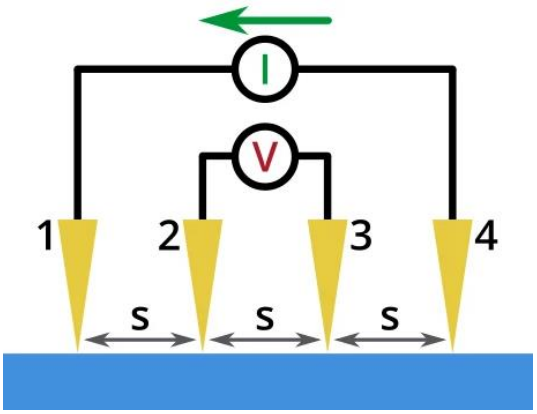
After the optical measurement, it is required the use of a software capable of using different reflection polarization results into a specific model of a specific material, and numerically calculate the thickness of the thin film.

2.4.2 Four-Point Probe

A four-point probe is a simple apparatus for measuring the resistivity of semiconductor samples. By passing a current through two outer probes and measuring the voltage through the inner probes allows the measurement of the substrate resistivity from its sheet resistance directly.

The working principle consists of four equally spaced metal probes (typically 1mm), which are part of a mechanical stage that goes up and down during the measurements. Two of the probes are connected to a high impedance current source, and a voltmeter connected to the other two measures the voltage across the inner two probes, as shown in the Figure 9 [17].

Figure 9 - Sheet resistance measurement method



(Adapted, Ossila, 2019).

Besides the resistivity, this instrument can give directly the sheet resistance obtained by the Equation 2, a crucial parameter, especially for thin films measurement.

$$R_S = \frac{\rho}{\tau} \tag{2}$$

As this measurement represents the resistance between the opposite sides of a square material, the most commonly used unit is ohms per square (Ω/□), in other words, the resistance of a given square of the sample, without any specific physical quantity. If one does not have the resistivity and thickness values, the sheet resistance can be calculated from the voltage and current measured in the sample, given by Equation 3.

$$R_S = \frac{\pi}{\ln(2)}\frac{\Delta V}{I} = 4.53236\frac{\Delta V}{I} \tag{3}$$

However, this equation is just valid if the material tested is no thicker than 40% of the distance between the probes and if the lateral size of the sample is large (full wafers, for example) [18]. An overestimation of sheet resistance can occur in small samples, because of the limitation that the edges of it in the current paths. Then, some geometric correction factors should be applied in order to compensate for it, depending on the size and format of the sample. The Equation 4 shows the correction factor of a circular sample, where *d* is the diameter of the sample and *s* the spacing between the probes [18].

$$C = \frac{\ln(2)}{\ln(2) + \ln\left(\frac{d^2}{s^2} + 3\right) - \ln\left(\frac{d^2}{s^2} - 3\right)} \tag{4}$$

2.4.3 Scanning electron microscopy

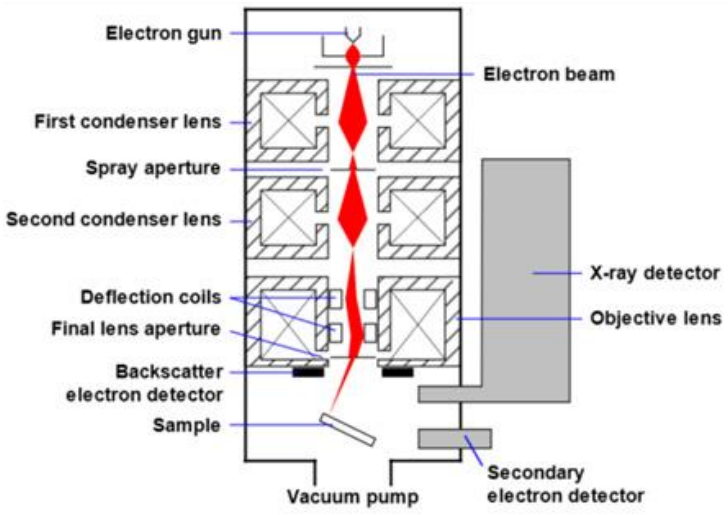
Scanning Electron Microscopy (SEM) is a powerful and versatile tool for material characterization. It is especially so in recent years, due to the continuous shrinking of the dimension of materials and devices in nanoelectronics, for example.

The technique consists basically of the observation of the shape of the surface and structure of a specific material. Electrons emitted backward elastically are backscattered when the incident beam collids with the specimen. BSE images have an atomic contrast and show the sample composition. Another technique called secondary electron form images with information with topographic contrast and is generally used to compose the overall image by observing the surface shape [19].

The main SEM components include a Source of electrons, column through which electrons travel with electromagnetic lenses, electron detector, sample chamber, computer, and

display to view the images. Electrons come from the generator at the top of the column, accelerated, and pass through several different lenses and apertures to produce an electron beam focused on the sample surface. The sample is placed in a vacuum chamber as the microscope is generally designed to operate at a low vacuum; a combination of pumps evacuates the column and chamber. Figure 10 shows the generic scheme of an SEM tool.

Figure 10 - SEM tool structure.



High-energy beam electrons interact with the sample, produce secondary electrons, backscattered electrons, and characteristic X-rays. These signals are picked up by one or more detectors to form images. When the electron beam reaches the sample surface, it penetrates the sample to a depth of a few microns, depending on the acceleration voltage and sample density [20].

3. Experimental Procedure and Materials

3.1. Details of the Equipments and Materials

The fabrication processes were performed in an ISO 6 Cleanroom, on the Nanofabrication Core Labs. Some metrology tools are also available inside the Cleanroom, as the four-point probe and the ellipsometer. The SEM images were obtained in the Image and Characterization Core Labs, both at KAUST.

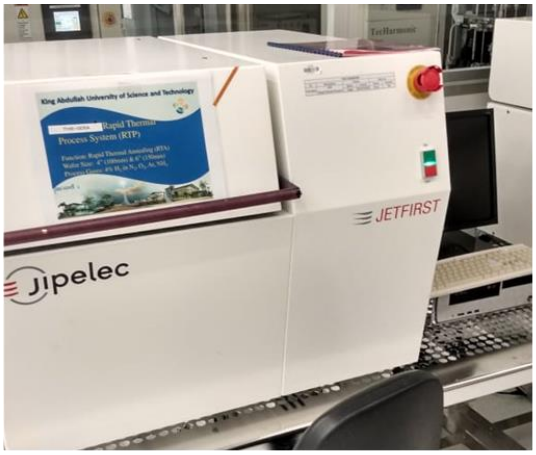
The base elements to begin the fabrication process are Silicon wafers. The Integrated Nanotechnology Laboratory provides 4-inch (100mm) wafers from WaferPro ©. For the first part of the work, the wafers were p-type, doped with Boron, fabricated by Czochralski epitaxial method, with a crystalline orientation <100> and a thickness of approximately 500 µm.

The PECVD tool (Figure 11 (a)), from Oxford Instruments, was used to deposit SiO_2 layers. The ALD tool (Figure 11 (b)) also from Oxford Instruments, was used to deposit ZnO, AZO. An annealing furnace from Jipelec, was used for future annealing steps (Figure 11 (c)).

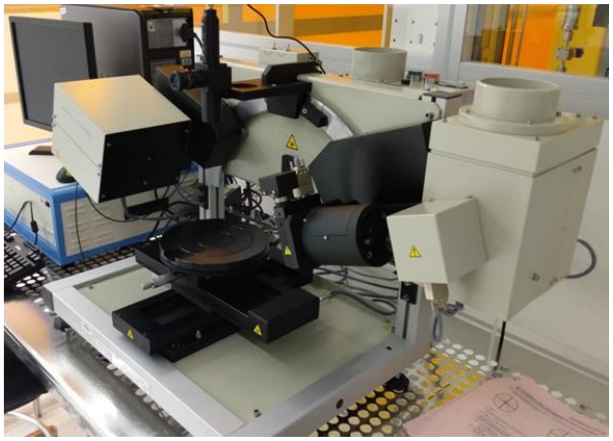
The UVISEL FUV spectroscopic ellipsometer (Figure 11 (d)) from HORIBA, was used to perform the optical measurements of the thin film thickness. The sheet resistance and resistivity measurements were performed using a 4-Point Probe (Figure 11 (e)), CMT-SR3000, Advanced Instrument Technology. To the obtainment of the cross-section images, a Spectrum Electron Microscopy were used.

Figura 11 - Equipment Used

(a) (b)



(c)



(d)

(e)

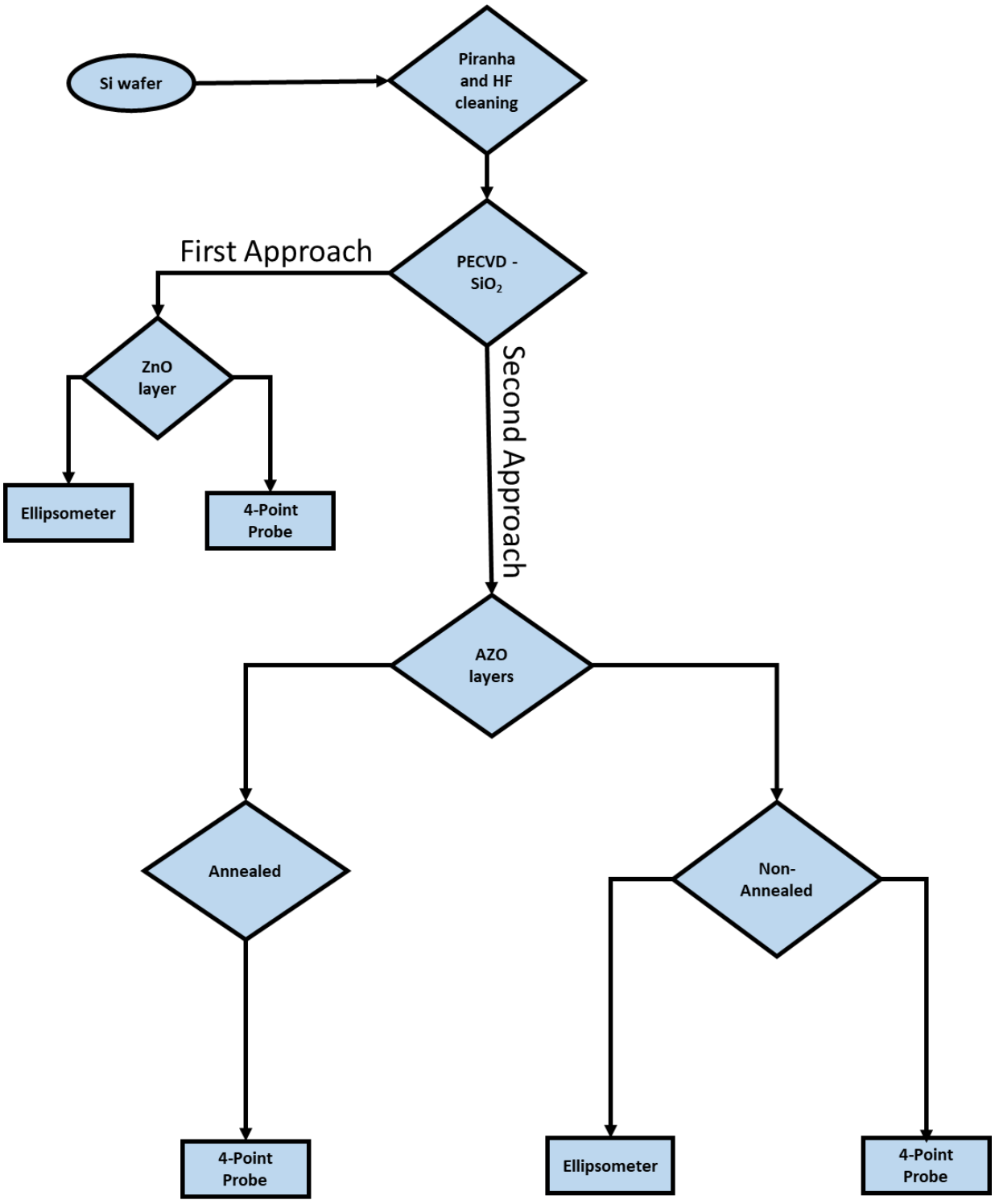
(Author)

3.2. Experimental procedure

The Bulk Silicon doped wafers were cleaned with Piranha solution and HF solution before being used for PECVD process. Then, the ALD performed the deposition of thin layers of ZnO, AZO and HfO_2.

The thickness of the thin films and the SiO_2 layers were measures using the Ellipsometer. Knowing the thickness, the sheet resistance were measured in the 4-Point Probe. The cross section were used to observe the thickness and also the grain growth in the thin layer. A process flow can be observed in the next page, in Figure 12.

Figura 12 - Block diagram of fabrication process



(Author)

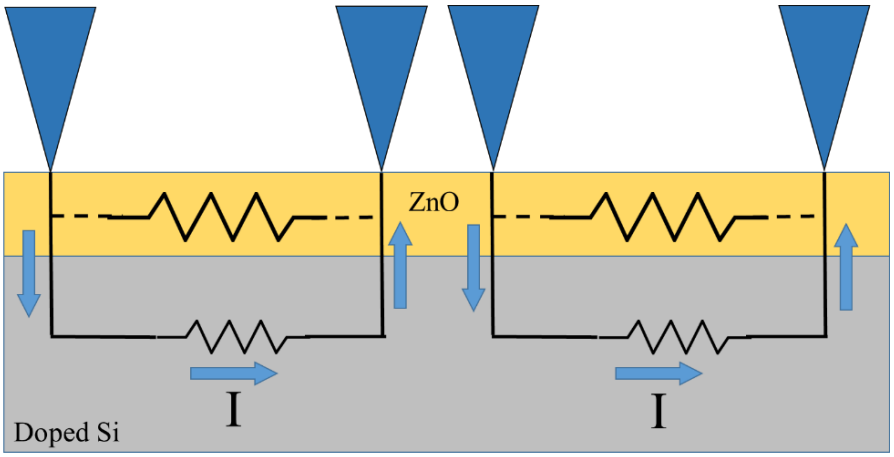
4. Results

In this section, the characteristics of the manufactured samples using the nanofabrication processes in the cleanroom will be presented, as well as material characteristics and electrical properties.

4.1. PECVD of SiO_2

The first part of the experimental procedure consisted in the isolation of the substrate to be possible the deposition of a Zinc Oxide film. This isolation step is needed because the doped silicon wafer presents a low resistivity (10-20 ohm.cm), which can form a parallel resistance with the Zinc Oxide films and disturb future measurements, as shown in Figure 13.

Figure 13 - Schematic parallel resistance without the SiO_2 layer.



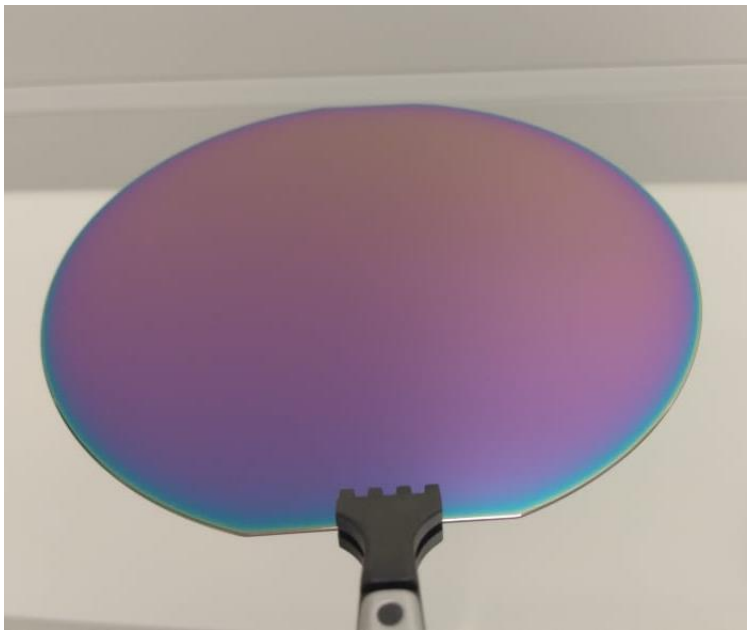
(Author)

Before performing the substrate isolation properly, the wafer need to be cleaned. A Piranha solution is required to remove any type of organic contaminants. The sample stayed immersed in a Piranha Solution, for 10 minutes and then cleaned with water in a 2 cycle drained bath. In addition, the silicon wafer can oxidize easily in contact with air, and an SiO_2 removal cleaning must be performed before every process, to ensure a better quality of it.

Silicon dioxide (SiO_2) was used as the insulator layer, and was grown by Plasma Enhanced Chemical Vapor Deposition (PECVD). Although it has a worse quality than other methods, such as Thermal Oxidation, it is a good insulator for this purpose and more accessible in the cleanroom than the other methods mentioned.

The process was performed at 300°C, for about 4.5 minutes, considering that the standard growth rate is 64nm/min. Figure 14 shows the wafer after the PECVD process. A difference in the color can be observed in the SiO_2 deposited wafer, due to the interference of the light reflected in the lower and upper boundaries of the SiO_2 film. The color is a function of its thickness.

Figura 14 - Wafer after the PECVD process



(Author)

The thickness was then measured with the spectroscopy ellipsometer, to ensure that the deposition rate estimated is right. As all the samples were fabricated in the same conditions, only the first three samples had the measurements taken for the thickness. We can observe that the thickness was approximately the same. The values are shown in Table 1.

Table 1 – Thickness measurement for SiO_2 layer

Sample	Thickness +/- Error (nm)
1	314.1759 +- 1.0169
2	320.1921 +- 2.9200
3	313.3764 +- 3.9878

(Author)

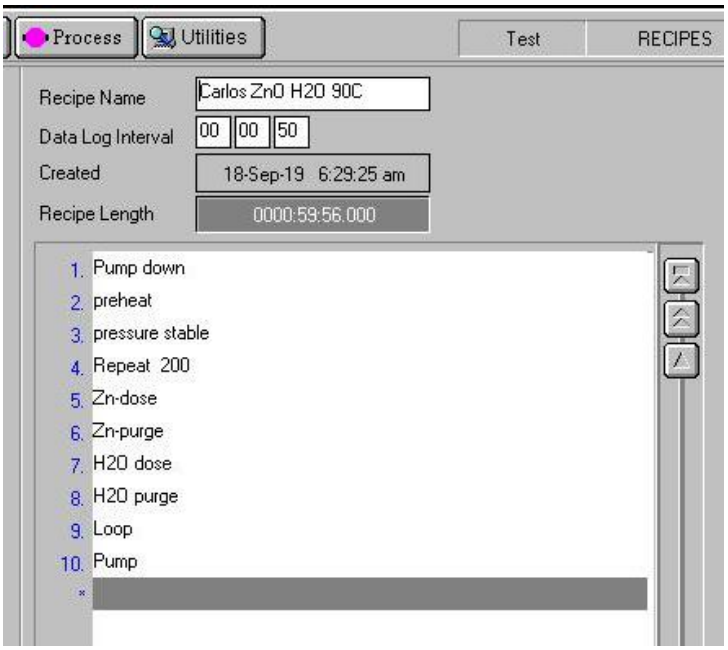
4.2. Recipe for ZnO as a transistor channel material

4.2.1. ALD of ZnO for different temperatures

The main fabrication part of the work is the Thermal Atomic Layer Deposition of Zinc Oxide thin film. The goal here was to find a good recipe for the ZnO, as it could be the channel material of a thin transistor, which means that the thin film must have the lowest sheet resistance possible, and a thickness of few nanometers. Two approaches were considered to the Zinc Oxide recipe.

In the first one, the recipe made in the ALD tool is described according to the procedure of Figure 15. The recipe was performed for four temperatures, 150°C, 110°C, 90°C and 80°C.

Figura 15 - ALD Recipe for ZnO deposition.



(Author)

The first step consisted of a pump-down to a pressure of 80mTorr, followed by a pre-heating to ensure that the wafer is at the same temperature required in the process and a setup pressure, this one to wait for the pressure stabilization, in the interior of the main chamber. Then, a repeat step is added to set the number of cycles required according to the thin film thickness desired. All the following steps between this repeat step and the loop steps were repeated by the number of times set in the recipe.

Then, the Diethylzinc (DEZ) was used as the precursor, and pumped inside the chamber for 30 ms, diethylzinc adsorbs and reacts rapidly on the surface to form monoethylzinc [21].

The by-products were then pumped away from the chamber with an Argon flow with a pressure of 250 mTorr. As it is a thermal ALD process, the reactant used was water (H_2O) vapour. The oxygen of water reacted with the Zn in the surface, forming the ZnO compound. Then, the by-products are again purged with the Argon flux away from the chamber. After repeating the desired number of cycles, the process stops, and the sample is transferred to the load lock to be withdrawn from the ALD machine. That is why a pumped up step is required. The screenshots of this first recipe can be found in Appendix I.

4.2.1.1 Thickness measurement and deposition rate estimation

The first metrology procedure required to evaluate the quality of the layers deposited was the thickness measurement. The model used for this measurement was ZnO.HYB, as shown in Figure 16. The results of this first part for thickness measurement can be observed in Figure 17.

Figura 16 - Model for ZnO thin film thickness

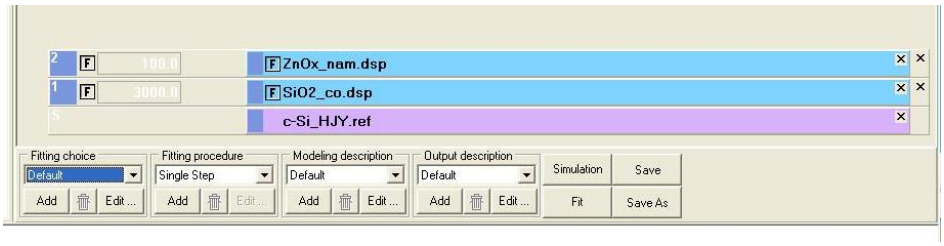


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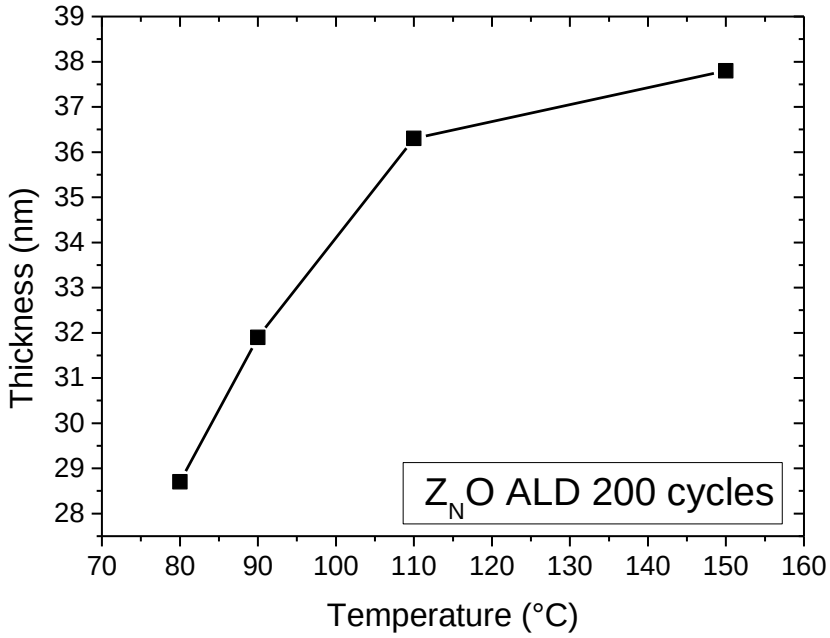
Figura 17 - Thickness variation as a function of the temperature.



(Author)

Through these results, we can estimate some parameters concerning the Atomic Layer deposition for Zinc Oxide. Firstly, it can be observed that for higher temperatures, the deposition rate per cycle is higher but less dependent on the temperature variation. The deposition rate obtained in this work is slightly smaller than the obtained in [22]. This variation can be explained due to the fact that lower temperatures induce the Wurtizite structure of ZnO, in which it is perpendicular to the wafer surface and denser than the (1 0 0) induced for higher temperatures. This makes it harder for the chemical reactions to occur in the surface, decreasing the rate and consequently the thickness for the same number of cycles [23]. However, the linear decrease of deposition rates suffers an abrupt fall for lower temperatures, in this case, most probably due to the decreasing reactivity of the precursor [22].

Table 2 – Summary of deposition rates and thickness for each temperature.

Temperature (°C)	Thickness (nm)	Deposition Rate (nm/cycle)	Temperature Rate (nm/°C)
80	28.7085±0.8506	0.1435	0.25
90	31.8788 ±0.7410	0.1594	
110	36.2901±0.7546	0.1814	
150	37.8018 ±2.4986	0.189	0.0375

(Author)

4.2.1.2. Sheet resistance analysis

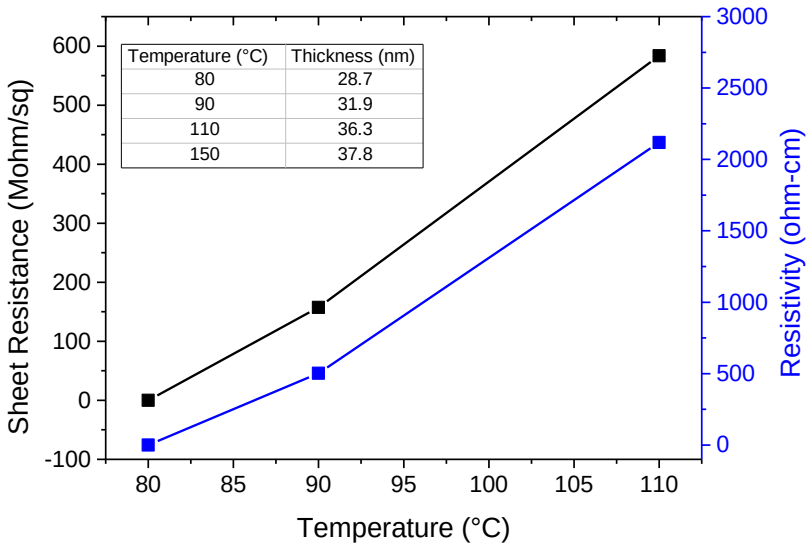
After knowing all the ZnO film thickness, the sheet resistance of these samples were verified using the Four-Point probe tool. For each sample, the measurement was performed in three different places of the wafer (Table 3), but the sample made with 150°C could not be measured because it was out the range of this tool. The average of the results was used to build the graph shown in Figure 18.

Table 3 – Sheet resistance in Ohm/Square.

Attempt	80°C	90°C	110°C	150°C
1	121K	175M	592M	Out of Range
2	150K	141M	588M	Out of Range
3	161K	157M	571M	Out of Range

(Author)

Figura 18 - Sheet resistance as a function of the temperature.



(Author)

As on can observe, the lowest values of sheet resistance were obtained for the sample fabricated at 80°C, besides it has the thinnest thickness. For the device to be fabricated usingin lower temperatures like this is required for devices to be later flexed or for transparent applications [9]. However, to perform the ALD process in low temperatures is very unusual, which makes the machines and chamber not wholly prepared for it, which can cause damages to the tool. In Core Labs, the lowest temperature admitted is 90°C. However, the responsible staff changed some internal parameters to allow the measurements at 80°C, even considering the risk of clogging the hoses that carry the gases inside the main chamber.

The resistivity values were then obtained through the Equation 2, for a better comparison with the reference, once the values of sheet resistance depend on the film's thickness, and can vary a lot from work to work. It is shown on Table 4 each sheet resistance value and the corresponding resistivity value for each temperature is also shown.

Table 4 - Summary of all the average sheet resistance and resistivity.

Temperature (°C)	Thickness (nm)	Average Sheet Resistance (Ω/□)	Resistivity (ohm-cm)
80	28.7085±0.8506	144000	0.41328
90	31.8788 ±0.7410	1.57433E8	502.21233
110	36.2901±0.7546	5.83533E8	2118.226
150	37.8018 ±2.4986	-	-

(Author)

The values of sheet resistance, as well as resistivity, may vary a lot depending on the process temperatures, not always respecting linear or direct relationship. Regardless this, Ref. [24] have reported values of resistivity going from 3.98 to 2460 ohm.cm for various temperatures, and Ref. [25] reported a resistivity of 5.84×10^4 ohm.cm for a 500°C process., much higher than the values obtained in this work. Also, considering an n-type silicon wafer, common resistivity values can go from few ohm.cm for a doping concentration of 1×10^{14}cm-3 to milliohms to a highly doped wafer (~1×10^{20} cm-3) according to [26].

4.2.2. ALD of Al_2O_3 doped ZnO for different temperatures.

The second approach considered an Aluminum Oxide doped Zinc Oxide thin film. As discussed in the literature review, ZnO is an n-type without the need for doping, but for extreme thin films, its sheet resistance is not small enough.

Considering all above, to dope a semiconductor with an oxide can be strange, but according to Eq. 5 ([27], Elmer, 2010) on adding group III oxides like Al_2O_3, Ga_2O_3 or In_2O_3

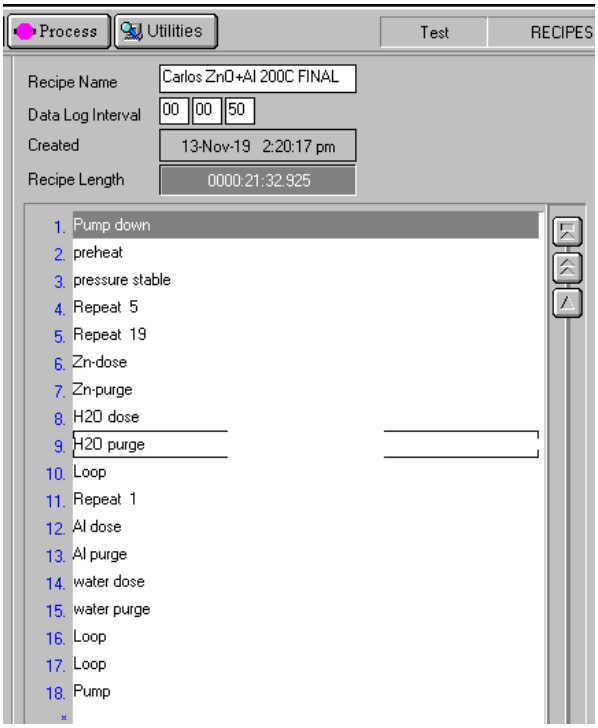
to Zinc Oxide, a third group dopant atom (Al, In, Ga) is released. These atoms have one valence electron more than Zinc, which means that they will act as a donor and built into a zinc lattice site. The additional electrons released during the process, according to Eq. 5 and not used for bonding, are delivered to the conduction band, and contribute to decrease the resistivity of the thin film. [27].

$$Al_2O_3 \rightarrow 2Al_{Zn} + 2e + \left(\frac{1}{2}\right)O_2 \quad (5)$$

The doping recipe considered was 19 of ZnO to 1 of Al_2O_3. The recipe procedure is shown in Figure 19, and all the parameters of the previous recipe were kept, except for the temperatures now were changed, so the chemical reactions for ZnO are the same as those of the last approach. For the aluminum layer, the only difference was the precursor used, the Trimethylaluminium (TMA) [28]. Other details, such as the screenshots of the recipe are available in Appendix II.

$$2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 6CH_4 \quad (6)$$

Figura 19 - ALD Recipe for Aluminum Oxide doped ZnO deposition



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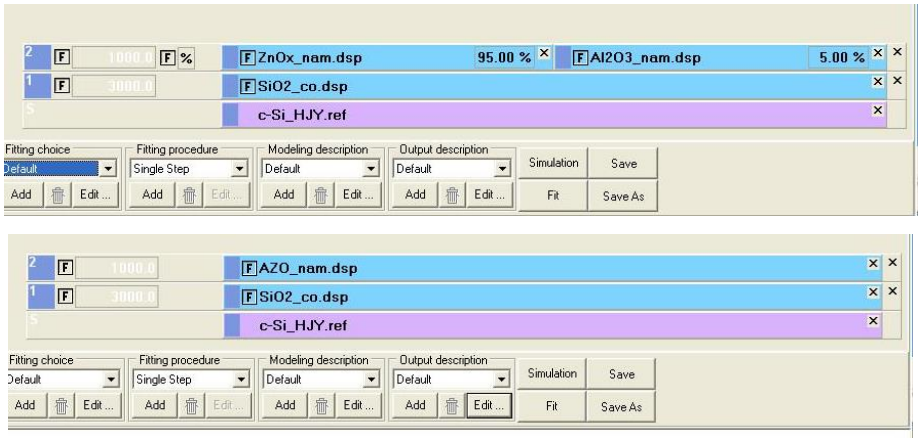
4.2.2.1 Thickness measurement and deposition rate estimation

The thickness measurement is the metrology procedure required to evaluate the quality of the layers deposited. Here, it was considered two different models: the first one consists of an AZO layer, and the second one a layer of 95% ZnO and 5% of Al2O3, respecting the

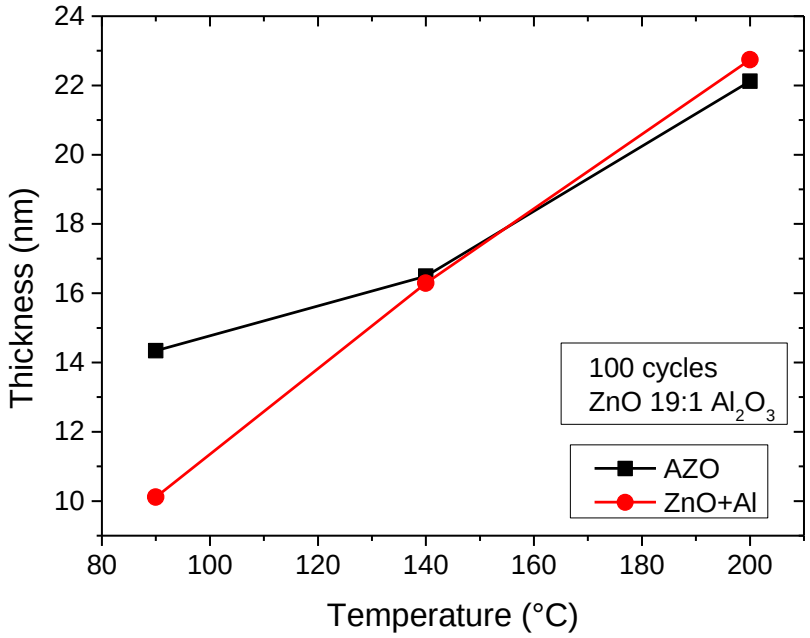
doping proportion, as shown in Figure 20. A plot of thr thickness as a function of the temperature for both models can be observed in the Figure 21.

Figura 20 - Models used for AZO film thickness measurement.



(Author)

Figura 21 - Thickness variation as a function of the temperature.



(Author)

As we can observe, the thicknesses measured are practically the same for the films deposited at 140°C and 200°C, but for 90°C the difference is more than 4 nm, what is significant for this scale. So, knowing that the second model considers the doping proportion between the two materials, it must be more trustable

In addition, as explained previously, the deposition rate has the same behavior as a function of the temperature. Considering that lower temperatures induce a denser crystallographic orientation than higher temperatures, which leads to smaller deposition rates [27]. Also, the deposition rate of Al_2O_3- layers once we have 4 of these layers in the film. Table 5 summarizes all the data obtained for the AZO films.

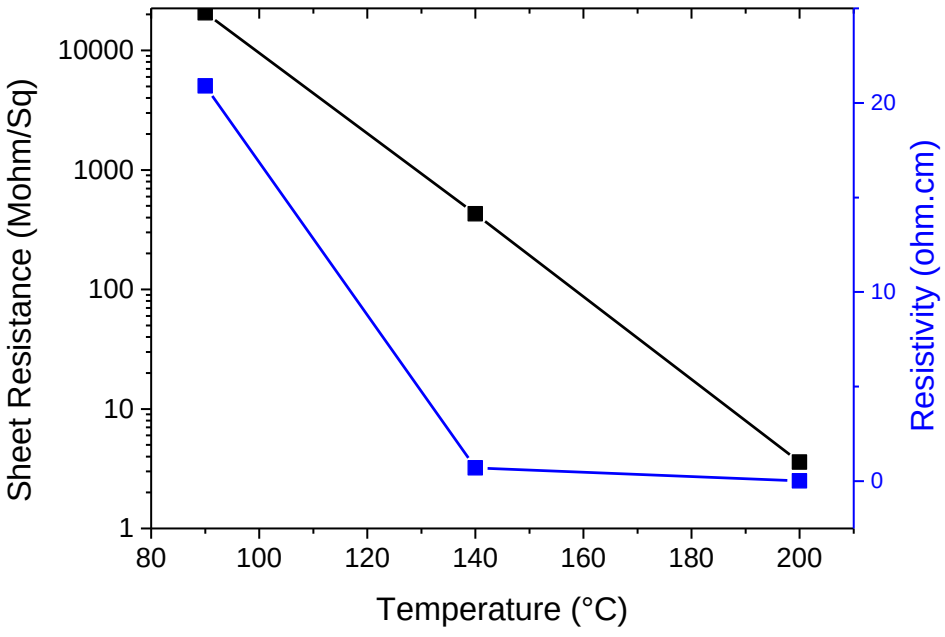
Table 5 - Summary of the data obtained, considering the $ZnO+Al_2O_3$ model.

Temperature (°C)	Thickness (nm)	Deposition Rate (nm/cycle)
90	10.1184 ±1.3246	0.1011
140	16.2901±1.0514	0.1629
200	22.7378 ±0.5441	0.227378

4.2.2.2. Sheet resistance analysis

The measurement for sheet resistance was performed in the exact same way as in the previous approach, for undoped ZnO. The results can be observed in Figure 22.

Figura 22 - Sheet resistance as a function of the temperature.



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The values of sheet resistance obtained with aluminum oxide doping are much smaller than the values obtained before, and it and also much smaller than Ref. [24-26]. These results prove that the doping aluminum oxide layers present a very good solution to a low resistivity ZnO based thin film, and it could be the right solution for the transistor channel's material.

Table 6: summary of the results obtained in though this approach

Temperature (°C)	Thickness (nm)	Average Sheet Resistance	Resistivity (ohm-cm)
90	10.1184 ±1.3246	2.07E+07	20.9
140	16.2901±1.0514	4.29E+05	0.6988
200	22.7378 ±0.5441	3.59E+03	8.39E-3

4.2.3. Annealed Al doped ZnO

Intending to improve the results obtained with the AZO recipe, an annealing procedure was performed. Annealing is a high-temperature furnace operation that can relieve stress in semiconductor, activate or move dopants, densify deposited or grown films, and repair implant damage in wafer processing. It can also change film to film or film to substrate interfaces for wafers with multiple films, bonded wafers, and SOI applications [29].

In order to have a recipe to anneal the AZO samples, [30] showed a very good one, which considers 200°C for 40 seconds.

4.2.3.1. Sheet resistance analysis

The sheet resistance measurement was again performed using the same Four Point Probe set up as the previous ones. However, unexpected results were obtained after annealing. The sheet resistance was so high that it could not be measured using the tool.

One of the reasons that could explain this effect is that the different methods used for doping in silicon are slightly different than the one used here. In the former, having the readymade silicon wafer and then, introducing the dopants. Nevertheless, here, the ZnO layer is fabricated along with the dopants, so in thesis, we should not need a step to activate the dopants because the crystal lattice was not broken [31].

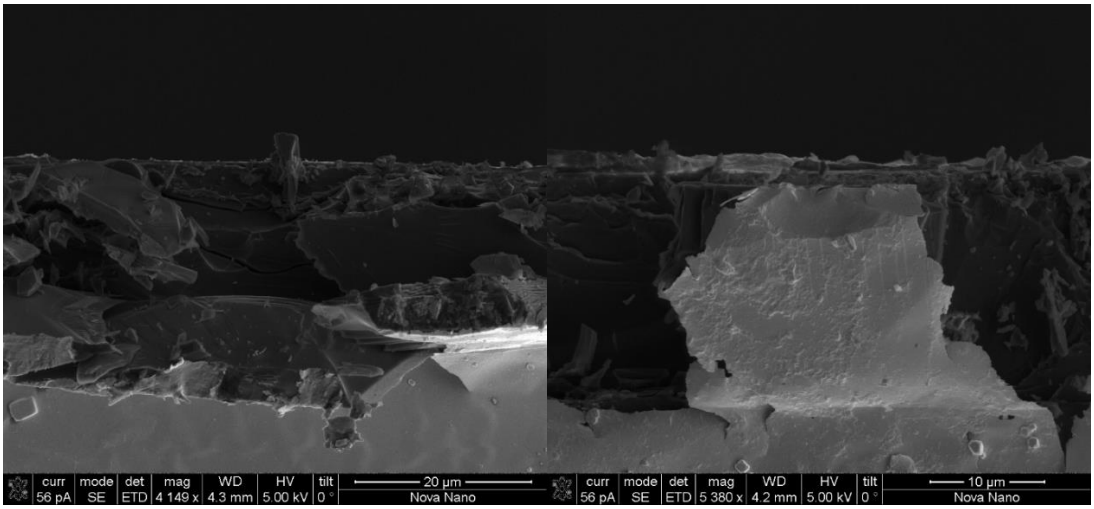
Also, because the AZO film was performed in air, more oxygen absorption on films surface at the grain boundary.These grain sizes decreased and the distance between two neighboring grain boundaries decreased that resulted in the higher resistivity. This oxygen atoms in the surface of a the film act like traps to the electrons, and it increases significantly the resistivity of the film.

4.4. SEM Images

The last step of this work was trying to effectively see the cross-section of the fabricated thin films of Aluminum-doped zinc oxide. Two samples of AZO 19:1 recipe at 200°C were prepared to obtain the SEM images. The first one, a sputtering step of aluminum were used to

enable and improve the imaging of samples. Creating a conductive layer of metal on the sample inhibits charging, reduces thermal damage and improves the secondary electron signal required for topographic examination in the SEM. In the second one, however, no aluminum coating was deposited on the top. The method used to cut the wafers and obtain the cross-sections was straightforward, using a diamond pen and cutting it with the force of two fingers. Nonetheless, as it can be observed in Figure 23, the coated sample has a cracked cross-section, what hindered a good visualization.

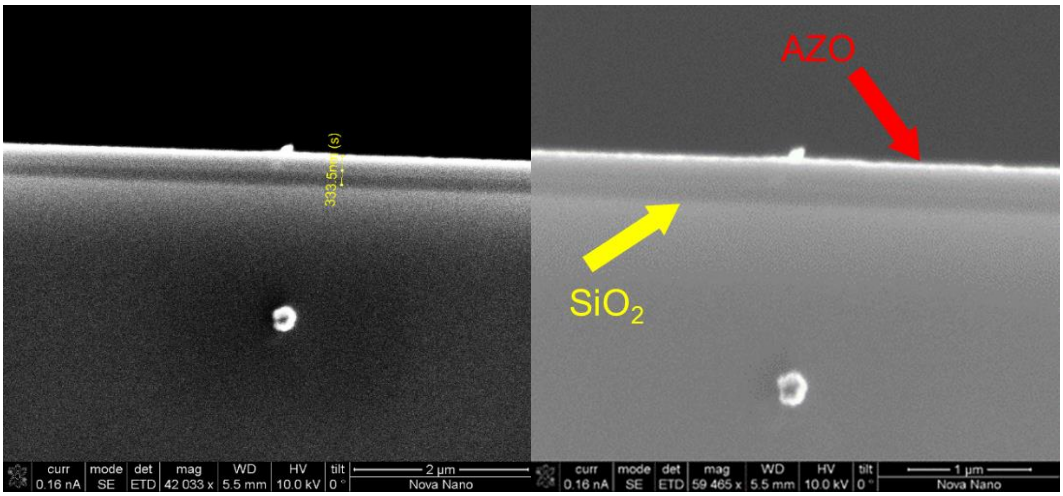
Figura 23 - SEM images of the aluminum-coated cracked cross-section.



(Author)

Nonetheless, the second sample coated with aluminum had a flatter cross-section, but the images were not as bright as in the first one. Regardless of this, as we can see in Figure 24, it is possible to observe a darker layer, which is the SiO_2 deposited by PECVD, to isolate the substrate. On the top, the white layer is the AZO one, because the aluminum is reflecting the ions bombarded by the ion beam. Unfortunately, this was the maximum resolution available on this SEM machine, and it was not possible to see the details of the AZO film.

Figura 24 - SEM images of the flat and uncoated cross section.



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6. Conclusion

In this work, II-VI semiconductor were presented as an alternative channel material compatible with Metal Oxide Semiconductor technology. Nanofabrication of undoped and doped Zinc Oxide thin films were performed to different conditions. Important parameters such as, film thickness, deposition rate, sheet resistance and resistivity, crystallographic orientation were analyzed in order to investigate the quality and electrical performance of the manufactured films.

The recipes for undoped Zinc Oxide thin films performed using the Thermal Atomic Layer Deposition method showed a thickness directctly related to the temperature for 100 cycles, as well as a larger variation in the deposition rate for temperatures lower than 110°C (0.25 nm/°C) than for the range of 110°C to 150°C (0.0357nm/°C). The best sheet resistance values obtained for this recipe were observed for the lower temperatures, even performing this process in low temperatures.

Aluminum Oxide doped Zinc Oxide solution were presented in order to enhance the sheet resistance on ZnO thin film. The best recipe, which presented the lowest resistivity value ($8.39x10^{-3}$ ohm.cm), was performed at 200°C. The other temperatures also presented good values of resistivity in comparison with the undoped ZnO recipes.

An annealing step were performed at 200°C on air for 40s were performed aiming to decrease the resistivity to even lower values. However the values of sheet resistance as well as resistivity increased a lot, due to the traps caused by the O_2 atoms in the surface of the material.

In conclusion, the ZnO thin film is shown as a good channel material if the ALD is performed at low temperatures (80°C). AZO 19:1 thin film presented even lower resistivity at 200°C and can be considered a better candidate for channel transistors with the dimensions of few nanometers.

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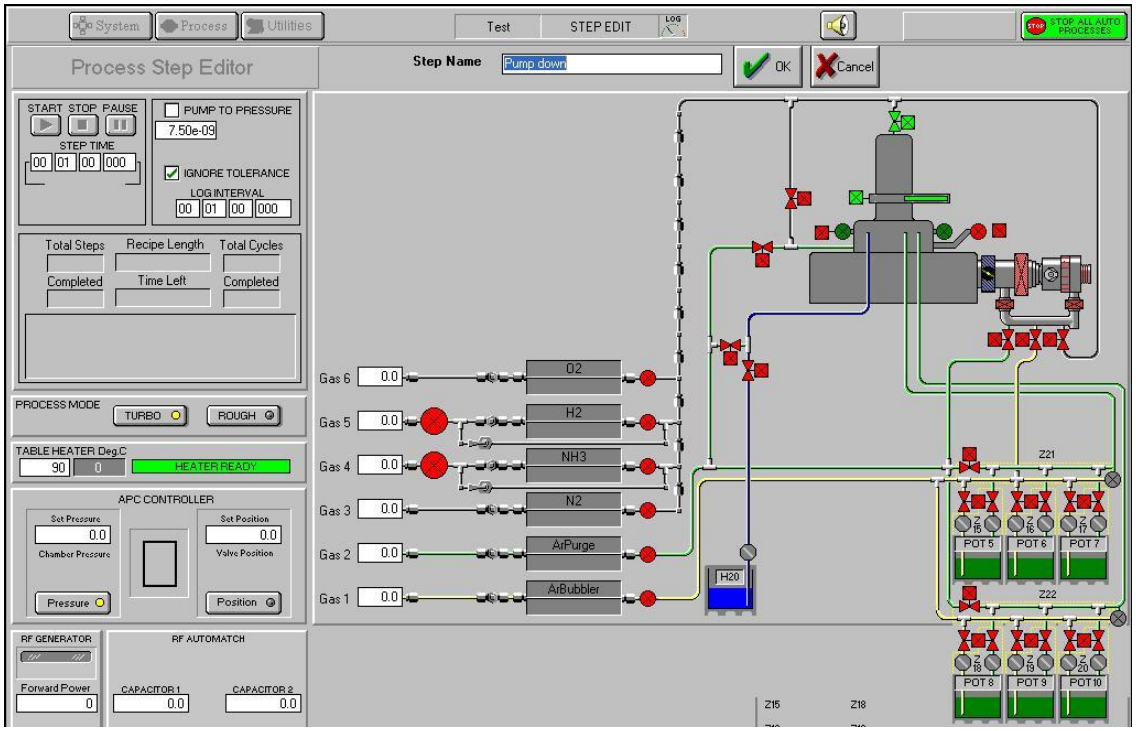
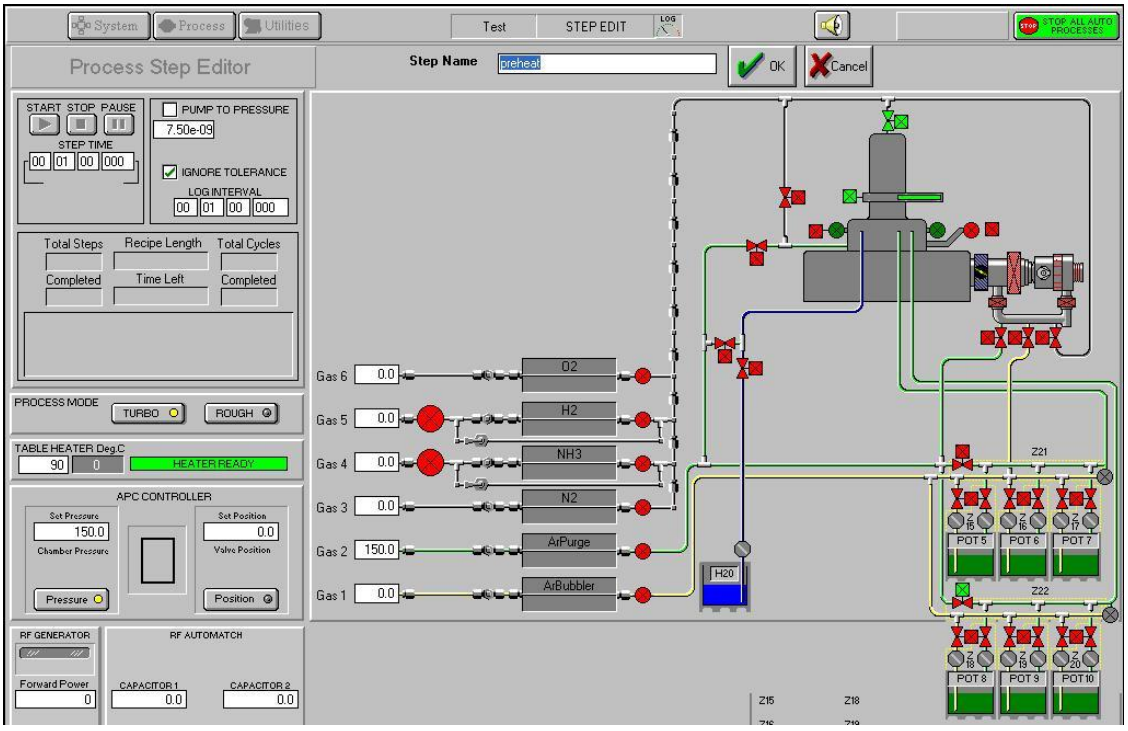
Appendix I – Steps of ZnO recipe

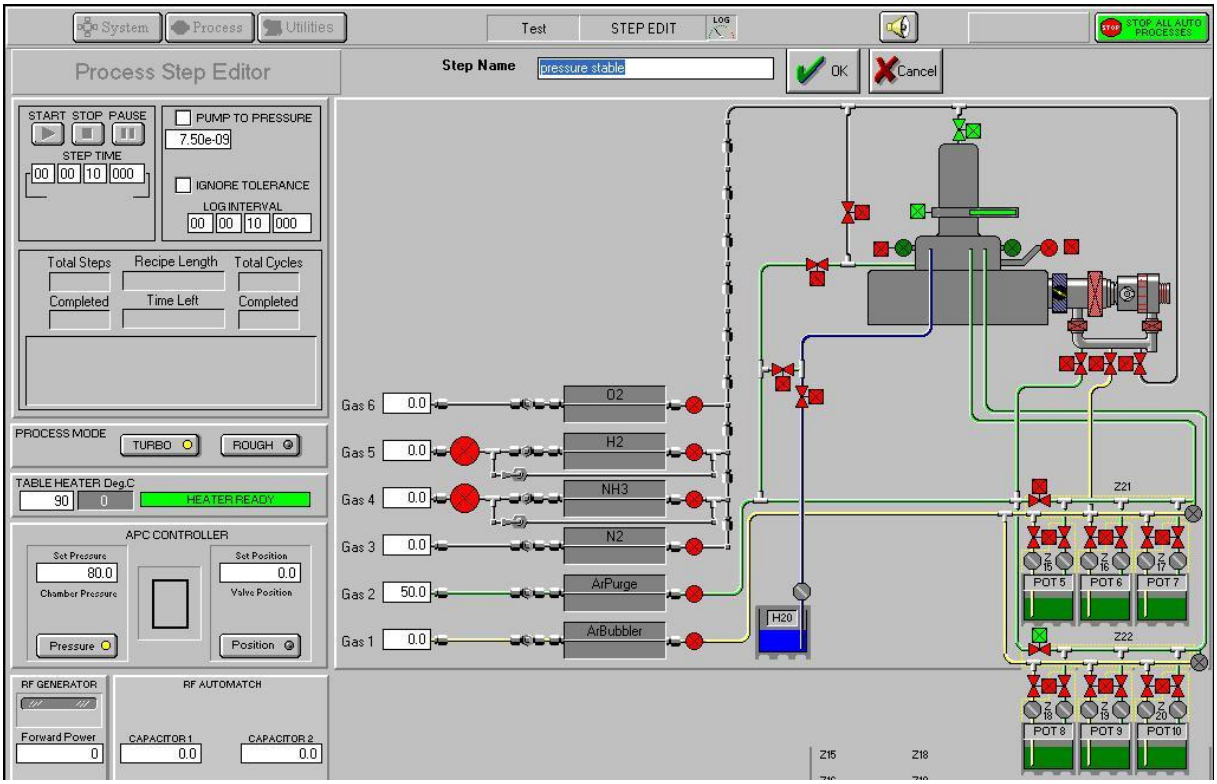
Step 1 – Pump Down



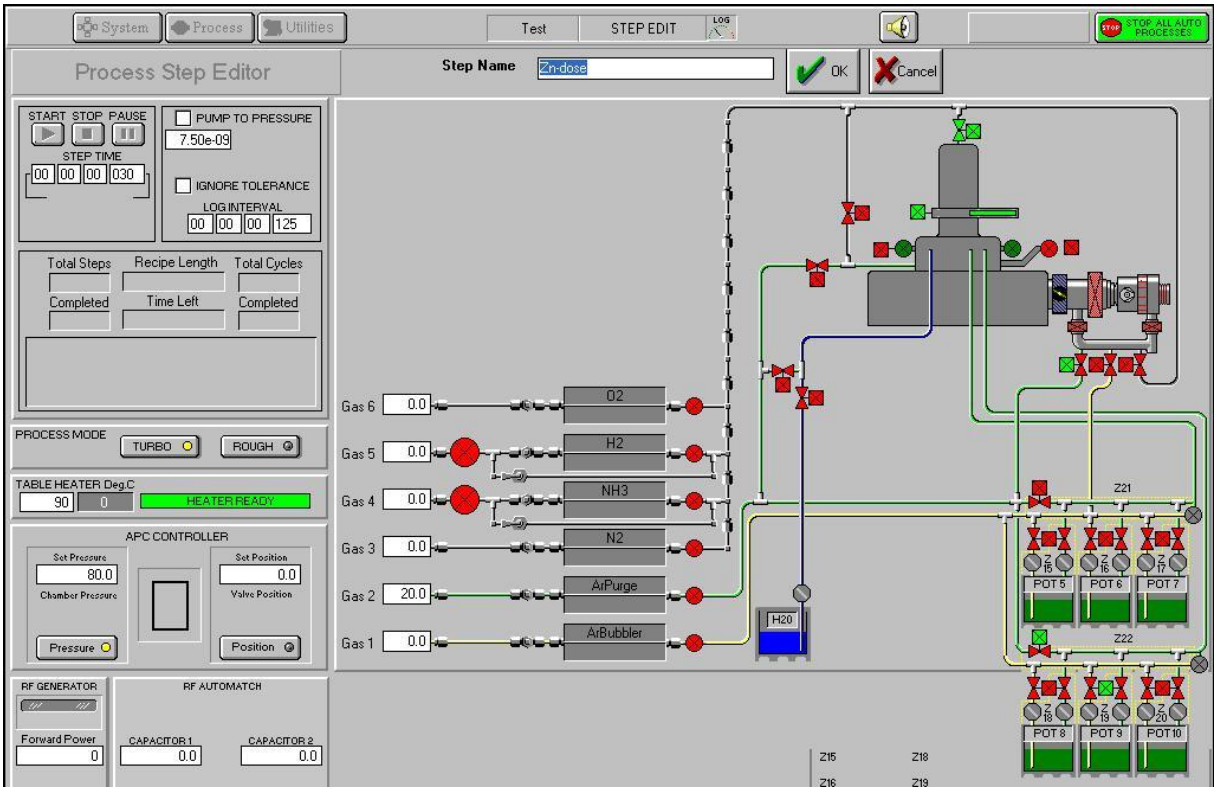
Step 2 – Pre heating



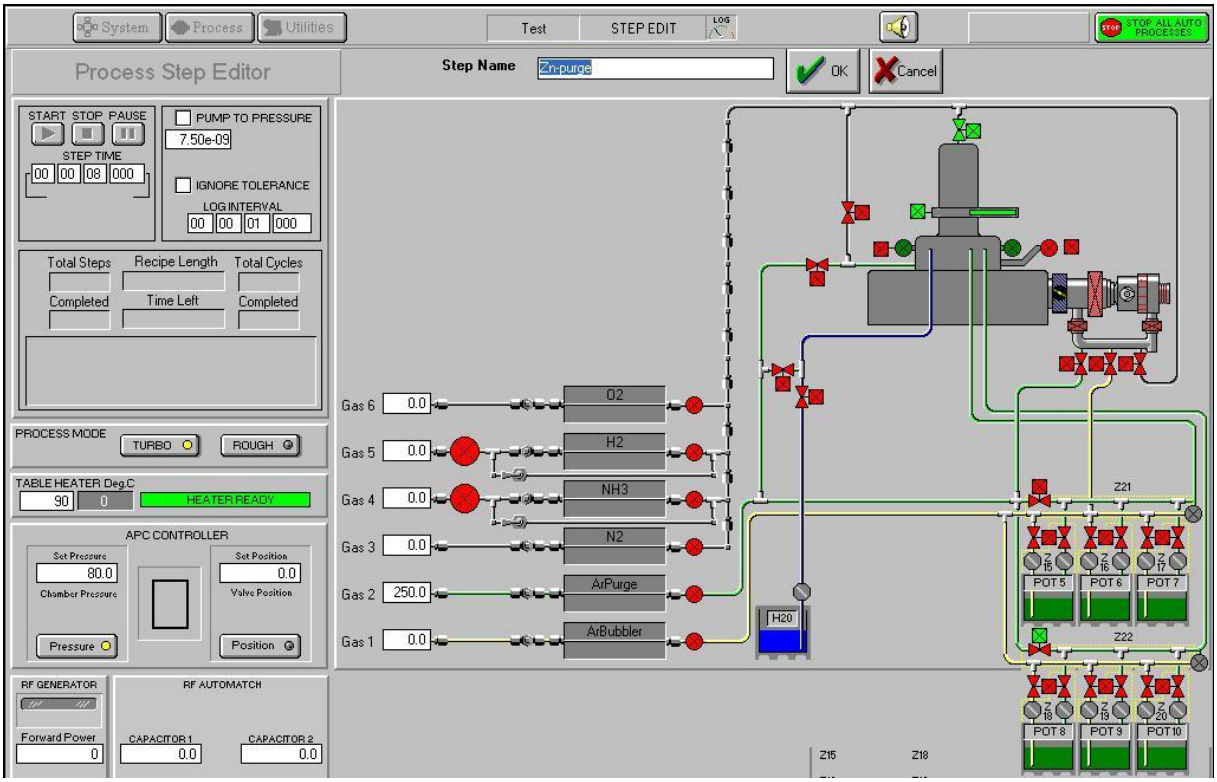
Step 3 – Preassure Stable



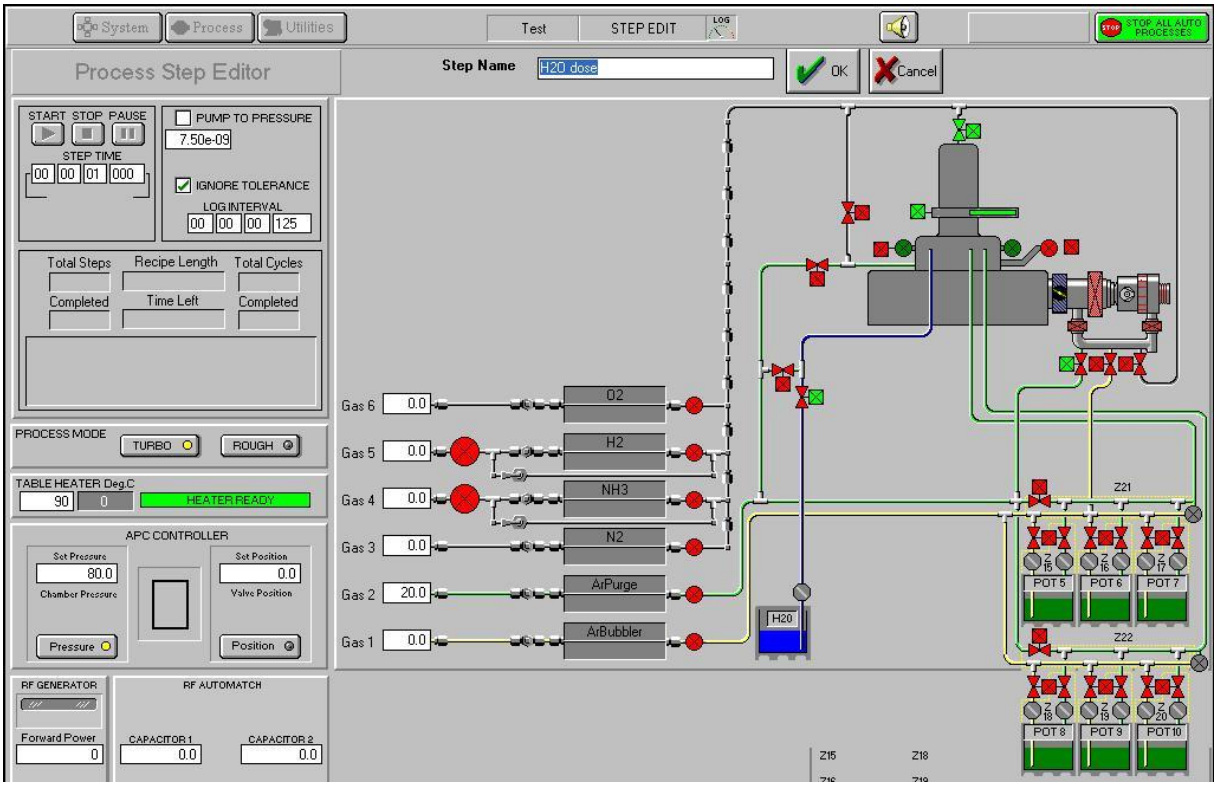
Step 4 – Zn Dose



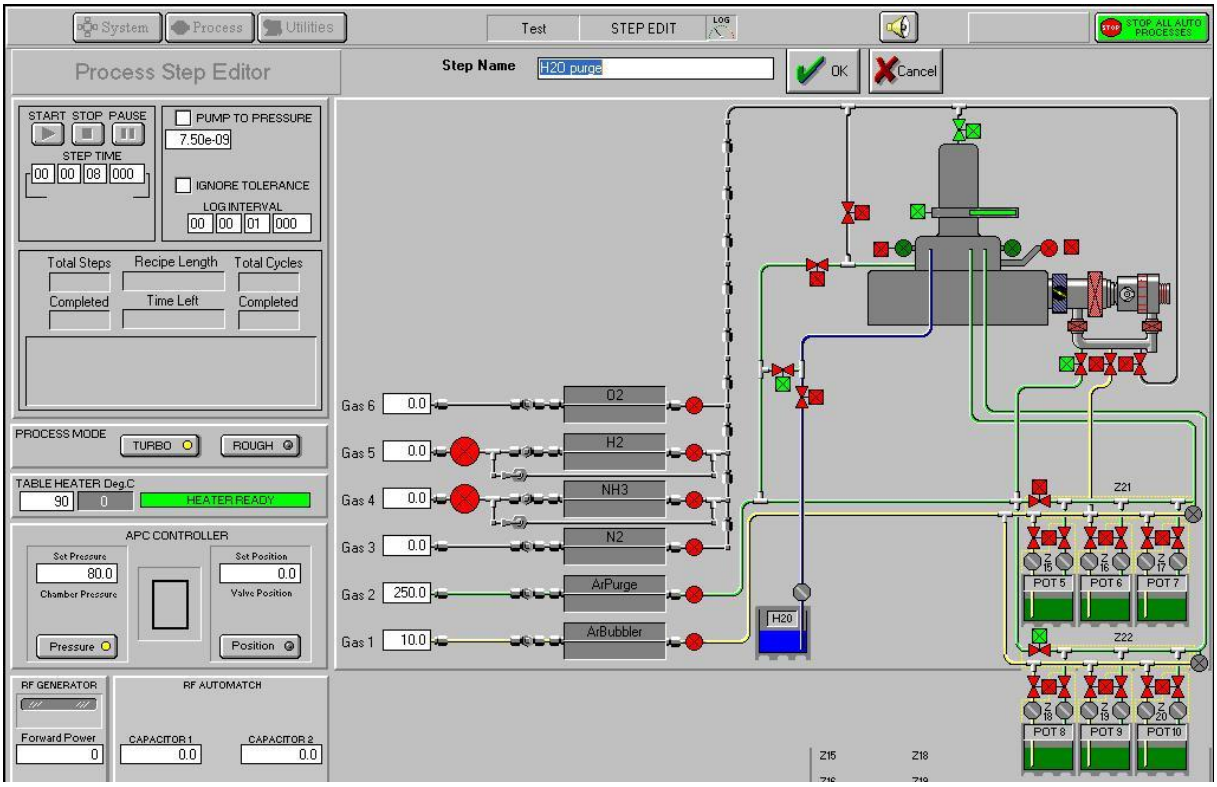
Step 5 – Zn Purge



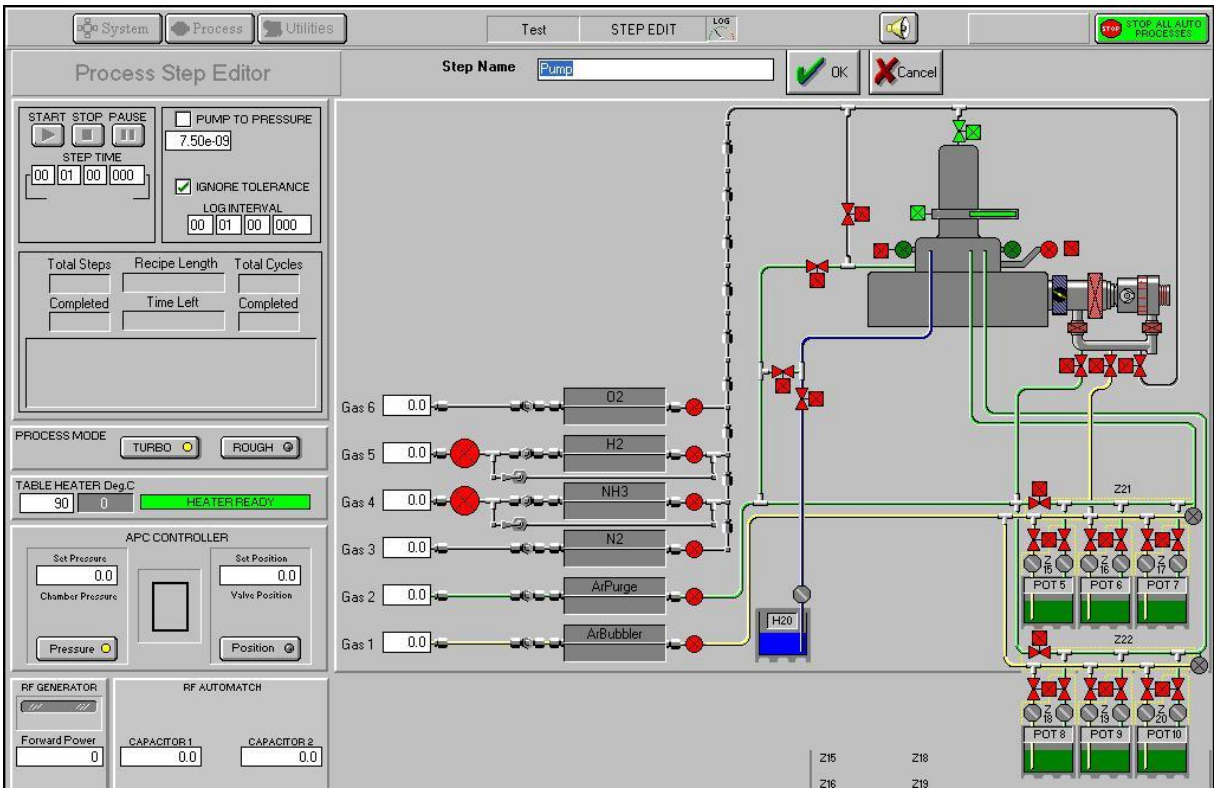
Step 6 – Water Dose



Step 7 – Water Purge

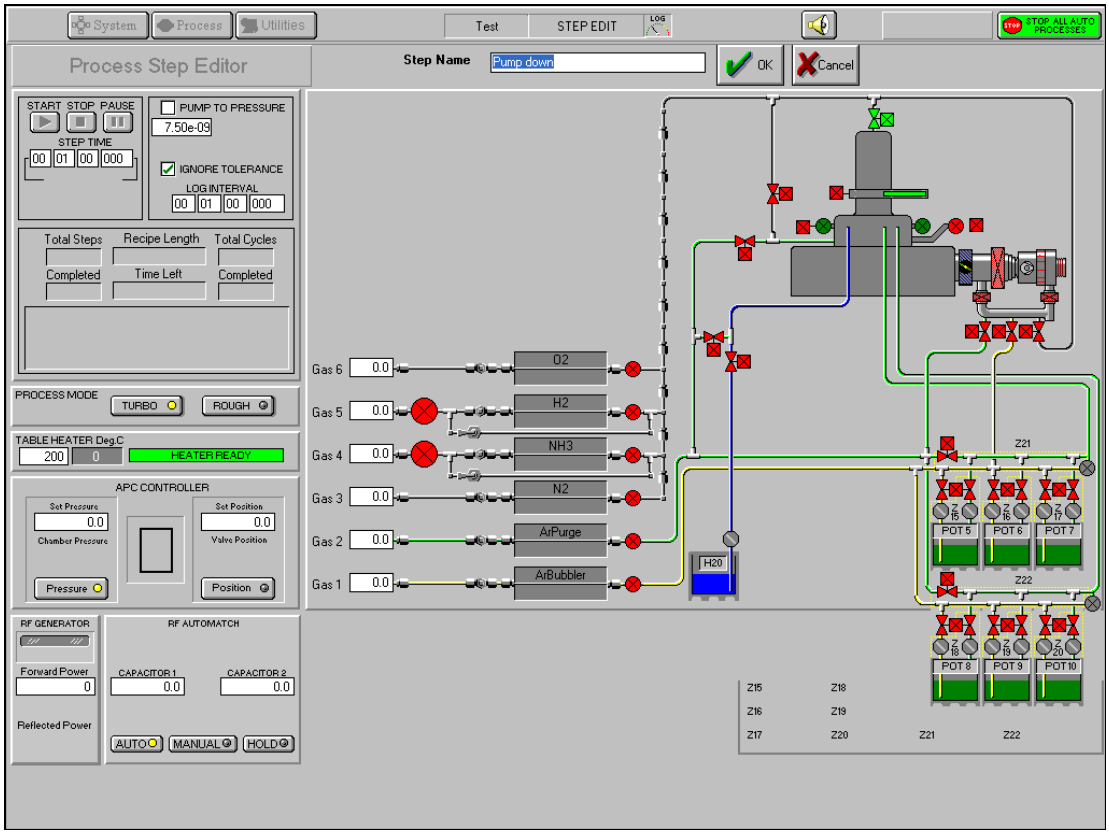


Step 8 – Pump Up

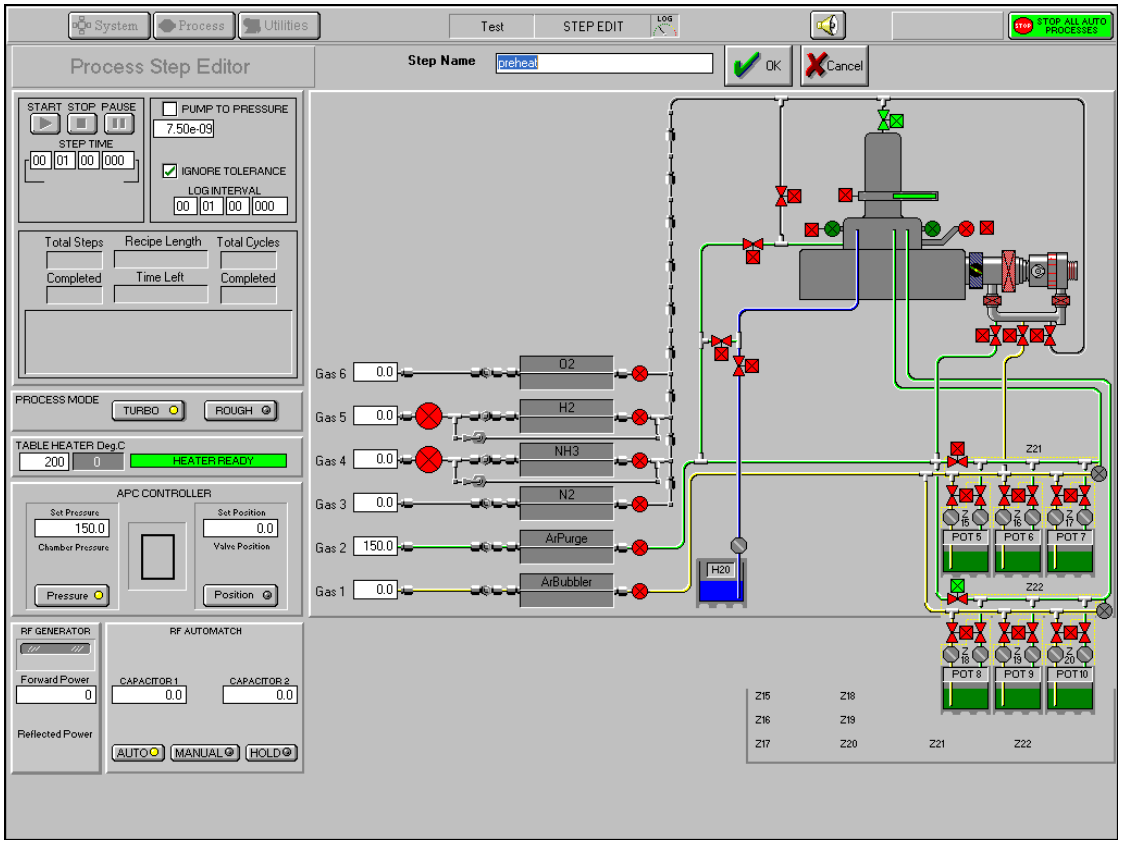


Appendix II - Steps of AZO recipe

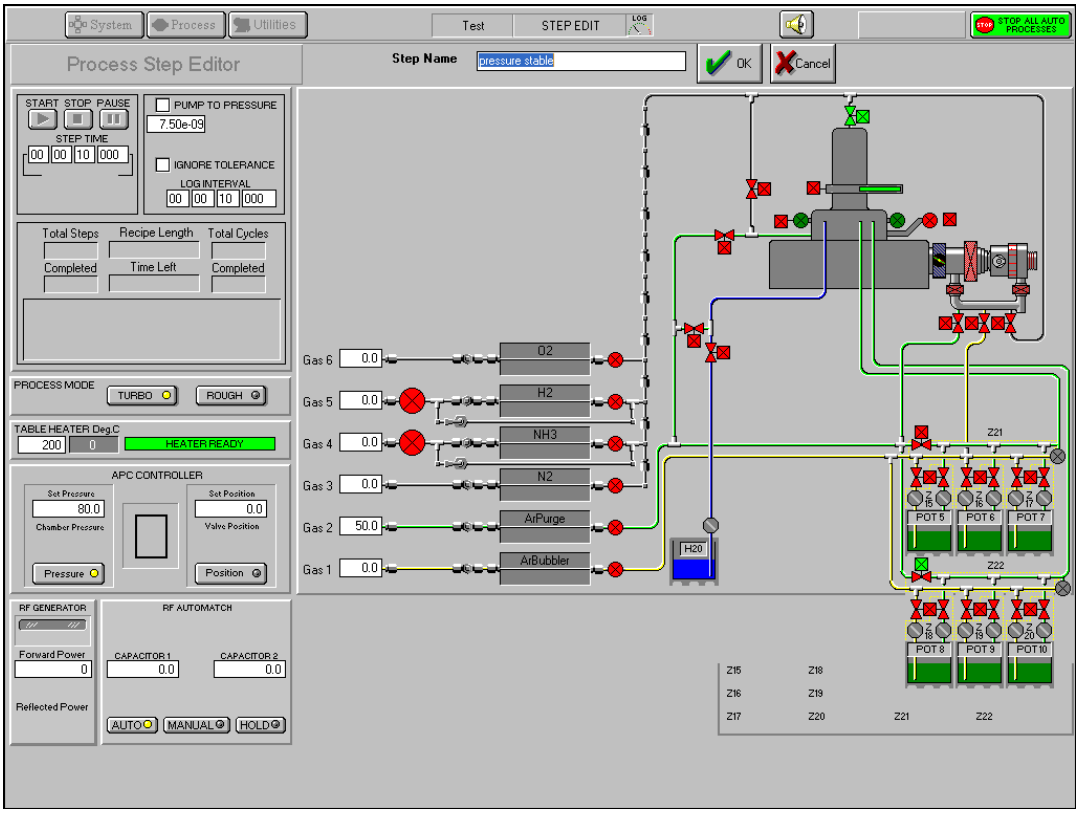
Step 1 – Pump Down



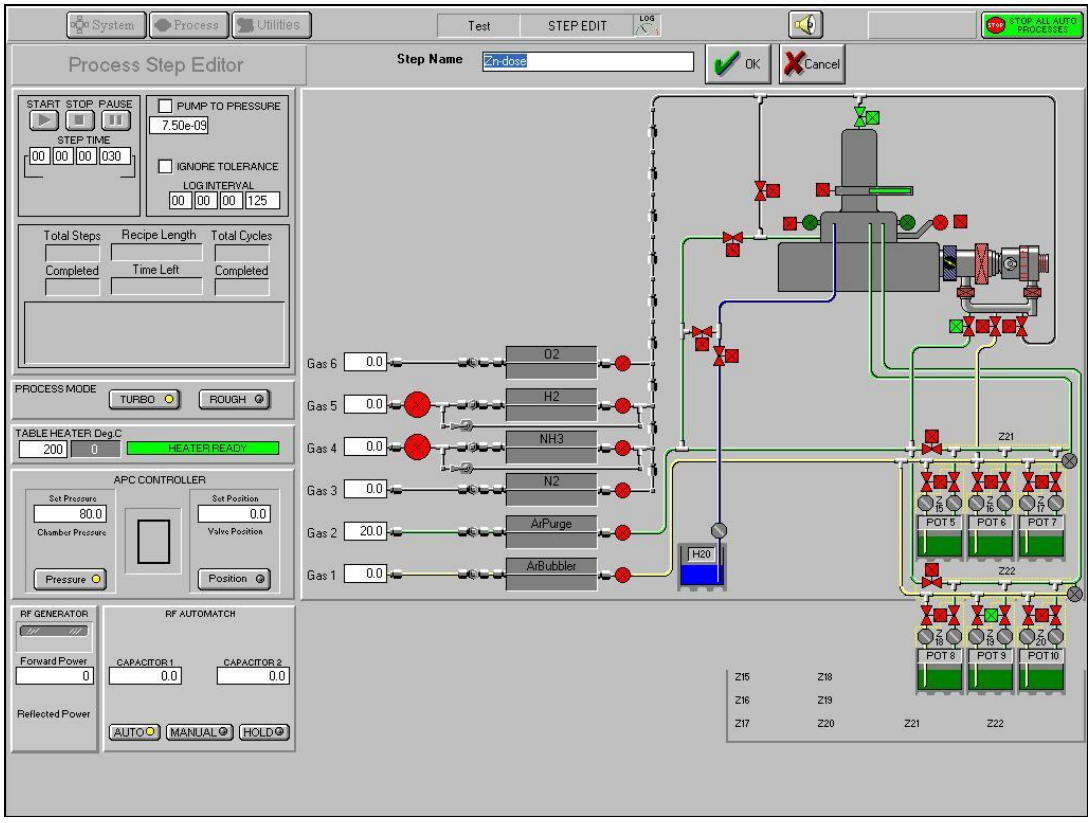
Step 2 – Pre heating



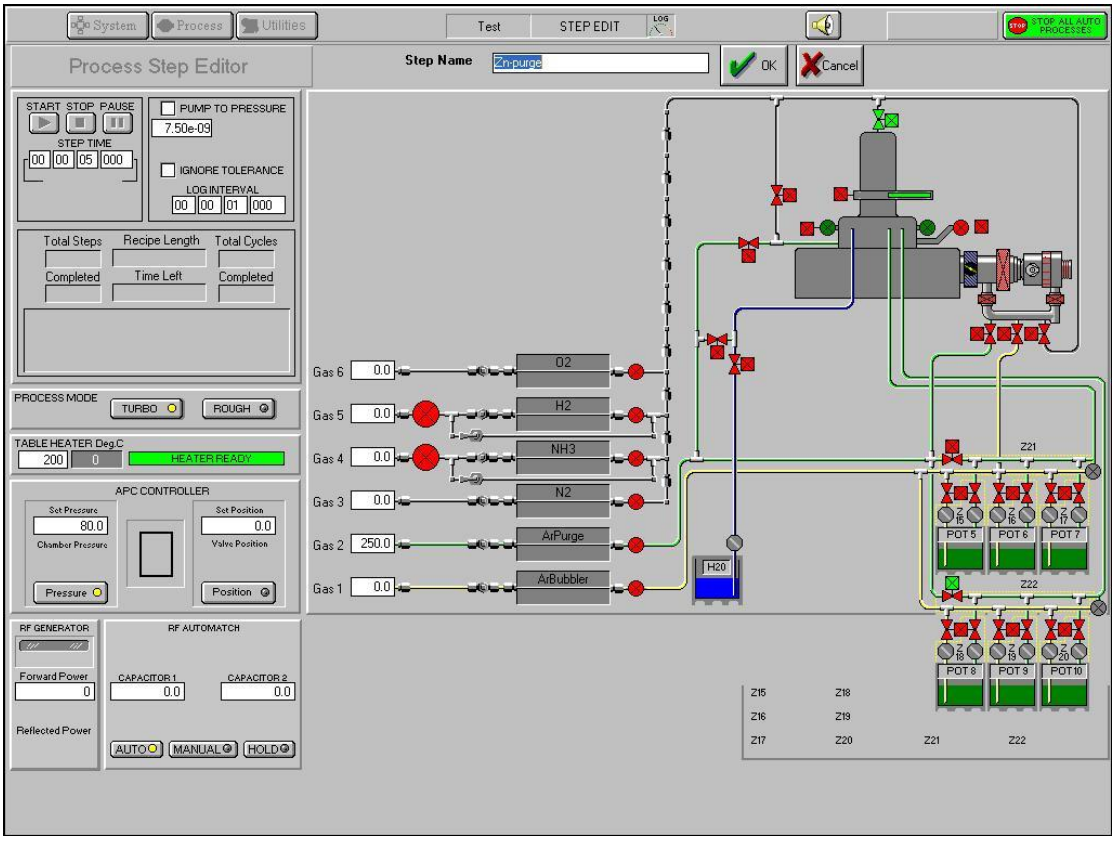
Step 3 – Pressure Stable



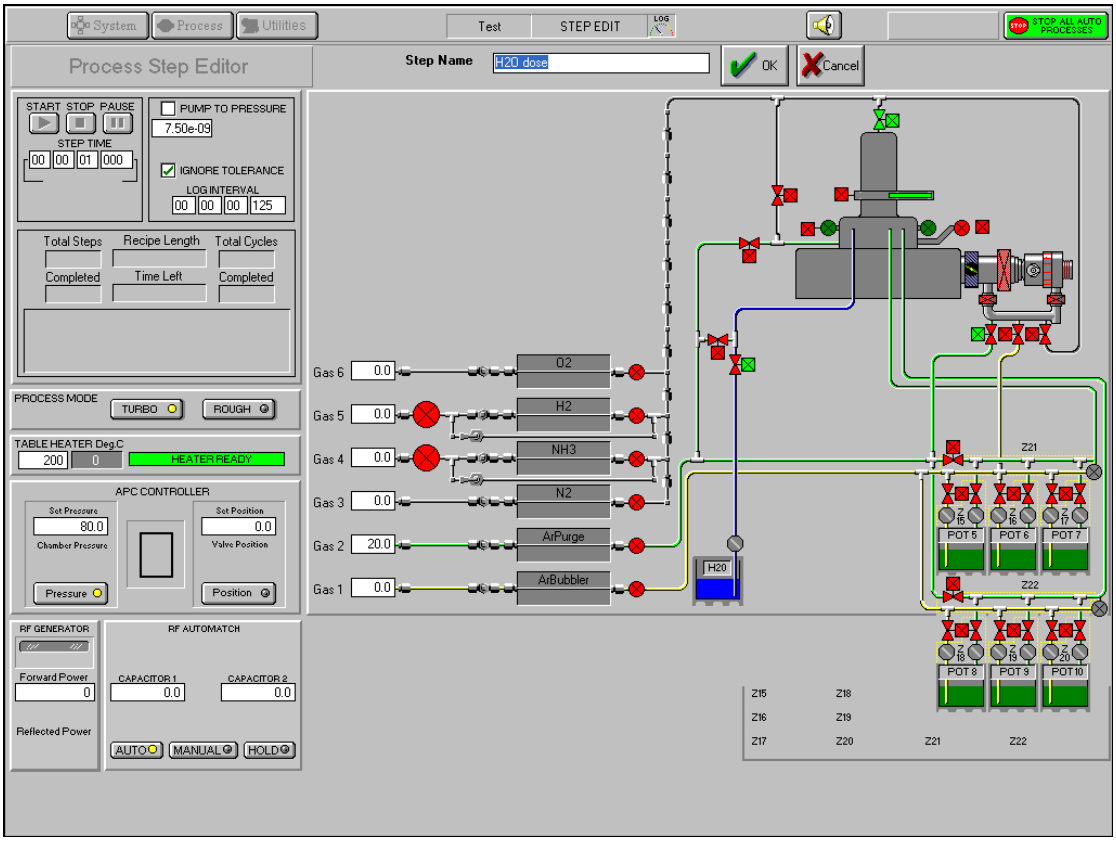
Step 4 – Zn Dose



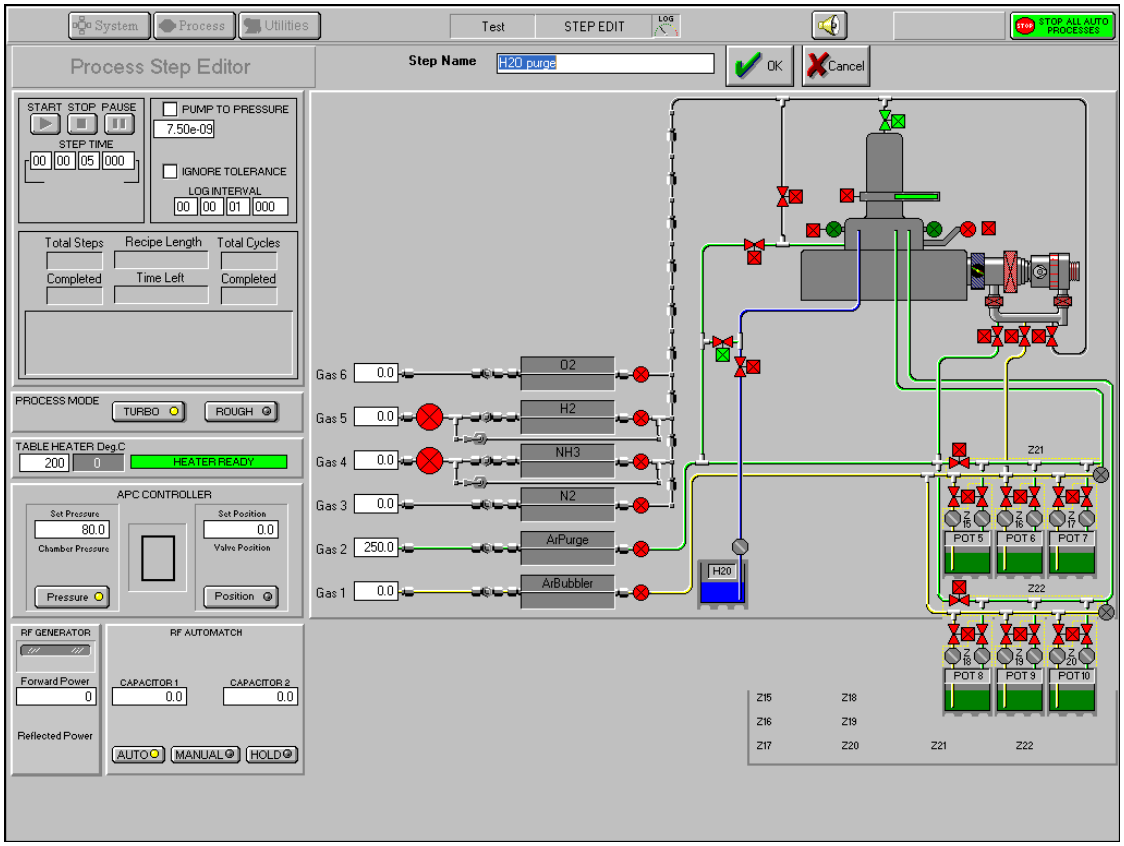
Step 5 – Zn Purge



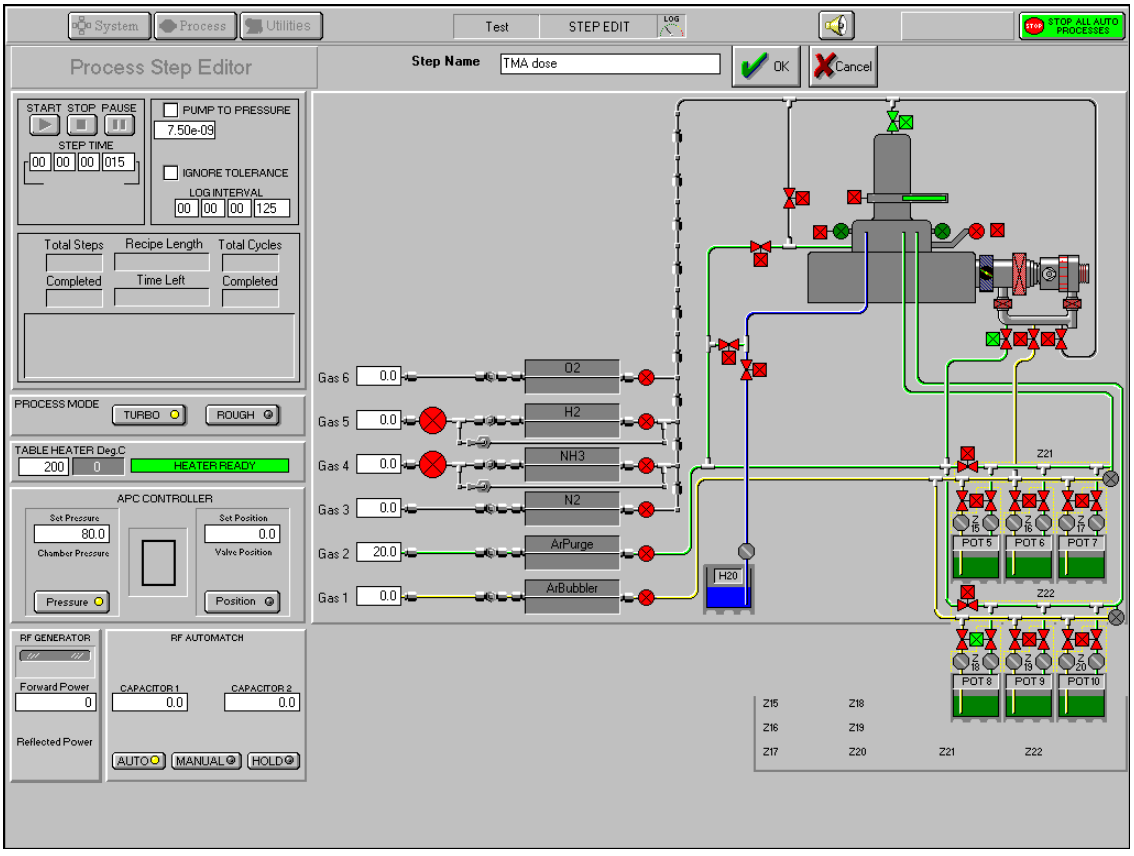
Step 6 – Water Dose



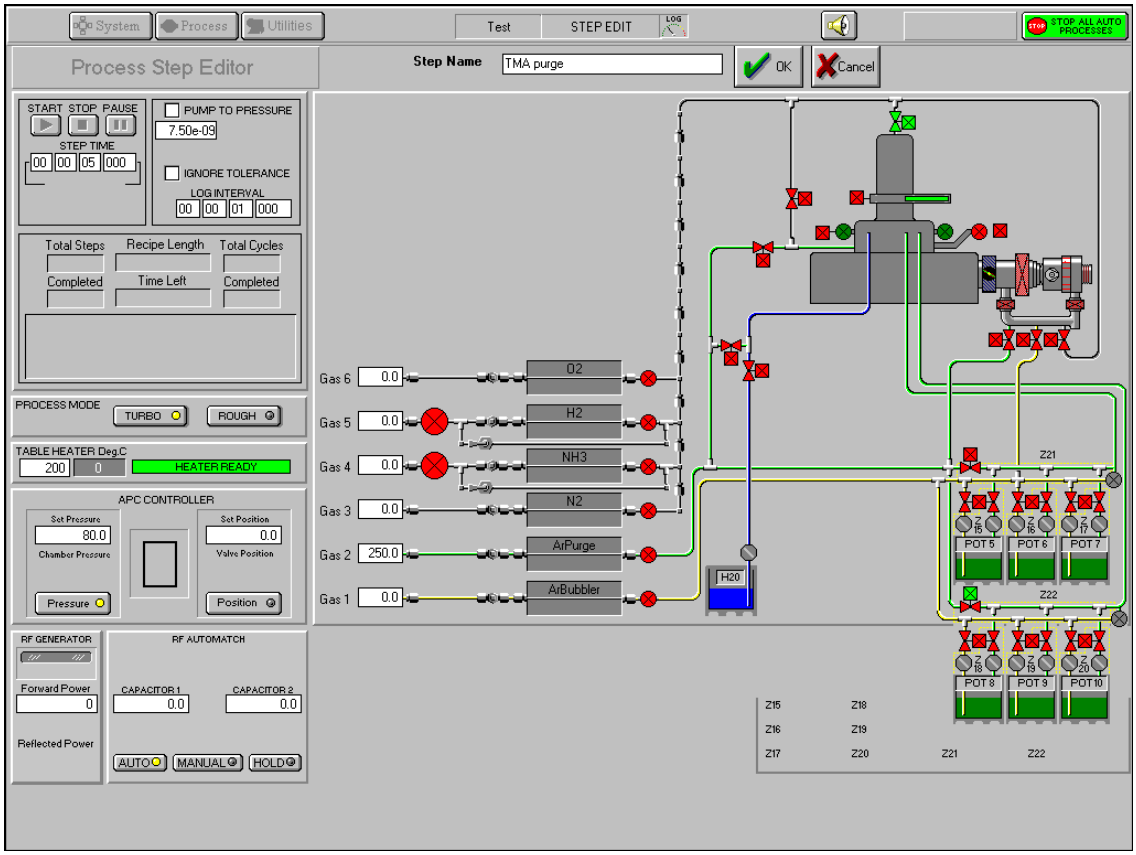
Step 7 – Water Purge



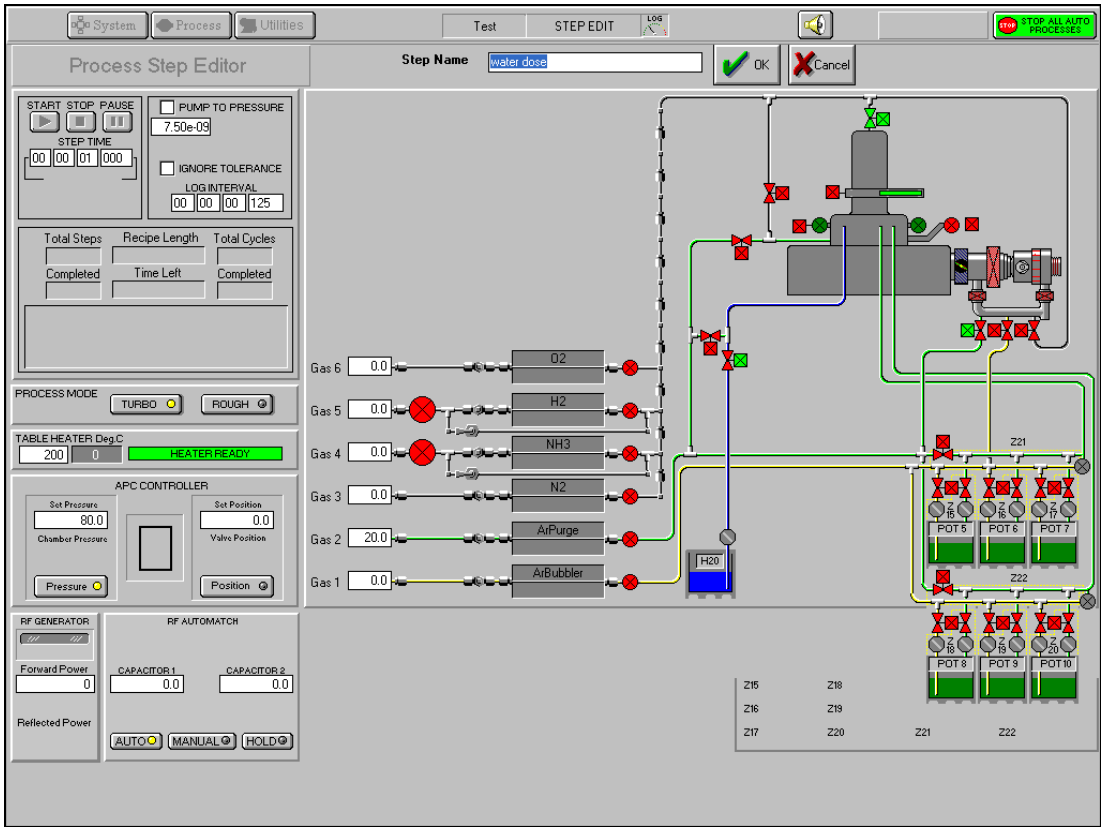
Step 8 – TMA Dose



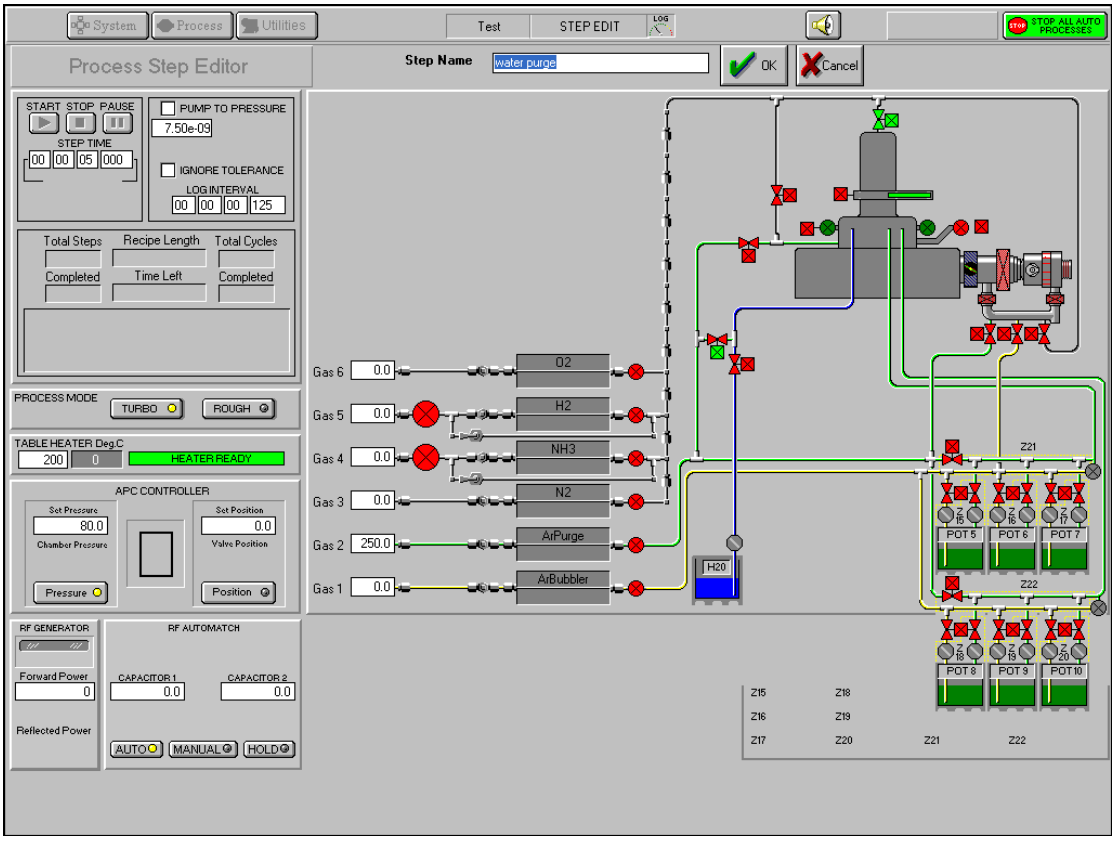
Step 9 – TMA purge



Step 10 – Water Dose



Step 11 – Water Purge



Step 12 – Pump Up