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Determining the interfacial density of states in metal-insulator-semiconductor devices based on poly(3-hexylthiophene)

N. Alves[a] and D. M. Taylor[b]
School of Electronic Engineering, Bangor University, Dean Street, Bangor, Gwynedd LL57 1UT, United Kingdom

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Low frequency admittance measurements are used to determine the density of interface states in metal-insulator-semiconductor diodes based on the unintentionally doped, *p*-type semiconductor poly(3-hexylthiophene). After vacuum annealing at 90 °C, interface hole trapping states are shown to be distributed in energy with their density decreasing approximately linearly from $\sim 20 \times 10^{10}$ to 5×10^{10} cm^{-2} eV^{-1} over an energy range extending from 0.05 to 0.25 eV above the bulk Fermi level. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2897238]

It is well known that trapping states located at the interface between the semiconductor and insulator can cause instabilities in the threshold voltage of metal-oxide-semiconductor devices based on crystalline, polycrystalline, and amorphous silicon. Small-signal admittance measurements have proved particularly useful for studying such states in silicon devices[1] and we have demonstrated[2,3] that similar measurements can be used for investigating interface states in organic metal-insulator-semiconductor (MIS) devices based on the *p*-type semiconductor poly(3-hexylthiophene) (P3HT). While there is some evidence[3] that the density of hole-trapping interface states decreases with increasing energy above the highest occupied molecular orbital of P3HT, a detailed investigation of the energetic distribution of such states has not yet been reported. In this contribution, we use the conductance method, initially advocated by Nicollian and Goetzberger (NG),[1] to reveal the density of states for the hole traps present at the interface between P3HT and the spin-on-glass polysilsesquioxane (PSQ).

For the study, we fabricated MIS capacitors on indium tin oxide (ITO) coated glass slides following our previously described procedures.[3] The PSQ gate insulator,~300 nm thick, was prepared by spin coating and thermally curing at 450 °C a precursor silsesquioxane (90% phenyl and 10% methyl content dissolved in butanone, Gelest Inc.). After cooling, the PSQ was treated with hexamethyldisilazane to render the surface hydrophobic. Subsequently, ~100 nm thick film of P3HT (Sigma-Aldrich Ltd.) was spin coated onto the insulator. The device was completed by evaporating a 50 nm thick gold electrode, 1 mm in diameter and surrounded by a guard ring. After preparation, the devices were heated under vacuum at 90 °C for several hours to remove adventitious dopants, e.g., atmospheric oxygen, from the P3HT. Measurements were then made at 30 °C using an impedance analyzer (Solartron Model 1255 with Dielectric Interface Model 1296). Bias and signal voltages were applied to the ITO electrode, with the detection circuitry connected to the gold electrode with the guard ring grounded.

Figure 1 shows the measured capacitance and loss (conductance/angular frequency) plotted as a function of bias voltage for frequencies in the range of 1 Hz–2.5 kHz. Although data was obtained by incrementing at 5 steps/decade, for clarity, data for only six frequencies are shown. The *C-V* plots demonstrate the changing conditions in the device from accumulation (negative voltages) to complete depletion of the semiconductor ($V > \sim 2$ V). Above ~600 Hz, the capacitance measured in accumulation (negative voltages) began to decrease rapidly signifying the onset of the well-documented[3] limitation on charge transport in the bulk semiconductor which gives rise to the classic Maxwell–Wagner relaxation characteristic of two dissimilar dielectric layers.[4] The "stretching" of the *C-V* plots at lower frequencies provides good evidence for the presence of interface

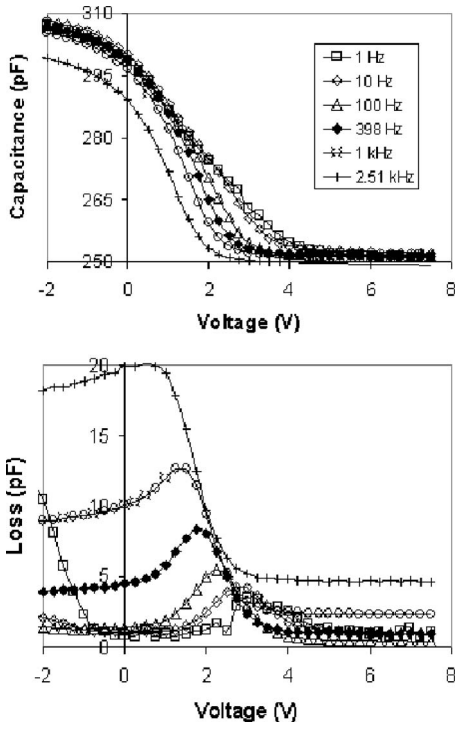

FIG. 1. (a) Capacitance and (b) loss (conductance/angular frequency) vs voltage plots obtained at six different frequencies in the range of 1 Hz–2.5 kHz for P3HT MIS diodes at 30 °C. The sharp rise in loss at 1 Hz for negative voltages arises from insulator leakage.

[a]Permanent Address: Faculdade de Ciências e Tecnologia, UNESP, CP 467, 19060-900, Presidente Prudente, SP, Brazil.
[b]Electronic mail: d.m.taylor@bangor.ac.uk.

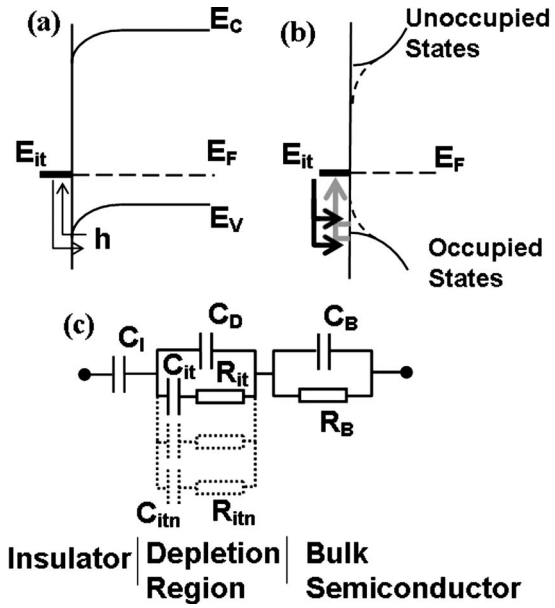

FIG. 2. Energy diagrams showing the interaction of holes with an interface state in (a) silicon and (b) a semiconductor with localized states extending into the bandgap. (c) Equivalent circuit representation of a MIS device with interface states biased into depletion.

states.[5] Loss maxima [Fig. 1(b)] increasing in magnitude and shifting to lower voltages as frequency increases, indicate that these states are distributed in energy.[1] Although using a guard ring may give rise to similar behavior,[6] this can be ruled out here since the loss peaks occur when the device is well into depletion.

In contrast to the loss plots [Fig. 1(b)], which are much more sensitive to the presence of interface states, little change is seen in the slope of the *C-V* plot between 631 Hz and 1 kHz. Therefore, since the stretching effect of the interface states is negligible in this range, the gradient of the Mott–Schottky plot,[7] i.e., C^{-2} versus V, corresponding to 631 Hz was used to deduce the acceptor doping density, $N_a = 2 \times 10^{16}$ cm^{-3}, in the bulk semiconductor.

To extract the energetic distribution of the interface states from the loss data, we follow the NG analysis[1] which is based on Shockley–Read–Hall statistics and a time-varying Fermi level resulting from the applied small-signal voltage. For a *p*-type semiconductor, the majority hole concentration at the interface greatly exceeds the electron concentration so we need consider only the interaction of holes with interface states [Fig. 2(a)].

Although developed for crystalline silicon, the model makes no appeal to any specific density of states distribution in the semiconductor,[8] so that the approach is more generally valid and can be applied, for example, to a semiconductor in which the density of localised, bulk hole states, $g(E)$, decreases exponentially with energy E into the bandgap,[9] i.e.,

$$g(E) = \frac{N}{kT_0} \exp - \frac{E}{kT_0} (0 < \mathrm{E} < \infty), \tag{1}$$

where N is the total number of states per unit volume, k is Boltzmann's constant, and T_0 is a parameter characterizing the distribution. These valence "tail" states are shown dotted in Fig. 2(b). Of interest here is that the fraction δ_S of these bulk states occupied at the interface depends on the gate-induced potential V_S at the semiconductor surface in the same way (except for the temperature dependence) as in the band model,[9] i.e.,

$$\delta_S = \delta_0 \exp - \frac{qV_S}{kT_0}, \tag{2}$$

where δ_0 is the fraction of states occupied by holes well away from the interface. The small-signal hole current flowing between the occupied bulk states and interface trap states is then calculated as the difference between the hole emission and capture rates by the traps, and leads to a complex admittance,

$$Y_S = j\omega \frac{q^2}{kT} \frac{N_{\mathrm{it}} f_0 (1 - f_0)}{(1 + j\omega (1 - f_0)/c_p p_{s0})}, \tag{3}$$

where $j = \sqrt{-1}$, ω the angular frequency of the small signal, q the electronic charge, N_{it} the density of interface states per unit area, k Boltzmann's constant, T the absolute temperature, and f_0 and p_s the Fermi function and hole concentration, respectively, established at the semiconductor surface by the bias voltage. For an organic semiconductor, the capture probability c_p is averaged over the tail states [Fig. 2(b)].

In the equivalent circuit in Fig. 2(c), Y_S describes[1] the series combination of R_{it} and C_{it} which has a time constant $\tau = R_{\mathrm{it}} C_{\mathrm{it}} = (1 - f_0)/c_p p_{s0}$ and in which

$$C_{\mathrm{it}} = \frac{q^2}{kT} N_{\mathrm{it}} f_0 (1 - f_0). \tag{4}$$

The other elements in this circuit represent the capacitance C_B and resistance R_B of the bulk semiconductor, and C_I and C_D the capacitances of the insulator and depletion region, respectively. Transforming the interface state response from the series to a parallel representation and including the depletion capacitance yields expressions for the equivalent parallel capacitance C_P and conductance G_P for the middle section of the equivalent circuit, i.e.,

$$C_P = C_D + \frac{C_{\mathrm{it}}}{1 + \omega^2 \tau^2} \tag{5}$$

and

$$\frac{G_P}{\omega} = \frac{C_{\mathrm{it}} \omega \tau}{1 + \omega^2 \tau^2}. \tag{6}$$

In the presence of a distribution of interface states, then, additional *RC* elements [shown dotted in Fig. 2(c)] must be included to represent each additional level. For a continuum of interface states, Eq. (6) is then replaced[1] by

$$\frac{G_P}{\omega} = \frac{qD_{\mathrm{it}}}{2\omega\tau} \ln(1 + \omega^2 \tau^2), \tag{7}$$

where D_{it} is the density of interface states per unit area per eV.

Following NG,[1] C_P and G_P may be evaluated from the measured capacitance and loss by correcting for the reactance of the insulator so long as conductance losses in the bulk semiconductor are negligible, i.e., well below the Maxwell–Wagner relaxation of the device. Figure 1(b) shows that this condition holds only for frequencies up to ~100 Hz. (In silicon devices, the limiting frequency is ⩾1 MHz owing to the higher carrier mobilities). When the device is in accumulation, bulk conduction losses in the semiconductor increase and distort the interface loss peak above ~100 Hz. In

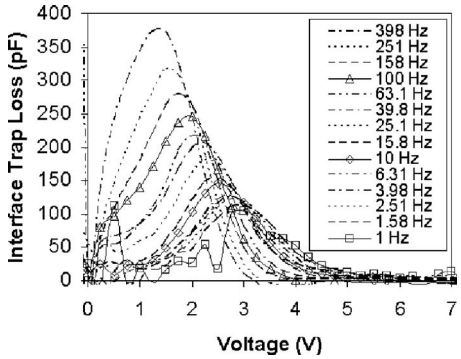

FIG. 3. Interface trap loss, G_P/ω, extracted from measured loss data and plotted as a function of applied voltage. Here, the data sets obtained at all frequencies up to 398 Hz are shown.

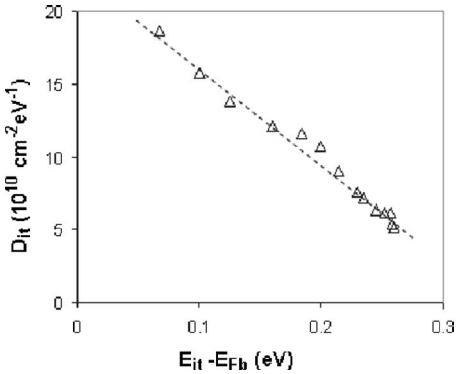

FIG. 4. Density of hole traps D_{it} at the P3HT/polysilsesquioxane interface plotted as a function of energy above the bulk Fermi level E_{Fb}.

depletion, additional parasitic losses cause further distortion above ~1 kHz. A first order correction can be made up to ~400 Hz by subtracting the bulk contribution to the loss, i.e., the plateau value in accumulation and an approximately linearly deceasing contribution throughout the depletion region[6] (this approach becomes increasingly tenuous at higher frequencies as terms involving products of the various elements become more significant). The resulting plots, based on data obtained at all test frequencies up to 398 Hz are shown in Fig. 3. Since the behavior is characteristic of a distribution of interface states, the maximum loss occurs when $\omega\tau=1.9$,[1] which upon substituting into Eq. (7) leads directly to an estimate of D_{it}, the density of interface traps being "interrogated" at the applied voltage corresponding to the maximum loss.

The energy E_{it} of these states is readily determined from knowledge of the band bending V_S induced by the applied voltage. Hence, applying the Poisson equation to the depletion region yields

$$Vs = E_{it} - E_{Fb} = \frac{qN_A\varepsilon\varepsilon_0 A^2}{2} \cdot \frac{1}{C_d^2}, \tag{8}$$

where E_{Fb} is the bulk semiconductor Fermi level and C_d is calculated at the appropriate voltage by assuming that at 631 Hz interface and bulk semiconductor losses are small so that the measured capacitance is the series sum of depletion and insulator capacitances.

The results of the analysis are given in Fig. 4 from which it is seen that the density of interface hole trapping states decreases approximately linearly from $\sim 20\times10^{10}$ to 5×10^{10} cm^{-2} eV^{-1} in the energy range of $0.05<(E_{it.}-E_{Fb})<0.25$ V. Probing deeper into the bandgap will require measurements to be extended below 1 Hz and working with thicker semiconductor films in order to achieve the necessary degree of band bending. Assigning an absolute value to the trap energies requires an independent measurement of E_{Fb}.

In conclusion, we have shown that admittance measurements provide a practical way forward for measuring the density of interface states in organic MIS devices based on *p*-doped semiconductors such as P3HT. Hence, the foundations have been established for undertaking a systematic study of the effects of processing conditions, aging etc on the interface properties of such devices.

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[1] E. H. Nicollian and A. Goetzberger, Bell Syst. Tech. J. **46**, 1055 (1967).
[2] I. Torres, D. M. Taylor, and E. Itoh, Appl. Phys. Lett. **85**, 314 (2004).
[3] I. Torres and D. M. Taylor, J. Appl. Phys. **98**, 073710 (2005).
[4] A. von Hippel, *Dielectrics and Waves* (Wiley, New York, 1954), p. 228.
[5] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley Interscience, New York, 1981), p. 382.
[6] D. M. Taylor and N. Alves, J. Appl. Phys. **103**, 054509 (2008).
[7] C. G. M. Fonstad, *Microelectronic Devices and Circuits*, International Edition (McGraw-Hill, New York, 1994), p. 254.
[8] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley Interscience, New York, 2003), p. 830.
[9] M. J. C. M. Vissenberg and M. Matters, Phys. Rev. B **57**, 12964 (1998).