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Distributed Harmonic Compensation in Single-Phase Low-Voltage Microgrids

Compensação Distribuída de Harmônicos em Microrredes Monofásicas de Baixa Tensão

Dissertation presented to the Universidade Estadual Paulista "Julio de Mesquita Filho", in partial fulfillment of the requirements for the degree of Master in Electrical Engineering.

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ATA DA DEFESA PÚBLICA DA DISSERTAÇÃO DE MESTRADO DE AUGUSTO MATHEUS DOS SANTOS ALONSO, DISCENTE DO PROGRAMA DE PÓS-GRADUAÇÃO EM ENGENHARIA ELÉTRICA, DA FACULDADE DE ENGENHARIA - CÂMPUS DE BAURU.

Aos 27 dias do mês de fevereiro do ano de 2018, às 09:00 horas, no(a) Instituto de Ciência e Tecnologia de Sorocaba-UNESP, reuniu-se a Comissão Examinadora da Defesa Pública, composta pelos seguintes membros: Prof. Dr. FERNANDO PINHABEL MARAFAO - Orientador(a) do(a) Engenharia de Controle e Automação / Instituto de Ciência e Tecnologia/UNESP, Prof. Dr. FRANCISCO DE ASSIS DOS SANTOS NEVES do(a) Departamento de Engenharia Elétrica / Universidade Federal de Pernambuco - UFPE, Prof. Dr. JAKSON PAULO BONALDO do(a) Departamento de Engenharia Eletrônica / Universidade Tecnológica Federal do Paraná - UTFPR, sob a presidência do primeiro, a fim de proceder a arguição pública da DISSERTAÇÃO DE MESTRADO de AUGUSTO MATHEUS DOS SANTOS ALONSO, intitulada **DISTRIBUTED HARMONIC COMPENSATION IN SINGLE-PHASE LOW-VOLTAGE GRIDS**. Após a exposição, o discente foi arguido oralmente pelos membros da Comissão Examinadora, tendo recebido o conceito final: APROVADO. Nada mais havendo, foi lavrada a presente ata, que após lida e aprovada, foi assinada pelos membros da Comissão Examinadora.

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"Ask, and it shall be given you; seek, and ye shall find;
knock, and it shall be opened unto you:
for every one that asketh receiveth;
and he that seeketh findeth;
and to him that knocketh it shall be opened."
("Matthew, 7:7-8")

ABSTRACT

The employment of switching power interfaces (SPIs) in power quality related issues is becoming a reasonable alternative to pursue maximum contribution of distributed energy resources in electrical grids. Beyond their major functionality, which is active power injection, additional ancillary services are possible due to the flexibility of their operations, being capable of providing interventions in reactive power support and many other important matters. Multifunctional inverters, as they are also called, could specially play a key role on harmonic mitigation, which may become a meaningful matter in low-voltage microgrids with high density of nonlinear loads spread out. Nevertheless, to take advantage of such multifunctional use it is fundamental to conquer a mutual and coordinated operation of many SPIs dispersed over the energy networks. Therefore, this work proposes an alternative two-level hierarchical topology focused on the cooperative operation of distributed SPIs, aiming their use on multifunctional activities related to harmonic mitigation in single-phase low-voltage microgrids. A novel secondary control approach, named Current-Based Control, is proposed aiming at achieving a coordinated contribution of inverters through a current sharing scheme, attempting power quality enhancement in a point of common coupling. The scope of this dissertation ranges from the design of primary level controllers for inverters, passing through simulation examples, up to the final experimental validation.

Keywords: Cooperative Control; Distributed Compensation; Harmonics; Multifunctional Inverters.

RESUMO

O emprego de *switching power interfaces* em problemas relacionados a qualidade de energia, tem se tornado uma alternativa interessante na busca de aproveitar ao máximo a contribuição de recursos energéticos distribuídos. Além da função majoritária, que é a injeção de potência ativa, serviços auxiliares são possíveis devido à flexibilidade de operação destes dispositivos, sendo capazes de prover suporte para potência reativa e muitas outras necessidades. Inversores multifuncionais, assim como também são chamados, podem especialmente ter papéis fundamentais na redução de distorção harmônica, que pode se tornar um ponto crítico em microrredes de baixa tensão com alta densidade de cargas não lineares dispersas. Entretanto, para usufruir dos benefícios da multifuncionalidade, é fundamental que se estabeleça uma operação coordenada desses inversores distribuídos. Portanto, este trabalho propõe uma topologia hierárquica de dois níveis focada na operação cooperativa de inversores, com o intuito de empregar atividades multifuncionais relacionadas à compensação harmônica em microrredes monofásicas de baixa tensão. A recente metodologia do chamado *Current-Based Control* é proposta, visando uma contribuição coordenada de inversores através de um esquema de compartilhamento de correntes, com a tentativa de melhorar a qualidade de energia em um ponto de acoplamento comum. O escopo desta dissertação foca desde o projeto de controladores de nível primário para inversores, passando por exemplos de simulação, até uma validação experimental final.

Palavras-chaves: Controle Cooperativo; Compensação Distribuída; Harmônicos; Inversores Multifuncionais.

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List of Abbreviations and Acronyms

AC	Alternating Current
APF	Active Power Filter
CBC	Current-Based Control
CC	Central Controller
CPT	Conservative Power Theory
CSI	Current Source Inverter
DC	Discrete Current
DER	Distributed Energy Resource
DG	Distributed Generator
DSO	Distribution System Operator
EG	Energy Gateway
FBD	Fryze-Buchholz-Depenbrock
FFHC	Fixed Frequency Hysteresis Controller
FFT	Fast Fourier Transform
MEA	Mean Absolute Error
PBC	Power-Based Control
PCC	Point of Common Coupling
PI	Proportional-Integral
PRep	Proportional-Repetitive
PRes	Proportional-Resonant
PV	Photovoltaic
PWM	Pulse Width Modulation
SG	Smart Grids
SPI	Switching Power Interface

SRF Synchronous Reference Frame

SS Storage System

TDD Total Demand Distortion

THD_i Total Current Harmonic Distortion

THD_v Total Voltage Harmonic Distortion

UI Utility Interface

VFHC Variable Frequency Hysteresis Controller

VSI Voltage Source Inverter

ZOH Zero Order Holder

Contents

1 Introduction

Renewable energy, since the past decades, has been catching attention as one of the most prominent alternatives to modernize the electrical power system. Besides this undeniable relevant matter, many other related reasons of a new trend on the energy sector lie on the sustainable capability of interchanging non-renewable sources by clean ones, and also on the economical side of their deployment, which is becoming more and more attractive around the world (OBAMA, 2017). As a result of this aggregation of ideas within the context of renewable energy, energy efficiency, future decentralization of resources, economic profitability and digitalization, a powerful definition named Smart Grids (SG) has been changing the implications of electricity and how its technologies are thought (KIESLING, 2016).

Focusing on the electrical outlook, this new approach based on distributed energy resources (DERs) directly impacts on grids' dynamics, once more diversified electricity generators may now be interconnected and contribute to the overall power availability in a network. In addition, with its intrinsic assorted generation capability, the traditional electrical grid concept has been evolving towards a more flexible structure under bidirectional power flow, able to account for smarter power management and countless other operations that may benefit grids themselves, utilities, and consumers (FANG *et al.*, 2012). Yet, allowing the creation of new paradigms, such as of the so-called prosumers (GRIJALVA *et al.*, 2011), in which distributed generators (DGs) have the opportunity to offer their surplus local energy production to a grid, for instance, in exchange for an economic reward.

Despite the global agreement on the prosperity of adopting a cleaner and more decentralized grid, from the technical side of this demand, it is imperative for all technologies there employed to provide reliable means of operation, accounting for a high interactive and diversified electrical system. A reasonable explanation for such need is given by the complexity behind integrating several technologies, which are composed of particular architectures and power generation characteristics, being also differently affected by intermittent climate conditions, and not equally responding to grid behaviors. DERs based on wind, photovoltaic (PV) and fuel cell generators, as well as storage systems or electric vehicles are good examples of such diverse architectures.

Switching power interfaces (SPIs) play a key role on DERs integration into grids, dispatching generated power under compliant requirements (KROPOSKI *et al.*, 2010). SPIs are power converters, or even called inverters, capable of converting DC generated power into usable AC power, under specific voltage and current conditions of frequency, amplitude and phase. The compliance of SPIs' operation with legally demanded grid regulations is crucial, as required in countries like USA, Germany and Brazil, through the respective standards, IEEE Std. 1547 (IEEE, 2003), VDE-AR-N 4105 (VDE, 2011), and ABNT NBR 16149 (ABNT, 2013).

Inverter technologies may also be employed in power quality enhancement, which has been increasingly required since nonlinear loads spread over electrical networks (SALMERON; VAZQUEZ, 2007). Nonlinear loads are defined by their unique behavior of not responding as a resistive, inductive or capacitive load, draining non-sinusoidal currents even when supplied by sinusoidal voltages (HART, 2011). That characteristic, which earlier was only particularly encountered in adjustable speed drives, arc furnaces and other heavy duty power equipment, are now proliferated due to intense use of switched-mode power supplies in the design of many kinds of home appliances and small electronic devices.

One of the main inconveniences of such nonlinear behavior of loads is related to the infliction of significant harmonic distortion onto current and voltage waveforms. As described by (ARRILLAGA; WATSON, 2004), heavy harmonic distortion may result in capacitors resonance, overheating and loss of torque in electrical machines, skin effect in transmission lines, unreliability in measurement instruments, false trips of circuit breakers and many other disturbances.

As the nonlinear loads are tied to an intolerable burden in electrical grids, specially by their harmful impact on more sensitive networks, e.g., low-voltage grids (BONIFACIO *et al.*, 2013), defining ways to prevent nonconformities have become compulsory. To reduce the harmonics impact and to comply with electrical requirements, power conditioners as passive, active and hybrid filters, have been extensively proposed, as further discussed in Chapter 2. In addition, expanding to the new model of electrical grids with large amounts of DGs dispersed, the consideration for power quality matters increases even more as a result of dynamic load profiles, complex interaction among nodes, and also by having intermittent bidirectional power flow.

Microgrids (LASSETER, 2002) may be one of the most suitable examples to point out how considerable amounts of nonlinear loads negatively affect power quality in low-voltage grids. This electrical entity, as defined by the U.S. Department of Energy Microgrid Exchange Group, presents a defined boundary, comprising groups of interconnected loads and DERs, being a single-controllable unit able to provide power flow management at a point of common coupling while respecting its power restrictions. Besides, it can operate connected or disconnected (islanded) from the main grid as desired. Based on this definition, dynamic interactions are intrinsically expected to occur inside such microgrids. As a result, the disturbances caused by drawing non-sinusoidal voltages and currents may affect the entire operation of both microgrid and the main grid when interconnected, unless power quality counter-measure actions are taken.

As coordination of distributed units have therefore become relevant, other related recent prospects are showing prominent usefulness due to their flexibility to provide decentralized operation, and reliable interaction of DERs. For such case, cooperatively operated distributed interfaces with plug and play features will likely be one of the most suitable alternatives in a near future on power quality improvement (LIGHTNER; WIDERGREN, 2010). Within that matter, distributed multifunctional SPIs (MARAFAO *et al.*, 2015) are gaining a positive status and strengthening its acceptability to be those interfaces. That may be justified by their fundamental presence in most of DERs, ease for supporting intelligent activities, and for their proved feasibility that many studies have been stating (BRANDAO *et al.*, 2017; YANG *et al.*, 2016; TENTI *et al.*, 2010). Moreover, looking at smart grids' regulatory and market perspectives, interest in their employment and applications are rapidly rising, said to be the future (KROPOSKI, 2016), and may also be evidenced by eminent leading edge regulations, such as the Rule 21 (CPUC, 2013) and the new UL 1741 SA standard (GONZALEZ *et al.*, 2016).

Being attached to the idea of developing flexible tools for supporting power interventions with SPIs, specially focused on power quality duties under disperse coordinated operation over low-voltage microgrids, the main goal of this dissertation is settled. The secondary control layer of a two-level hierarchical control methodology for cooperative operation of multifunctional inverters is herein proposed, aiming harmonic current mitigation at the point of common coupling (PCC) in low-voltage single-phase networks. Regardless of the microgrid's voltage condition, the control methodology, which is herein called Current-Based Control (CBC), aims at standing reliable and consistently providing the sharing of active, reactive, and harmonic terms among distributed SPIs.

Therefore, this work intents to clearly describe the mathematical development of the methodology, and additionally explain its translation into real physical application considering power electronics technologies. Extensive computational simulations are carried out to demonstrate the adequacy of the secondary controller under diverse circumstances. Furthermore, experimental results are performed to validate the adoption of this harmonic current sharing method, and also, start discussions related to possible inherent constraints.

1.1 Dissertation Contribution

Techniques employed on cooperative control of dispersed SPIs, as later presented in the state of the art, have been recently proposed following several approaches. Among many strategies, two approaches must be particularly highlighted to emphasize the motivations of this work, being them: a centralized methodology based on power terms, which is named Power-Based Control (CALDOGNETTO *et al.*, 2015b), and decentralized techniques based on droop control methods (GUERRERO *et al.*, 2013).

The first approach is the foundation of the Current-Based Control methodology since, being developed under a master/slave hierarchical control architecture, it provides power sharing among distributed SPIs driven as current-controlled sources within a microgrid. In addition, this topology takes into consideration the existence of a tertiary upper layer which establishes the power flow requirements at the PCC under interconnected mode, a secondary layer that, based on data exchanging with distributed SPIs, provides accurate sharing of active and reactive power terms, and a lower primary layer responsible for the local control o SPIs and their DERs. The feasibility of such approach has been extensively reiterated (BRANDAO *et al.*, 2017; CALDOGNETTO *et al.*, 2015a) for the *P/Q* power management (SANGWONG-WANICH *et al.*, 2018) in microgrids, coordinating SPIs to attend a demand of active power injection and reactive power compensation in a network, as desired by a central controller.

Nevertheless, the Power-Based Control does not present an intrinsic method for mitigating current and voltage harmonic distortions, depending on the existence of an interactive grid-forming converter connected to the PCC (BRANDAO, 2015) to compensate such disturbances for the entire microgrid. The main reason of such requirement is related to the fact that, being developed to handle power terms based on a conservative manner, this methodology is not able to deal with harmonic power due to its non-conservativeness (TENTI *et al.*, 2011). This means that, particularly for the Power-Based Control approach, if a power quantity does not present a conservative feature, it is not suitable to be partitioned and addressed as a reference for remote control of SPIs (TENTI *et al.*, 2011). Consequently, rising as an alternative for finding a more suitable approach to deal with harmonic compensation under a cooperative perspective, a centralized methodology based, not only on power terms, but on decomposed current parcels allows to attain a more tangible and comprehensive coordinated control. Therefore, the resulting methodology coming from this discussion converged on the herein proposed Current-Based Control.

Decentralized methodologies based on droop control must also be reiterated here due to their wide adoption in microgrid control (HAN *et al.*, 2016a; SREEKUMAR; KHADKIKAR, 2017). When comparing to the Power-Based Control, in a general way, such approach presents the very convenient feature of not relying on communication links to coordinate distributed SPIs within a network. This allows a more flexible operation in terms of plug & play capabilities, also eliminating issues related to data transmission and dependence on grid-forming converters for operation in islanded mode. Nonetheless, classic methodologies of decentralized droop based control (DDBC) are well-known by causing frequency and voltage deviation as a tradeoff upon *P/Q* power sharing (GUERRERO *et al.*, 2013; ZHONG; ZENG, 2016).

Additionally, classic DDBC depends on previous knowledge about line impedances and it is mainly employed with SPIs operating as voltage-controlled sources, which requires more complex control approaches than the one required by the Power-Based Control (ROCABERT *et al.*, 2012). Yet, beyond the fact that most DDBC methods provide power sharing based on power terms, none of them are able to concentrate, in one methodology, the ability to coordinate distributed SPIs in islanded and grid-connected mode, providing sharing of active, reactive and harmonic terms, balancing of SPIs' thermal stresses over the microgrid, and also allowing compensation of harmonic current terms in a selective way. Thus, being able to aggregate all those features, the contribution of the CBC presentation can be reinforced and justified as well.

Having stated the premises of the development of the CBC algorithm, the main contributions of this work are said to be the following:

1. Provide a detailed explanation about the Current-Based Control methodology, its master/slave architecture and operational scheme for active, reactive and harmonic current sharing;

2. Demonstrate the complementary abilities of the CBC on providing proportional coordination of current injection, respecting individual thermal stress capabilities of SPIs, and also on performing selective harmonic compensation at the point of common coupling under generic voltage conditions;

3. Evaluate the CBC operation with several SPIs, considering different network scenarios, along with the dynamic conditions of single-phase microgrids;

4. Present initial considerations on the matter of system stability and data transmission issues, on the matter of the hierarchical topology of the CBC;

5. Implement a single-phase laboratory-scale prototype able to support the interconnection of several SPIs, with the goal of allowing further experimental validation of the CBC and other distributed control methodologies.

1.2 Dissertation Structure

This dissertation is organized following a chronological and sequential approach, allowing readers to follow the evolution of the concepts until the plain understanding of the main proposal for power quality improvement in single phase low-voltage grids, as well as the impacts of its experimental results.

The literature review brought in Chapter 2 aims at showing what has been proposed so far regarding distributed compensation, having the intention to later clarify the contribution of this particular work proposed herein. Chapter 3 brings explanations related to the main topology adopted for the modeling of DC-AC converters to be used in later developments. Along with it, methodologies for the implementation of three-level PWM modulation, the design of LC output filters, and also a synchronism algorithm are presented.

In Chapter 4, the primary control layer of the hierarchical control is approached, focusing on the design and adequate operation of SPIs. Control methodologies for SPIs and their modeling are taken into consideration, with the purpose of determining which may be the most suitable for implementation in simulations and experimentally.

Chapter 5 presents the original Current-Based Control approach, focused on enhancing power quality in single-phase microgrids through harmonic mitigation and support for reactive currents. Discussions related to the methodology of this secondary control proposal, as well as the mathematical development behind it are raised.

Simulations more focused on cooperative operation of SPIs, aiming at harmonic mitigation at the PCC, are carried out in Chapter 6. Some case studies give an overview of the selective and multifunctional capabilities brought by the employment of the Current-Based Control. The experimental work is presented in Chapter 7 for a preliminary validation purpose.

Finally, Chapter 8 concludes and proposes future works.

2 State of the Art in Distributed Compensation

When it comes to establishing power conditioners for power quality improvement, passive filters may be considered the most classical solutions, being adopted for a long time (JULIO *et al.*, 1973; PENG *et al.*, 1988). Regarding local compensation strategies, pros and cons of several topologies of passive filters have already been deeply discussed in the literature (DAS, 2004; NASSIF *et al.*, 2009), affirming that benefits from their use ranges from fast response time to economic attractiveness in MW rating systems. Negative effects stand on lack of flexibility once new tuning setpoints may be needed, series and parallel resonances, and up to the limited operation with loads like cycloconverters or in the presence of interharmonics (BASIC *et al.*, 2000; XU *et al.*, 2010).

A more elaborated solution than passive filter, for what concerns harmonic damping, reactive power correction, unbalance current minimization and other power quality issues, is active power filter (APF). Taking advantage of switching semiconductors, this technology has achieved a significant status in reliability and effectiveness, by providing more flexible means for tackling issues in diversified applications (AKAGI, 2005; SINGH *et al.*, 1999). Yet, with their use under distinct topologies, such as shunt, series and hybrid filters, and based on local control techniques (AKAGI, 1996; BRANDAO *et al.*, 2016), the impact of nonlinear loads was proven to be diminished in electrical circuits.

Once passive and active filters started to be intensively employed in dispersed nodes along networks, and a more significant number of them were present, a trend for their decentralized operation has emerged. From the primary local applications aforementioned, their employment followed a rising tendence onto radial distribution (AKAGI, 1997) and then to decentralized operations (CHENG; LEE, 2006). Concomitantly, as depicted in Fig. 1, this decentralization process of passive and active filters created a need for having each unit operating in accordance with their primary design, while not impacting others. Therefore, considering that it was a non-trivial task that required further study, proposals for modeling and designing those decentralized systems started to track a new path in the literature as following discussed.

Poorly controlled interaction among dispersed power filters may result, for instance, in issues as worsening of voltage harmonic content, and also voltage rise in ending nodes on long feeders as complication of Ferranti's effect (DAS, 2015b). Focusing on these two specific concerns, Wada *et al.* (2002) started to brainstorm ideas onto decentralization, aiming to use APFs in radial feeders with power factor correction emulating resistive characteristic intending at tackling the so-called "whack-a-mole" effect. Thus, this work showed that, the whack-a-mole issue, which refers to effective voltage harmonic compensation on respective installation nodes, but deterioration on other feeders' locations, may be overcome if the dispersed shunt APFs are capable to control their characteristic impedances, acting as resistors in specific frequencies.

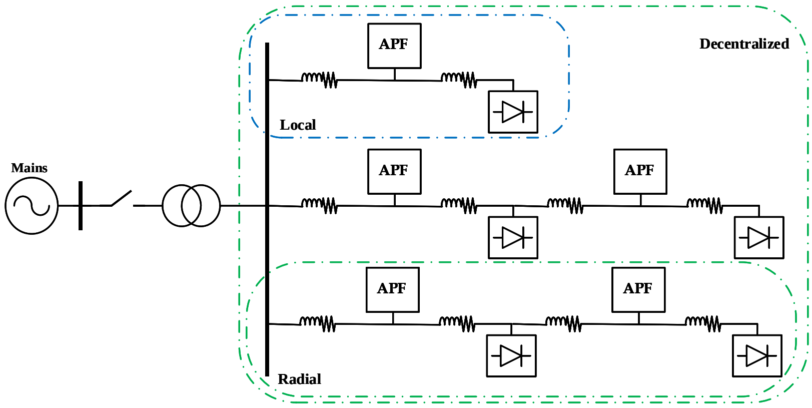


Figure 1 – Decentralization process of passive, active and hybrid filters.

Compensation was achieved by means of controlled current injection based on voltage harmonics detection at the installation points. Besides, the technical development points out that placing APFs in end buses does not cause whack-a-mole, if installed considering a maximum distance of a quarter of the wavelength of the most critical lower harmonic frequency.

As distributed compensation techniques started to sprout, there was an inevitable convergence into a mutual controlled operation as means for avoiding negative operation interferences, and also for sharing power quality improvement duties. Pursuing harmonic damping through dispersed APFs, in Jintakosonwit *et al.* (2003), an alternative for this joint maneuver was elegantly defined as cooperative control operation. For this particular study, regulating conditioners to operate under a cooperative way strove for having shunt APFs sharing local harmonic compensation deeds by automatically adjusting their control gains, as well as not letting total voltage harmonic distortion levels (THD_v) to rise above a certain limit on determined nodes.

Though powerful, as discussed in Chen *et al.* (2005), the spreading of APFs throughout networks has the inconvenience of high costs due to the need of their elaborated design and operation. That strengthens the reason of employing joint operation, as therein proposed by having distributed passive filters designed for suppressing harmonic components of most critical orders and supplying reactive power for the distortion source, while having smaller APFs mitigating current harmonics along with the correction of unbalanced currents. This idea is presented as a way for providing a more economically feasible alternative, as it lower the APF's power rating, and consequently its price.

Back to the cooperative operation proposed mainly with APFs in (JINTAKOSONWIT *et al.*, 2003), it imperatively relied on exchanging information from each APF unit, such as their actual compensation current injection and THD_v of each respective site of installation, making it dependent upon a reliable communication system. For this particular case, the communication link is established by a 16-bit parallel common data bus that is responsible for transmitting the local information of each APF to the host computer, as well as transmitting response commands calculated by the host computer to every APF individually. Control references for compensation purpose were attained using a similar method to the previous case discussed. As a result of the work, two cooperatively operated APFs were capable of sharing compensation goals, being both in different buses or even at the same one.

Although effective, by depending on serial communication links at that time, possible delays on data transfer and processing affected the system operation and caused difficulties to operate on transient conditions. Besides, the update time of control setpoints had to be longer than $70ms$ to avoid the so-called limit-cycle instability due to the time constant of low-pass filters. As a consequence, works like the one presented by Lee *et al.* (2008), started to aggregate droop control methodologies onto cooperative coordination of dispersed power conditioners. The major benefit of applying droop characteristics on this sort of control is given by the real-time response capability with no dependence on communication.

For instance, this particular study (LEE *et al.*, 2008) proposed a dynamic tuning method that leads to enhanced harmonic voltage mitigation using a droop control approach, based on conductance adjustment commands as the power related to harmonic currents changed along the line under different nonlinear load conditions. Another relevant matter was the regulation of APFs' power capacity, ensuring that each unit endured their maximum rated filtering capabilities. That was done through a synchronous reference frame (SRF) current transformation, with a proportional-integral (PI) controller modifying APFs' gains. Despite being useful and widely accepted as efficient, droop control approaches also present drawbacks as frequency and voltage deviations, limitations when line impedance is not properly considered, and fluctuations caused in the presence of DGs due to intermittent active power injection (HAN *et al.*, 2016a).

Broadening to a perspective where DGs began to more commonly appear in electrical networks, new possibilities came along to improve harmonic mitigation in partnership with passive and active filters. In a general way, since DGs take advantage of SPIs to modulate voltage and current for injecting active power following grid's standards, they can also be used to support compensation goals. Having that ability, as showed by Hashempour *et al.* (2016), it becomes possible to manage dispersed APFs and DGs to work together on compensation of voltage harmonic distortion. For this particular case, two levels of a hierarchical control topology using ancillary droop scheme are presented.

The primary control level uses the principle of selective virtual impedance (GUERRERO *et al.*, 2013) to locally control the current and voltage loops of each DG. Thus, the secondary control manages a selective harmonic compensation, in a way that when the harmonic content is not enough mitigated by the DGs, the APFs dispersed on the grid share the effort to compensate the residual pollution according to their respective power ratings. Some of the most interesting benefits of adopting virtual impedance in control loops are that it is robust regardless whether the line impedance has accentuated inductive or resistive characteristics, and also that, it can simulate resistances with no power losses. On the opposite side, it adds complexity to SPI modeling once the output impedance is not a predetermined value for designing gains, impacting as well in trades on droops relationships.

Nowadays, the penetration of DGs has become significantly high, inevitably, leading to the spread of large numbers of SPIs in the electrical networks. The more SPIs are available, the more useful tools in terms of compensation are added to the power grid. By the fact that they are part of DGs' structures, and are already settled and interacting with the grid, their implementation is also made easy by only adjusting software. Furthermore, focusing on distributed compensation purposes, multifunctional inverters are extremely interesting tools because they allow different techniques to be used on synthesizing references for mitigation of voltage and current harmonics, reactive power and unbalance currents correction, grid voltage support, and several other features (YANG *et al.*, 2016; MARAFAO *et al.*, 2015).

Power theories, for instance, may provide interesting means for modulating compensation signals through multifunctional SPIs. In Zeng *et al.* (2014), the possibility of deriving harmonic and reactive currents through equivalent conductances and susceptances, brought by the Fryze-Buchholz-Depenbrock (FBD) theory (DEPENBROCK, 1993), is adopted on generating and sharing control current references. Yet, with the use of proportional-resonant (PRes) current tracking controller, and low pass filters for detecting fundamental components, a coordinated operation of multifunctional inverters was shown effective for improving power quality, even in non-sinusoidal grid voltage conditions. It is worthy mentioning that a general constraint of multifunctional SPIs lies on remaining power availability to employ auxiliary functions, since the main goal of these equipment is supply of active power (BONALDO *et al.*, 2016; HOSSAIN *et al.*, 2018).

Following a similar approach, the Conservative Power Theory (CPT) (TENTI *et al.*, 2011) has been extensively used in many approaches with multifunctional inverters for distributed compensation goals. In Marafao *et al.* (2015), the study proved that multi-tasks can be accomplished based on the CPT, once it gives the ability to decouple current references that may be used to selectively damp harmonics and provide reactive current compensation. At the same time, it could allow SPIs to interact with grids and DERs to inject active power or even, for example, to absorb it for storage purposes. An extension could be considered for the reinforcement that the CPT implemented for multifunctional means may also be effectively used in three-phase systems along with non-sinusoidal conditions (BRANDAO *et al.*, 2016). At last, power quality improvement at the PCC could as well be attained by an elaborated approach of the CPT with optimization techniques, such as linear programming using Simplex algorithm (BRANDAO *et al.*, 2016).

In terms of optimization, and retrieving to the main limitation of multifunctional uses, an interesting work showed the possibility to tackle power quality disturbances, while also attaining optimal utilization of a SPI's remaining power (ZENG *et al.*, 2015). Two objective-oriented compensation control techniques were proposed, the first aiming to evaluate power quality enhancement at a PCC using as minimal apparent power as possible, and the second trying a maximum improvement with certain apparent power available. Nevertheless, as drawbacks, optimization solutions are usually followed by digital processing constraints, such as convergence, time delays and limited processing capability.

Although selective compensation may be achieved as previously mentioned, each multi-functional inverter is very likely connected to different node conditions regarding harmonic distortion and other disturbances. That may be due to, mainly, a not uniform amount of nonlinear loads in each electrical node of their corresponding DGs, i.e. low-voltage residential systems. With such differences, cooperative operations become arduous as a result of these electrical variations along the network. Optimization has also been applied to cooperative and distributed control of microgrids by (MAKNOUNINEJAD; QU, 2014), in a way that DGs' reactive power dispatch is controlled based on a power loss minimization algorithm, providing a consistent voltage profile not always acquired in droop methodologies.

To tackle this sort of issue, Munir *et al.* (2016) took advantage of a modal analysis scheme to perform selective harmonic compensation considering the respective priorities of individual SPI's nodes. Yet, as a result of a virtual harmonic impedance methodology for inverter controllers, mitigation of locally undesired currents was provided in single or multiple resonances. For establishing such approach, however, it is advisable to keep track of the possible impact caused by those individual local compensations at the PCC conditions.

Recently, the concept of microgrids has also introduced new challenges regarding power quality concerns in "weak" electrical grids (PAQUETTE; DIVAN, 2014), such as: reliable interactivity between DERs and the grid, in terms of respecting electrical limitations of the related devices, and the thresholds determined by standards that regulate the operational conditions of grids and interconnected equipment (IEEE, 2014a; IEEE, 2003); supporting transitions from connected to islanded modes considering the use of storage systems, requiring ability to adequate frequency and voltage amplitude for this later case; and also many other disturbances caused by inadequate operation of switching interfaces in DGs. Thus, additional intelligent and robust approaches have been targeted on studies since the past years, especially when it comes to an even more complex situation, which is the cooperative operation of those distributed resources. Considering such scenario (e.g., non-sinusoidal voltages), one of the leading milestones worthy to be pointed out is the one presented by Tedeschi *et al.* (2009).

The main contribution of this study is given by the use of complex power quantities as parameters for a coordinated control conception, considering single or poly-phase systems, under or not sinusoidal condition, with an assorted number of power conditioners along the microgrid, such as APFs, SVCs, SPIs and so forth. By diagnosing PCC's electrical quantities through a complex power decomposition, which may be said to be an earlier approach of the aforementioned CPT, compensation terms may be derived in a central controller (CC). Hence, by employing a dispatching logic that accounts for each conditioner available on the network, compensation currents references are sent to be generated, aiming the reduction of disturbances. The major foundation of the proposal brought in this dissertation is much related to the methodology of cooperative control, although being made by current terms instead of complex power. Deeper discussions on benefits and limitation of those knowledge lines will be later discussed.

A more elaborated development of this previous mentioned concept, progressing on the pursuance for effective cooperative operation of DERs, had as outcome the proposal of the so-called Power-Based Control (PBC) (CALDOGNETTO *et al.*, 2015b). For this case, a central controller that may be included in a three-phase converter named utility interface (UI), is responsible for gathering information from all of the distributed units, as long as it is comprised of a consistent communication bandwidth. This information includes, for each SPI spread over the microgrid, their power generation/absorption capability, apparent power rate, along with their previous and actual contribution on active and reactive power. Therefore, the PBC processes that information aiming a common goal, then broadcast operation commands driving all units to contribute to the microgrid's needs in proportion to their corresponding power capacity. A generalization of the PBC on a hierarchically organized microgrid is depicted in Fig. 2.

The control methodology of microgrid for that proposal is based on a three-layer hierarchical structure. Its primary level basically comprises the three layers of distributed generation systems with basic and specific functions, and also ancillary services (BRANDAO, 2015). Basic functions are described, for instance, by current/voltage control and grid synchronization. Specific functions are related to operations of maximum power point tracking (MPPT), anti-islanding protection, plant monitoring and so forth. Lastly, ancillary services are responsible for local harmonic compensation, overvoltage dynamic control and many other possibilities.

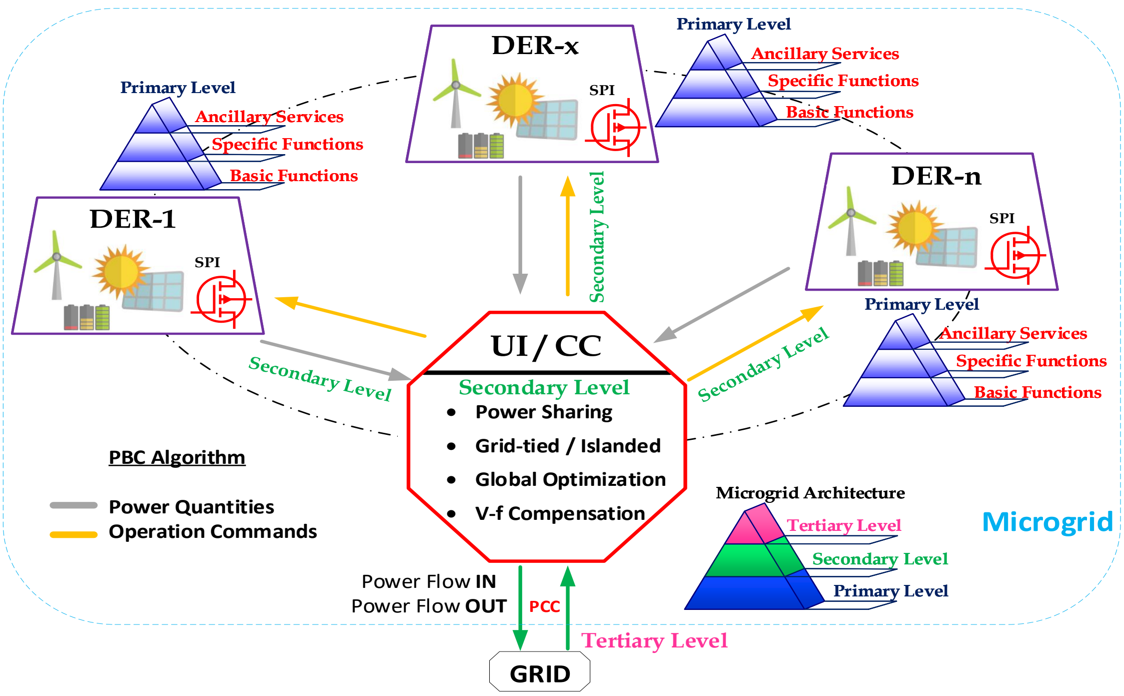


Figure 2 – Microgrid infrastructure and PBC generalized operation.

Secondary control, which is the main focus of the PBC algorithm, is based on a power sharing scheme that takes responsibility for microgrid's energy management and general welfare operation of all distributed units. Supplementary, a tertiary control sets the active and reactive power flow at the PCC, and still allows the UI to use its control loops to diminish remaining disturbances at the PCC in real time, while also maintaining a high power factor. For the integration of such methodology, a master-slave topology proved to provide an effective performance. Being that said, it is possible to mention in advance that, since the PBC is an improvement of the main idea in (TEDESCHI *et al.*, 2009), the proposal in dissertation aims at widening its concepts following a parallel approach.

To emphasize PBC's effectiveness on distributed cooperative operation, and consequently its flexibility to be applied for many different scenarios, Brandao *et al.* (2017) showed that it is conceivable to use arbitrarily connect multifunctional SPIs in three-phase four wire systems to provide a phase-independent control method. Under the same master-slave topology, unbalance compensation and power flow among different phases may be attained even under distorted and asymmetrical voltages using dispersed single-phase converters. Also, becoming possible to enhance power quality at the PCC without previous knowledge of line impedances, neither current phase displacements.

Hierarchical control and another proposal of power sharing among DERs is likewise exploited by Han *et al.* (2016c), aiming enhanced power quality with focus on islanded microgrids in presence of nonlinear and unbalanced loads. However, instead of a three-layer scheme, primary and secondary control are combined with droop controllers targeting real and reactive power, implementation of positive and negative sequence impedance loops, along with virtual variable harmonic impedance loops. All of that being regulated under a centralized operation, in which a low bandwidth communication link is required to allow data flow among all units and central controller.

In (SREEKUMAR; KHADKIKAR, 2017), a hierarchical uniform harmonic sharing is achieved without requiring communication, combining the concept of variable virtual impedance and feedforward control. This work presents an interesting way of exploiting DGs capabilities without exceeding their nominal currents. The sharing of harmonics is set on a droop-related compensation factor dependent on the harmonic power availability of each DG. The main drawback is the inability to provide selectivity of harmonic compensation, which directly leads to bandwidth constraints for applied current controllers, resulting in poor compensation under much distorted conditions. Besides, power flow control at the PCC is not addressed in (SREEKUMAR; KHADKIKAR, 2017).

Finally, (LORZADEH *et al.*, 2015) introduces a two layers hierarchical strategy based on circulating currents. The primary layer comprises of error compensation loops to relieve the burden of no previous knowledge of network parameters, and based on a low bandwidth communication link, a secondary controller drives voltage source SPIs toward the proportional share of reactive power and harmonic currents, similarly to (GOLSORKHI *et al.*, 2017). The balancing of SPIs current contributions is obtained through a mixed scheme of synchronous (dq) and stationary ($\alpha\beta$) frame controllers. The defined distribution factors that proportionally coordinate SPIs are attained by power terms, which make the scheme not fully based on currents. Moreover, the flow of active, reactive and harmonic quantities at the PCC cannot be regulated in grid-connected conditions, and SPIs are also susceptible to transient overcurrent stress due to the virtual resistance features, requiring adaptations as explained in (GOLSORKHI *et al.*, 2017).

All the content of this literature review is highly important to consolidate the evolution of power quality enhancement approaches, considering that new trends have been taking over electrical systems, additionally bringing new challenges to be resolved, which in summary are: the complex coordination and interaction of distributed SPIs, stability matters of DG insertion on such dynamic scenario, and non-active current management in diversified nodes. Moreover, these discussions provide a way to chronologically show how the proposal in this dissertation arose, and may later exalt its scientific contribution.

3 Modeling DC-AC Converters for DERs

Regarding the content further discussed in this chapter, firstly, an overview is given on the chosen inverter topology, as well as on the testbed proposed for further simulations. Then, the methodology of the adopted PWM technique is explained. After that, a low-pass output LC filter, which is responsible for coupling the inverters with the grid, is described and designed. A phase-locked loop algorithm is later discussed, with the intention of demonstrating how SPIs synchronize their references to actively participate in grid-tied operations. Lastly, the open loop model of the inverter is described and discussed for further design of four distinct current controllers and one voltage regulator.

3.1 Inverter Topology

Regardless of topology, an uncountable number of power converters for DERs have been proposed and questioned over the years (FOROUZESH *et al.*, 2017; GUPTA *et al.*, 2016; ZENG *et al.*, 2013; TEKE; LATRAN, 2014). Particularly on DC-AC conversion, a conventional generalized full-bridge topology is highly adopted (ESPINOZA, 2011). Considering single-phase applications, such topology is demonstrated in Fig. 3. If three-phase circuits are the focus, then a similar topology may be applied, although with one more leg being added to the SPI, or even two more legs if in four-wire circuits (LIBERADO, 2017). The main idea behind the concept of such devices is the conversion of DC voltage and current, which are supplied by an energy storage element, to the AC format through controlled alternated commutation of switches.

As found in literature (ESPINOZA, 2011), inverter topologies are generally defined by two possible approaches regarding their DC side energy storage, being described as voltage source inverter (VSI) or current source inverter (CSI). When output voltage control is the main

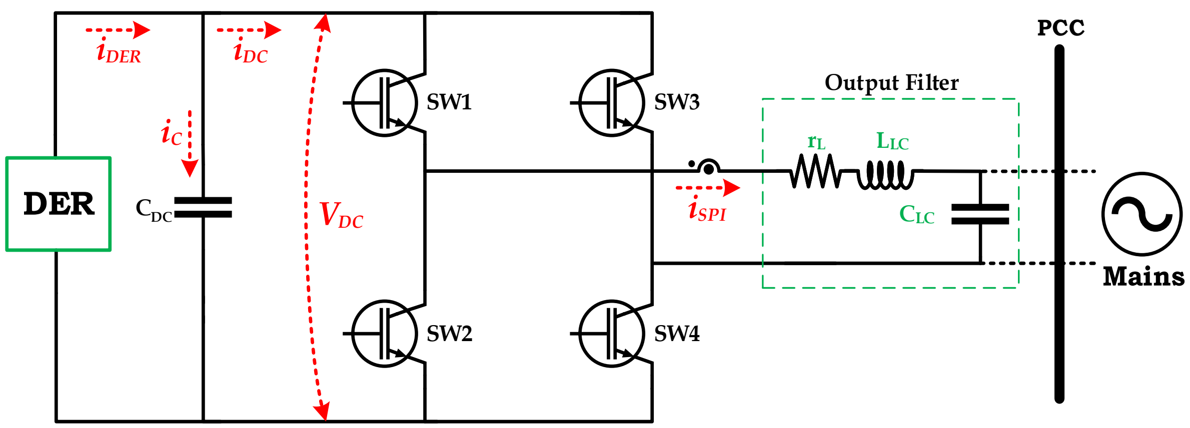


Figure 3 – General full-bridge inverter topology for DERs.

goal of the application, VSIs are employed by adopting a capacitor in its DC side. On the opposite, when an inductor is placed at the DC side of the inverter, current control is usually targeted. Besides the fact that CSIs are tied to inconveniences related to higher switching losses and disadvantages by energy storage through inductors (ROUTIMO *et al.*, 2007), VSIs can also be efficiently used for current control (VASQUEZ *et al.*, 2013).

Additionally, VSIs have been more adopted since control techniques were able to provide reliable simultaneous voltage and current control (BROD; NOVOTNY, 1985; BUSO *et al.*, 1998). It is important to highlight that, despite the literature definition of VSIs, here they are said to operate as current source, when the main controlled quantity is the output current through the inductor of LC output filter, whereas are named to operate as voltage source when the voltage across the capacitor of LC output filter is controlled.

Beforehand, for the development of the next sections, some fundamental explanations must be given regarding the electrical features of a few elements considered on simulations, and also on part of the future experimental work developed. The reason of this early explanation is due to the fact that such circuit conditions will be taken as orientation for the design of SPIs and as background for quantitative and qualitative analyses of their later discussed operation and control methodologies. Therefore, an ideal testbed is proposed for the use in the discussions of Chapters 3 and 4.

3.2 Testbed for Simulations and Initial Considerations for the Design of SPIs

Initially, the testbed is presented in Fig. 4, comprising a single-phase circuit, with AC voltage source, line impedance, and a SPI (being represented by an ideal controlled current source) in parallel with a nonlinear load. Following the intended approach of power quality evaluation in single-phase low-voltage networks, it is mandatory to appropriately constitute a system with reactive and harmonic distorted characteristics. Hence, led by the availability of physical loads at the laboratory where experiments are expected to be held, from now on, an arrange of loads, forming a nonlinear piece, will be majorly considered as the most used element on evaluated circuits.

Such nonlinear load is composed by a RL load ($1.502 + j15.079\ \Omega$), in parallel with a diode rectifier, containing an inductor ($L_L = 5mH$) in its AC side, feeding a resistive load ($R_{RC} = 16\Omega$) in parallel to a capacitor ($C_{RC} = 2.35mF$) at the DC side. Concerning grid conditions, for now, the mains is considered as a sinusoidal voltage supply, with nominal value of $V_g = 127V$ and frequency equals to $f_g = 60Hz$, under a line-neutral topology. Once the target is low-voltage networks, a more resistive behavior (high R/X ratio) of line impedance (LI; KAO, 2009) is selected.

Disregarding the line impedance ($Z_L = 0\Omega$) and SPI at this moment, to facilitate the

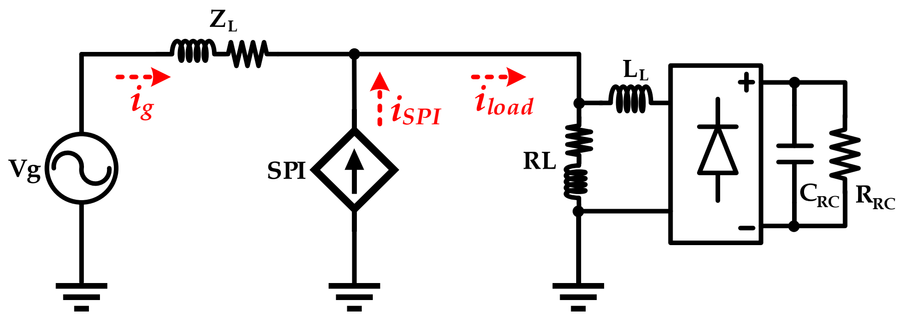


Figure 4 – Testbed circuit for testing design parameters of SPIs.

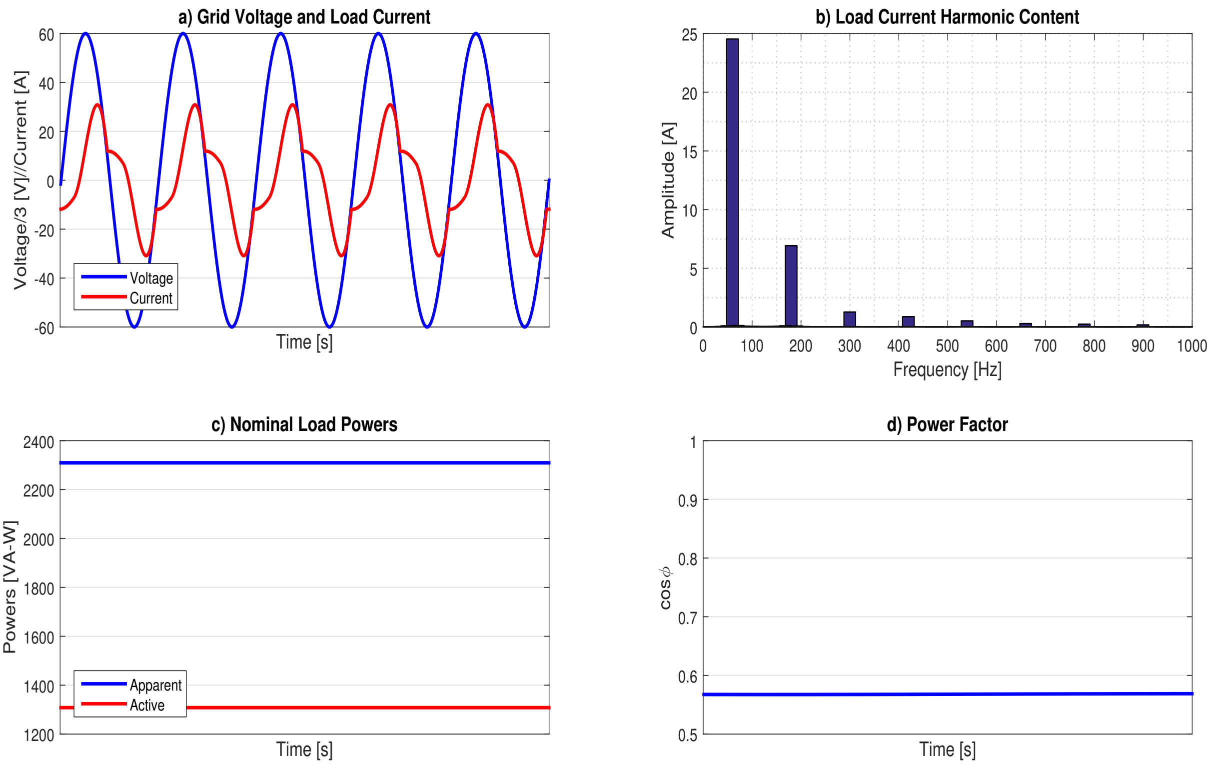


Figure 5 – Characteristics of the grid and load conditions.

understanding of the circuit's electrical features, as shown in Fig. 5-a, a simulation presents the nonlinear behavior of the current drawn by this chosen load. Further looking into its current spectrum, demonstrated in Fig. 5-b, one can see the composition of its harmonic content, which in that case, consists of most considerable odd harmonics orders from the 3rd up to the 13th. It can be said in advance here that, for later practical purposes, since the amplitude of some harmonic frequencies is significantly low in comparison to the fundamental one, some of the power quality interventions proposed in this work take into consideration only fewer orders.

By further exploring the load's current and voltage, even more information about its behavior can be extracted. It is shown in Fig. 5-c that, in a steady state condition and under pure sinusoidal grid voltage support, the load has nominal active power of approximately $P_{load} = 1.3kW$, draining as well an amount of $A_{load} = 2.3kVA$ of apparent power. As a result of such power demand, a power factor of $PF_{load} = 0.56$ is calculated. Once grid and load conditions are slightly better understood, sequence can be given in Section 3.3, showing the meaning of possessing such information with intention of designing a full-bridge single-phase inverter.

3.3 Initial Considerations for the Design of Inverters

Full-bridge voltage source multifunctional SPIs are, herein, the main elements used as power conditioners. Therefore, their design, control and operation must be well described, in order to effectively consolidate the ideas brought on the harmonic power sharing methodology in this work. An interesting fact about distributed networks is their capability of integrating many different DGs, with very particular power ratings and energy generation capabilities. As consequence, due to organization purposes, a design example for a single inverter rating is presented in the following discussions.

For beginning the design of a multifunctional grid-connected SPI, some electrical parameters must be determined, and for the sake o simplicity, the features of the previously explained nonlinear load are chosen as reference. Making the assumption that the inverter is supposed to fully support the load nominal apparent power demand, its apparent power (A_{SPI}) is said to be equal to the load rating, resulting in eq. (3.1). Note that this consideration is taken aiming at showing the SPI functionalities related to active and non-active current injection. In more realistic applications, the capability of a multifunctional VSI is given by the apparent power of the DER present at its DC side. Another important highlight is that, upon the presentation of the hierarchical control approach proposed in this dissertation, which is modeled based on current capabilities, the nominal power processed by the SPI (A_{SPI}) is translated into a feature of current quantity ($I_{SPI} = I_{nom}^{ft}$).

$$\begin{aligned} A_{SPI} &= A_{load} \\ A_{SPI} &= 2300 \text{ VA} \end{aligned} \tag{3.1}$$

Also, as good practice, it is advisable to consider an extra power rating amount due to safety matters. Therefore, considering that the SPI should support an additional power effort of $coef_{saf} = 30\%$ of its nominal load, the maximum apparent power is given by eq. (3.2).

$$\begin{aligned} A_{SPI}^{max} &= (1 + coef_{saf}) \cdot A_{SPI} \\ A_{SPI}^{max} &= 2990 \text{ VA} \end{aligned} \tag{3.2}$$

The full-bridge (two legs) topology has a DC link with a supporting capacitor (C_{DC}) that needs to be well designed to cope with the overall power capabilities of the converter. For instance, such capacitor is required to storage enough energy to, at least, instantaneously support voltage peak demands. Having that in mind, additionally, it is also commonly consented in SPI designs to take into consideration a safety measure appropriated to the application (ESPINOZA, 2011). Considering such requirement, a 30% level is to be considered as well in this case, then satisfying the following DC voltage condition of eq. (3.3) (BRANDAO, 2013).

$$\begin{gathered}
V_{DC} = V_g^{peak} \cdot (1 + coef_{saf}) \\
V_{DC} = 127 \cdot \sqrt{2} \cdot 1.3 \\
V_{DC} = 233.48 \text{ V} \\
V_{DC} \approx 235 \text{ V}
\end{gathered} \tag{3.3}$$

For the goal of having a multifunctional inverter, the capacitor (C_{DC}) should store enough power to support dynamic variations of load and grid. In other words, this energy should support the SPI when operating as APF, DG or both together. Yet, considering those possible applications, it is highly relevant for this capacitor not to present voltage ripple that could affect the desired voltage and current outputs. Therefore, just a small amount of $V_{ripple} = 3\%$ is designed to be allowed. Although additional control loops (KOTSOPOULOS *et al.*, 2003; CHEN *et al.*, 2008) or DC-link filter topologies (IYER; JOHN, 2015) may be further implemented for maintaining a steady state capacitor output voltage without practical ripple, they add complexity to the design of SPIs. Therefore, also considering that the herein allowed voltage ripple value (V_{ripple}) is not critical for the intended applications of this work, a general design model for the DC link capacitor is taken (BRANDAO, 2013), resulting in eq. (3.4), where $\Delta V_{DC} = V_{ripple} \cdot V_{DC}$. More details on the steps for attaining eq. (3.4) are present in (ZONG, 2011).

$$\begin{gathered}
C_{DC} > \frac{A_{SPI}^{max}}{2 \cdot \pi \cdot f_g \cdot V_{DC} \cdot \Delta V_{DC}} \\
C_{DC} > \frac{2990}{2 \cdot \pi \cdot 60 \cdot 235 \cdot 0.03 \cdot 235} \\
C_{DC} > 1.125\ mF \\
C_{DC} \approx 1.2\ mF
\end{gathered} \tag{3.4}$$

Another physical SPI feature that needs to be determined is the switching frequency, which is related to the modulation periods of the voltage power source at its DC side. Usually, low to medium power inverters employ IGBTs as switches, and as any other electrical component, they present limited electrical features and power rating. Since at the future it is aimed experimental procedures, for now, it is considered a general model of transistor, with commonly used switching frequency of $f_{sw} = 12kHz$. Yet, since the switching control of these components are usually digitally implemented, the sampling frequency (f_s) of measurements should be higher or at least equal to f_{sw}. Here f_s is chosen to be $2 \cdot f_{sw}$ aiming to obtain more precise results, as explained in sequence in the PWM model. The most relevant specifications and definitions for the grid, load and SPI, are summarized in Table 1.

Table 1 – Grid, load and inverter specifications.

Nonlinear Load	
Feature	**Specification**
Nominal current (I_{load})	18.07 A
Peak current (I_{load}^{peak})	30.85 A
Nominal Power (P_{load})	1300 W
Inverter	
Feature	**Specification**
Nominal apparent power (A_{SPI})	2300 VA
Maximum Apparent power (A_{SPI}^{max})	2990 VA
DC link voltage (V_{DC})	235 V
Switching frequency (f_{sw})	12 kHz
Sampling frequency (f_s)	24 kHz
Factor of safety ($coef_{saf}$)	30 %
DC link voltage ripple (V_{ripple})	3 %

3.4 PWM Model

Pulse Width Modulation (PWM) is one of the most adopted alternatives regarding the generation of digital control commands for power converter switches (e.g. SW1, SW2, SW3 and SW4), allowing synthesized voltage and current outputs to track a desired behavior. Among many alternatives of PWM techniques (HOLMES; LIPO, 2003), the sinusoidal PWM (SPWM) provides an efficient way of making its output, which are digital pulsed signals, to fairly track time variant references. The creation of these digital pulsed outputs is accomplished by comparing a reference signal with a carrier wave, which usually is defined to follow a triangular or sawtooth pattern.

As simple as in an analog comparison, as represented in Fig. 6-a, the instantaneous differential value between the modulating signal and carrier wave amplitude is responsible for determining the high or low state of each of the inverter's switches. Retrieving the full-bridge topology of Fig. 3, for instance, setting SW1 and SW4 high at the same moment, a voltage output of $+V_{DC}$ is achieved, and similarly, by making SW3 and SW2 high, allows the inverter to create $-V_{DC}$. This approach is therefore, defined as a two-level, or bipolar, PWM.

The difference between the abovementioned modulation and a three-level one, which is also called unipolar, consists in generating as output, three voltage states instead of two, which are $+V_{DC}$, 0, and $-V_{DC}$, as seen in Fig. 6-b. For this case, however, having the first leg of the inverter controlled by a sinusoidal reference, it is expected a 180º phase shift in such reference to control its second leg switches, as shown in Fig. 6-c. Focusing on DC-AC converters, the main advantage of adopting unipolar modulation is the reduction on the total harmonic content generated by the inverter switching. That improvement on harmonic level is due to the ability of this technique to provide the elimination of even multiple harmonic frequencies of the switching

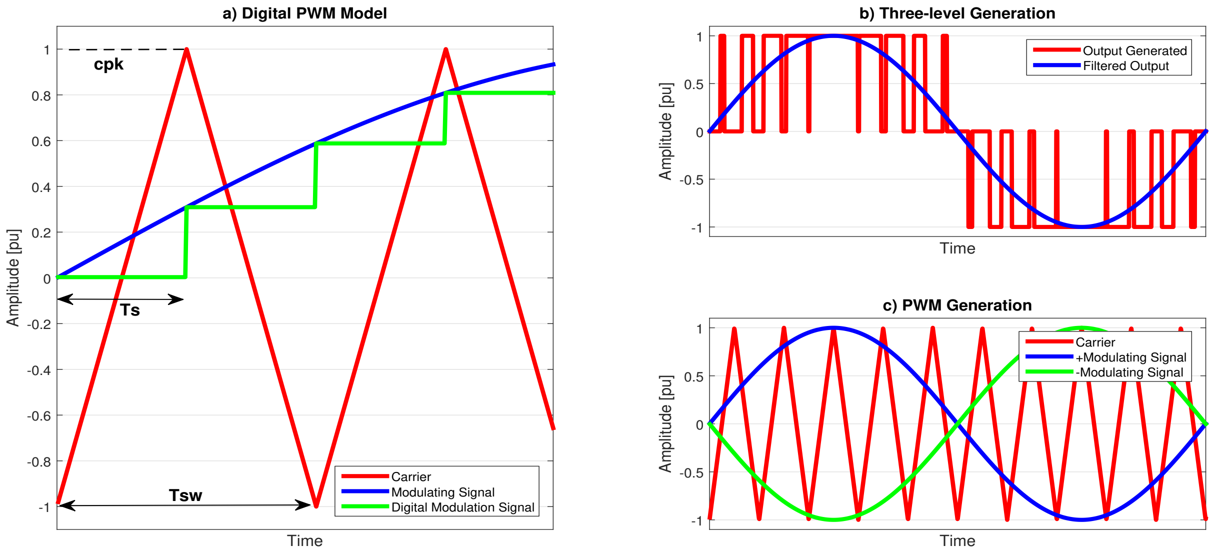


Figure 6 – Three-level modulation and triangular carrier small signal modeling.

frequency (ESPINOZA, 2011), directly minimizing the design of filtering components.

For the mentioned analog comparison of the unipolar generation, a small signal analysis is conducted aiming to achieve a PWM duty cycle model. Furthermore, for such development, it is considered herein the use of a triangular carrier with peak amplitude of c_{pk}, being compared with a modulating signal $m(t)$. Under assumption of $m(t)$ slowly changing along time, which is reasonable in comparison with the much greater carrier frequency f_{sw}, the duty cycle $d(t)$ of the PWM modular is given by eq. (3.5) (BUSO; MATTAVELLI, 2006).

$$\begin{aligned} \frac{m(t)}{d \cdot T_{sw}} &= \frac{c_{pk}}{T_{sw}} \\ d(t) &= \frac{m(t)}{c_{pk}} \end{aligned} \tag{3.5}$$

Thus, by using the Laplace transform, the following transfer function given in eq. (3.6) is achieved for the PWM modulator.

$$\frac{D(s)}{M(s)} = \frac{1}{c_{pk}} \tag{3.6}$$

In its discretization process, (BUSO; MATTAVELLI, 2006) mentions that such PWM model may be represented by the static gain in eq. (3.6) and its respective delay effect, which therein is represented by a first-order Padé approximation. Another relevant matter to highlight is the discussion regarding the synchronization of PWM switching frequency in relation to the sampling frequency of the discrete modulating signal. For the case of a triangular carrier in a three-level scheme, the double-update mode shown in Fig. 6-c is advisable for reducing phase lag of the digital PWM modulator, resulting in $f_s = 2 \cdot f_{sw}$ and making eq. (3.6) to be half of its value. This is done by updating compare registers twice in a modulation period. Therefore, considering the same triangular carrier with peak unitary amplitude c_{pk}, the digital PWM model in a double-update mode results in eq. (3.7).

$$PWM(s) = \frac{1}{2 \cdot c_{pk}} \cdot \frac{1 - s \cdot \frac{T_{sw}}{4}}{1 + s \cdot \frac{T_{sw}}{4}} \tag{3.7}$$

3.5 Output LC Filter

PWM controlled SPIs present characteristic pulsed voltage as output of their operation. That is an undesirable feature considering a needed reliable interactivity with grids, which demands compliance with requirements regarding harmonic distortion and sinusoidal frequency and phase synchronization. Thus, filtering such synthesized voltage and current outputs to comply with standards becomes crucial. Passive filters under many possible topologies have been proposed for that purpose, and have also been employed along with virtual and active damping techniques (WANG *et al.*, 2016; LISERRE *et al.*, 2004).

Among the mentioned passive filter topologies (BERES *et al.*, 2016), the two most consolidated in the literature are the LC and LCL filters. Although LCL filters have the advantage of providing a very efficient filtering conditions for grid-tied inverters (REZNIK *et al.*, 2014), it has the drawback of impacting control instability conditions of SPIs. That occurs since it adds one more pole to the system's transfer function, resulting in the need for a more robust control approach.

With the goal of controlling inverters as current sources, LC filters are interesting because they act as low-pass filters, retaining high frequency content above a desired cut-off frequency. In addition, the modeling of an LC filter leads to a second order transfer function, providing more facilitated control design with single or three-phase inverters than LCL topologies. Therefore, considering such characteristics, a LC filter has been adopted for the integration with the modeled VSIs.

For the design of the proposed LC filter, it is required to define some following acceptable conditions of its operation (SOUZA; BARBI, 2000), which for this case, are summarized in Table 2. The inductor of the filter needs to be designed for adequate current attenuation. It should be capable of constraining a maximum peak current supposed to flow through it, taking into consideration the given acceptable ripple percentage. For that, the inverter switching frequency must be accounted, since as a consequence of it, the current changes ($\frac{di_{SPI}}{dt}$) occur during fixed periods as well, given by $T_{sw} = 1/f_{sw}$. Besides, reminding that a maximum allow-

Table 2 – LC filter specifications.

Feature	Specification
Current ripple (ΔI_{LC}^{ripple})	5%
Reactive inductance (r_L)	$10\% \cdot X_{L_{LC}}$
Capacitor resonance (f_C^{res})	$(f_{sw}/10)\ Hz$

able current ripple value has to be attended, the current efforts should respect eq. (3.8).

$$\frac{di_{SPI}}{dt} \leq I_{SPI}^{peak} \cdot \Delta I_{LC}^{ripple} \tag{3.8}$$

Yet, as stated by (PRAKASH *et al.*, 2016), for a three-level PWM modulations, the maximum current (I_{SPI}^{pk}) flowing through the inductor may be given by eq. (3.9).

$$I_{SPI}^{peak} = \frac{2 \cdot A_{SPI}^{max}}{Vg \cdot \sqrt{2}} \tag{3.9}$$

$$I_{SPI}^{peak} = \frac{2 \cdot 2990}{127 \cdot \sqrt{2}} = 33.29A$$

Considering a three-level PWM with triangular carrier, the equation (3.10) allows the calculation of the inductor of the LC filter. It represents the condition in which the current limits are complied with a given inductor (SOUZA; BARBI, 2000), where $\overline{\Delta I_{SPI}}$ is a parametrized value, being equal to 0.25 for this modulation approach. The inductor design in such model regards to the current synthesized in each switching period of the converter (T_{sw}), accounting for the requirement of attaining a filtered current that do not exceeds a maximum threshold (I_{SPI}^{peak}) and also presents ripple value lower than ΔI_{LC}^{ripple}. An extensive explanation about eq. (3.10) is presented in (SOUZA; BARBI, 2000). As previously determined in Section 3.3, it is taken as consideration the design of a SPI fully supplying the load demand, which means that the maximum current flowing through the inductor is the peak demand of the load plus a safety quantity.

$$L_{LC} \geq \frac{\overline{\Delta I_{SPI}} \cdot V_{DC}}{2 \cdot f_{sw} \cdot I_{SPI}^{peak} \cdot \Delta I_{LC}^{ripple}} \tag{3.10}$$

$$L_{LC} \geq \frac{0.25 \cdot 235}{2 \cdot 12000 \cdot 33.29 \cdot 0.05}$$

$$L_{LC} \geq 1.47\ mH$$

$$L_{LC} \approx 1.5\ mH$$

When modeling this inductor, it is also important to take into consideration its aggregated resistance, which here is considered to be 10% of the respective value of L_{LC} at the fundamental frequency of $60Hz$.

$$r_L = 0.1 \cdot w_{LC} \cdot L_{LC}$$

$$r_L = 0.1 \cdot 2 \cdot \pi \cdot f_g \cdot L_{LC}$$

$$r_L = 0.1 \cdot 2 \cdot \pi \cdot 60 \cdot 1.5mH$$

$$r_L = 0.056\ \Omega$$

Continuing with the design of the capacitor of the LC filter, an extremely relevant fact to be considered is the selectivity of the filter. Sufficient attenuation of undesired frequencies should occur, though not causing any impact on the controller bandwidth. Having that in mind, it is advisable to select a cut-off frequency for the filter in order to avoid overlaying with the controller passing band. For this particular case, retrieving the load harmonic content of Fig. 5-b, since the controller is intended to possibly account for a current content up to the 13th (780 Hz) harmonic, a passing band (f_{sw}/10) would be appropriate (CHA; VU, 2010; HOJABRI; HOJABRI, 2015).

With such considerations, it is here adopted a resonance frequency for the capacitor (f_C^{res}) equal to 1.2 kHz. Besides, knowing that the resonance of a LC element may be defined by eq. (3.11), through some manipulation, the capacitance that needs to be selected to maintain the filtering capability is determined, leading to eq. (3.12) and resulting in the following C_{LC}.

$$\omega_C^{res} = \frac{1}{\sqrt{L_{LC} \cdot C_{LC}}} \tag{3.11}$$

$$\begin{aligned} C_{LC} &= \frac{1}{(\omega_C^{res})^2 \cdot L_{LC}} \\ C_{LC} &= \frac{1}{(2 \cdot \pi \cdot f_C^{res})^2 \cdot L_{LC}} \\ C_{LC} &= \frac{1}{(2 \cdot \pi \cdot 1200)^2 \cdot 1.5mH} \\ C_{LC} &= 11.72\ \mu F \end{aligned} \tag{3.12}$$

Having designed the LC components, and knowing that it responds as low-pass filter with transfer function given by eq. (3.13), its frequency response can be evaluated aiming at confirming its effectiveness. From Fig. 7 it can be seen how filter gives a significant high gain at the designed resonance frequency ($f_C^{res} = 1.2kHz$). In frequencies higher than f_C^{res}, it can be noted the attenuation behavior of the filter, presenting a passing band of $1.87kHz$, which is adequate for the operation of the inverter since it does not suppress the approximate bandwidth of $1.2kHz$ of the later discussed current controllers.

$$H_{LC}(s) = \frac{\frac{1}{L_{LC} \cdot C_{LC}}}{s^2 + \frac{r_L}{L_{LC}} \cdot s + \frac{1}{L_{LC} \cdot C_{LC}}} \tag{3.13}$$

Once all the filter parameters have been determined, the investigation of other ideas employed on the model, design and control of current controllers may be discussed.

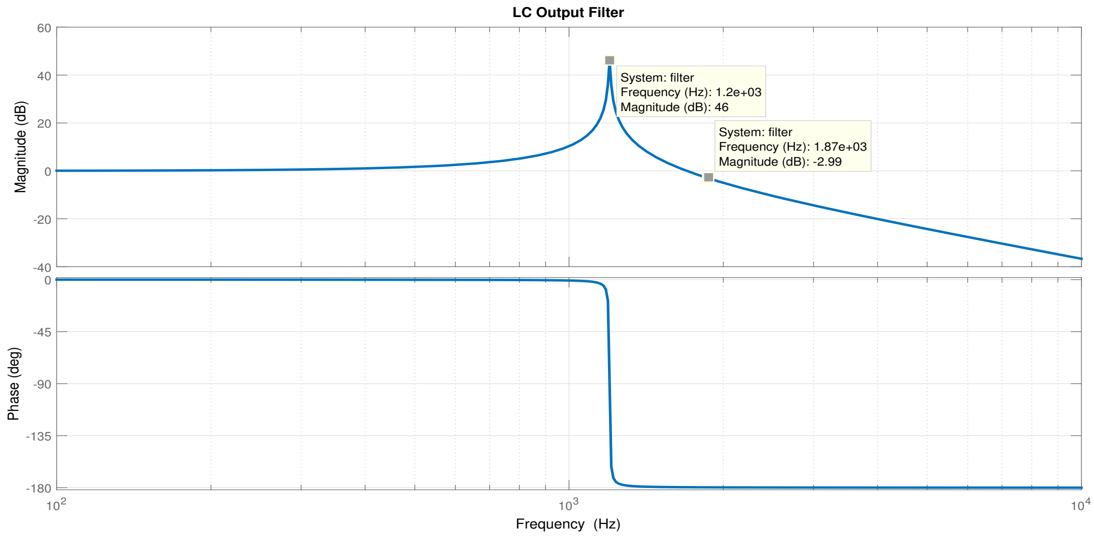


Figure 7 – Frequency response of the LC filter.

3.6 Synchronization by Phase-Locked Loop Algorithm

Due to possible several detrimental electrical consequences of improper frequency and phase matching between inverter and grid voltages, such as grid's nominal frequency deviation and others issues (JAALAM *et al.*, 2016), algorithms for grid integration of DC-AC converters are critically needed in DERs. Their operation is highly required in primary control schemes to avoid impairment of frequency, phase and amplitude features of voltages and currents, especially if the the grid presents unbalanced or distorted conditions. Many methodologies for those synchronization algorithms have been proposed and were widely discussed in literature (PADUA *et al.*, 2007; NEVES *et al.*, 2010; GOLESTAN *et al.*, 2017), showing advantages and constraints regarding many circumstances.

For the primary level synchronization of the proposal presented in this work, a natural frame algorithm based on a phase-locked loop (PLL) methodology is adopted, due to its simplified design and implementation, and also because of its robust response under non-sinusoidal conditions (MARAFAO, 2004). Following a structure as reported in Fig. 8, such synchronization algorithm works on the phase detection of an input signal (x) by adjusting its synthesized orthogonal signal ($x_\perp$). By multiplying these two signals, their dot product (d_p) is generated, becoming a quantity that should present a null mean value in steady state instants. This mean value calculation may be, for instance, implemented by means of a moving average filters (MAF), providing an output that can be compared for the creation of an error value (ε_{dp}).

MAFs are a particular approach of finite impulse response (FIR) filters, operating as a low-pass selector that smooths a time-domain input signal ($y(t)$) according to the number of elements (M) in an array used on its digital implementation (SMITH, 1998). Such filters are represented in discrete domain as shown in eq. (3.14), being herein implemented by means of a fixed size circular buffer (BRANDAO; MARAFAO, 2016) with window equal to $M = f_s/60$ elements. The use of MAFs with fixed or adaptive (DESTRO *et al.*, 2013; MARAFAO *et al.*,

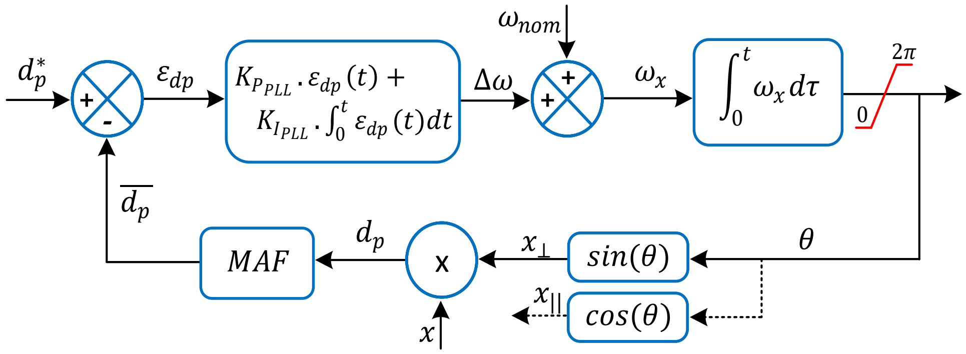


Figure 8 – Phase-locked loop block diagram.

2004a) windows have been extensively used for PLL purposes, mainly due to its simplicity for digital implementation and robustness under distorted input signal condition (GOLESTAN *et al.*, 2014; HAN *et al.*, 2016b). Nevertheless, depending on its implementation method, some constraints related to the use of MAFs stand in regard of slow convergence times, reduced noise immunity and possible incapability to reject disturbances (GOLESTAN *et al.*, 2014).

$$\frac{y(z)}{x(z)} = \frac{1}{M} \cdot \frac{1 - z^{-M}}{1 - z^{-1}} \tag{3.14}$$

Retrieving the explanation of the chosen PLL methodology in this work, the dot product reference (d_p^*) is set to be zero, by relating to the mathematical affirmation of obtaining a null value when two orthogonal signals are multiplied. Thus, the goal for a null ε_{dp} is sought by a proportional-integral (PI) regulator, which has as output an angular frequency correction (Δw) for the frequency base (w_x) of $x_\perp$. The integration of w_x provides the tracking of the phase angle θ that is locked for the converter synchronization. Though it has been discussed here a single-phase approach, by adjusting extra loops with symmetrical lagging phase angles, this synchronization method could be extended to three-phase topologies as well (MARAFAO, 2004).

To give an overview of the operation of the adopted PLL methodology, it is first required to design the PI regulator responsible for the correction of the error ε_{dp}. For that, we assume a general PI controller, with proportional and integral gains defined to be, respectively, $K_{P_{PLL}}$ and $K_{I_{PLL}}$. As stated by Marafao (2004), the PI ought to be designed aiming a slow dynamic behavior, in a way that the entire closed loop system presents a crossover frequency w_n of around 5-10 Hz. Herein, $10Hz$ is chosen for the PLL controller design. Yet, since this PLL methodology may be reasonably represented as second order transfer function ($H_{PLL}(s)$), it can be defined by eq. (3.15).

$$\begin{aligned} H_{PLL}(s) &= \frac{2\xi \cdot w_n \cdot s + w_n^2}{s^2 + 2\xi \cdot w_n \cdot s + w_n^2} \\ H_{PLL}(s) &= \frac{K_{P_{PLL}} \cdot s + K_{I_{PLL}}}{s^2 + K_{P_{PLL}} \cdot s + K_{I_{PLL}}} \end{aligned} \tag{3.15}$$

Moreover, consequently, resulting in controller gains given by eq. (3.16) and eq. (3.17).

$$K_{P_{PLL}} = 2\xi \cdot w_n \tag{3.16}$$

$$K_{I_{PLL}} = w_n^2 \tag{3.17}$$

Considering the supposed controller conditions just mentioned, both the proportional and integral gains can be calculated as follows.

$$K_{I_{PLL}} = (2 \cdot \pi \cdot 10)^2$$
$$K_{I_{PLL}} = 3947.83$$
$$K_{P_{PLL}} = 2 \cdot 1 \cdot 2 \cdot \pi \cdot 10$$
$$K_{P_{PLL}} = 125.66$$

Carrying out simulations with PSIM, the proposed PLL was implemented and tested to effectively operate under a non-sinusoidal grid condition. In such case, the PLL is supposed to generate an unitary sinusoidal signal that follows the fundamental component of a distorted voltage reference, for instance, as in an analogy of real application cases of grid-tied inverters. This distorted grid voltage condition was simulated as a fundamental component with nominal value $V_{1_{rms}} = 127V$, additionally with 8% and 12% of, respectively, fifth and seventh harmonics.

From the results presented in Fig. 9 one can note that the PLL is able to adequately track the phase of the distorted reference and lock it to generate an orthogonal signal, from which others may be generated as well. Fig. 9-a and c show the normalized grid voltage and the PLL in-phase and orthogonal signals synthesized from its orthogonal phase reference. It is reinforced that the synchronism angle θ is a quantity evaluated between $0 - 2\pi$, although presented normalized as well. In Fig. 9-b it is shown the frequency of the PLL being locked at the grid nominal frequency. Also, as it is depicted in Fig. 9-d and e, since the PLL synthesizes unitary in-phase and orthogonal signals, any other multiple order terms are possible to be generated as well, in respect to phase, frequency or amplitude. This is a very interesting feature, once it could be used on the adequacy of control references for multifunctional SPIs, providing flexible power quality interventions (BRANDAO *et al.*, 2016).

By concluding the explanation related to the methodology and operation procedures of the chosen synchronism algorithm, discussions can evolve to another undeniably important matter for power converters, which is the implementation of voltage and current controllers.

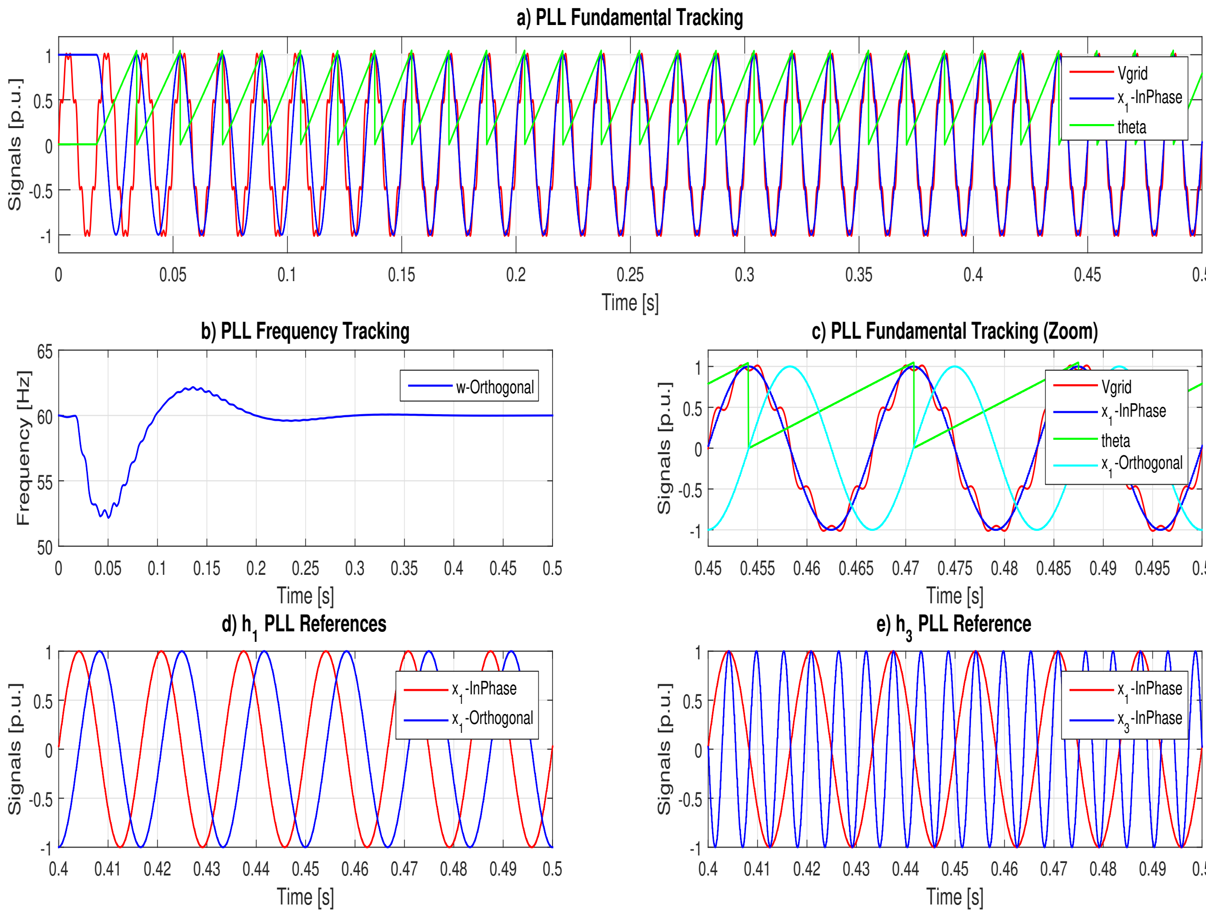


Figure 9 – Phase-locked loop simulation.

3.7 Transducers

Before explaining how current and voltage controllers can be designed, it must be said that they rely on the measurement of sensors spread over their circuits. Although this sensoring is fundamental for the design and adequate operation of inverters, the quantities acquired on current and voltage measurements, usually, cannot be directly used on such operations. That occurs due to the fact that controllers of such inverters are digital and electronically implemented, presenting in the most general cases, analog-to-digital (ADC) converters as interfaces for the input measurements. ADCs, however, typically deal with signals within a range of 3-5 volts, becoming necessary the use of signal conditioners.

For this purpose, current and voltage transducers are highly employed, and operate giving gain values on sensor measurements, making such quantities readable by ADCs, being commonly used as per unit (p.u.) values. Therefore, since p.u. signal feedback loops are essential in the control of converters, transducer gains must be considered on the modeling of power converter systems. In this work, four quantities are used for the right operation of an inverter. These quantities are the inverter and load currents, and also the voltage of inverter nodes and their DC link voltages.

Regarding currents, it has been shown that, considering the example of the earlier discussed nonlinear load, the maximum supposed peak current of the inverter, considering a safety quantity, would be $I_{SPI}^{peak} = 33.29A$. With such value, in order to make the output of the transducer always fit a p.u. range, which is between 0 to 1, its gain (K_i) is considered for the current measurements as defined by eq. (3.18). Note that, when an experimental approach is considered, this (K_i) value represents the gain given by hall sensors used for acquiring the physical measurements and also considers the handling provided by a signal conditioning board, which already incorporates physical anti-aliasing filters. More details on the signal conditioning hardware is seen in (SOUZA, 2016).

$$K_i = \frac{1}{50} \tag{3.18}$$

Likewise, the AC voltage transducers (K_{VAC}), respective for the grid and other nodal AC measurements, as well as the DC link voltage one (K_{VDC}), can be attained by eq. (3.19) and eq. (3.20). Both of these transducer gains are chosen to avoid saturation of the sensors and signal conditioning scheme, even under short transient periods in which such voltages may reach values higher than the expected nominal features. To facilitate the understanding about the real implementation of such transducer gains, in Fig. 10 is shown an experimental example where an AC voltage signal is measured with a hall sensor and processed on the signal conditioning board. Note that, having an input voltage signal (v_{real}) with peak amplitude of practically $300V$, the output of the system (v_{adc}), which may therein be used in the ADC of a digital signal processor (DSP), presents an offset of 1.5V plus a peak-to-peak value of practically 1.5V (entirely fitting within the physical 0-3V range of the ADC).

$$K_{VAC} = \frac{1}{300} \tag{3.19}$$

$$K_{VDC} = \frac{1}{500} \tag{3.20}$$

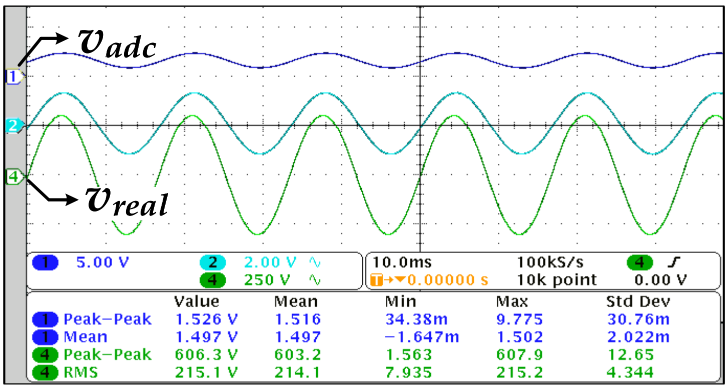


Figure 10 – Experimental example of practical implementation of transducer gains.

3.8 Single-phase Inverter Control Model

To consider the possibility of controlling the voltage and current generated by an inverter, firstly, it is fundamental to understand how these outputs are synthesized considering the entire system, from the generated power coming from a DER, up to the coupling of the LC filter to the grid. In advance it is worth mentioning that the inverter is herein modeled as a multi-loop system, in which there is an inner fast-dynamic loop for current control function, and another outer slow-dynamic loop that takes responsibility of the output DC voltage control.

Initially, aiming at current control, and recalling the circuit of Fig. 3, it can be noted that the instantaneous output voltage (v_p) of the SPI, which pulses based on the DC link voltage (V_{DC}), having a LC output filter, is given by eq. (3.21). Since it is considered herein that the current signal used as reference for the feedback control loop is measured before the capacitor C_{LC}, this last is not considered in the transfer function at this moment. Another simplification considered is that the grid is absent (i.e., stand-alone inverter) (BRANDAO, 2013; ALGADDAFI, 2016; MORTEZAEI *et al.*, 2016), resulting in $v_{pcc} = 0$.

$$v_p(t) = r_L \cdot i_{SPI}(t) + L_{LC} \cdot \frac{di_{SPI}(t)}{dt} + v_{PCC} \tag{3.21}$$

Furthermore, taking advantage of the Laplace transformation (OGATA, 2001), eq. (3.21) can be modeled in frequency domain, resulting in the representation of the SPI current transfer function ($G_i(s)$) represented by eq. (3.22).

$$\begin{aligned} V_p(s) &= r_L \cdot I_{SPI}(s) + L_{LC} \cdot s \cdot I_{SPI}(s) \\ G_i(s) &= \frac{I_{SPI}(s)}{V_p(s)} = \frac{1}{L_{LC} \cdot s + r_L} \end{aligned} \tag{3.22}$$

Considering the parameter values, the SPI would therefore be represented by eq. (3.23).

$$G_i(s) = \frac{1}{(1.5 \cdot 10^{-3}) \cdot s + 0.056} \tag{3.23}$$

Even knowing how the SPI interacts with the LC filter, for the modeling of the entire control system, three more elements should be considered. They are, respectively, the gain of the inverter (V_{DC}), the PWM model discussed in Section 3.1., and the controller employed on each loop for an adequate operation of the inverter. The PWM is driven by the modulated signal (m) that is defined by the current controller ($C_i(s)$), which operates trying to minimizing the error (e_i) created by the difference between the desired current value (i^*) and the actual output current synthesized ($i^{"}_{SPI}$).

The inner current loop of the SPI is then determined by the block diagram presented in Fig. 11, where "d" stands for the duty cycle generated by the PWM regulator, and "K_i" is the current transducer gain. Note that, since a transducer is considered in this plant, the current reference (i^*) must be handled as a p.u. value.

Now, focusing on the outer loop of the SPI control model and retrieving Fig. 3, one can note that the current available for the DC-AC conversion (i_{DC}) is supported by the DC link capacitor and the DER. In general, when single-phase SPIs are modeled to operate as DGs, their

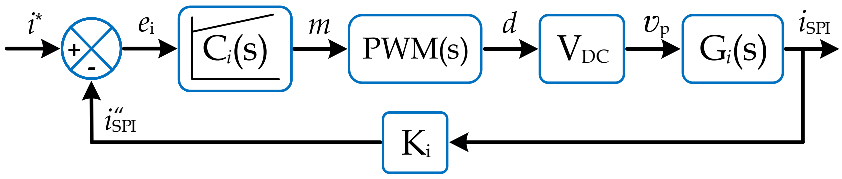


Figure 11 – Block diagram for the inner current control loop of the SPI.

DC link voltage is controlled by DC-DC converters with MPPT methodologies (KJAER *et al.*, 2005; BRANDAO *et al.*, 2013), thus the DC link voltage is considered constant for the SPI. However, when power generation is not available at the DER (i.e., $i_{DER} = 0$), the outer voltage loop must be controlled by the SPI, such as in an APF operation (i.e., $i_C = i_{DC}$). Therefore, by analyzing the circuit for this last case, it leads to the following expression of eq. (3.24).

$$v_{DC}(t) = \frac{1}{C_{DC}} \cdot \int_0^t i_{DC}(t)dt \tag{3.24}$$

Targeting the SPI output voltage, with respect to the current provided, by using the Laplace Transform, from eq. (3.24) a formulation for the relation between voltage and current in the DC link ($G_v(s)$) is attained as in eq. (3.25).

$$G_v(s) = \mathcal{L}\left\{\frac{v_{DC}(t)}{i_{DC}(t)}\right\} = \frac{1}{s \cdot C_{DC}} \tag{3.25}$$

$$G_v(s) = \frac{1}{s \cdot (1.2 \cdot 10^{-3})}$$

Since the DC-AC conversion must handle the DC side power to the AC side as a conservative quantity, in which the power provided by the DC side is equal to the one on the AC side, we can then define the needed gain (K_{DC}) that correlates this translation on the outer loop (BRANDAO, 2013). Therefore, considering an equivalent conductance ($g_{DC} = i_{DC}/v_{DC}$) for the DC side, eq. (3.26) is achieved.

$$K_{DC} = \frac{i_{DC}(s)}{i_{SPI}(s)} \tag{3.26}$$

Relating to the mentioned apparent power conservation, meaning $A_{DC} = A_{AC}$, from eq. (3.26) it is attained eq. (3.27).

$$K_{DC} = \frac{v_{AC}}{V_{DC}} \tag{3.27}$$

To compare the generated powers at the AC and DC sides, it is considered that v_{AC} is equal to the grid rms voltage (V_{AC}) (BRANDAO, 2013), resulting in a DC static gain as follows:

$$K_{DC} = \frac{V_{AC}}{V_{DC}} = \frac{127}{235}$$

$$K_{DC} = 0.54$$

Finally, the complete closed loop control diagram of the inverter is depicted in Fig. 12. It can be noted that, as in the inner current loop, an error quantity given by the difference between the DC link voltage reference (v_{DC}^{*}) and the current voltage value generates an error signal (e_{vi}) that goes through a voltage controller ($C_{vi}(s)$), resulting in the mentioned DC side equivalent conductance. As shown in (CIOBOTARU *et al.*, 2010; YANG *et al.*, 2015), a synchronized signal (s^{*}) given by a PLL based on the grid voltage (v_{ac}) is required for the DC-AC power conservative translation, and it is simply used as a sinusoidal current synthesis reference (NUNEZ-ZUNIGA; POMILIO, 2002). Note that, as in the inner current loop, v_{DC}^{*} is a p.u. value, requiring the reference current (I^{*}) to be normalized as well, which is done by K_{VAC}. i_{inj}^{*} represents the p.u. current reference desired to be injected by the SPI into the grid, aiming at active current offering or compensation purposes (reactive and harmonic current terms).

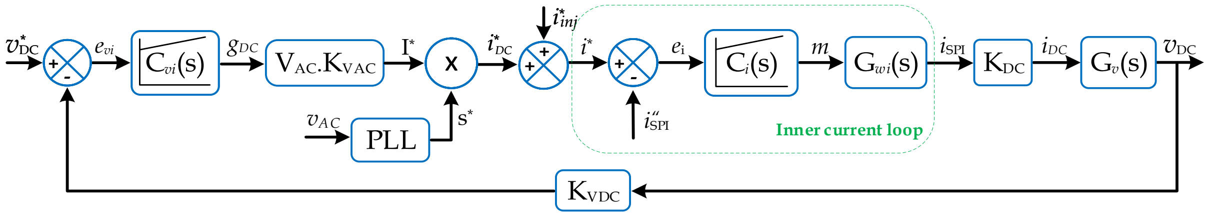


Figure 12 – Block diagram for a grid-tied VSI operating as a DG.

3.8.1 Open Loop Inverter Model

The consideration of having an inner fast-dynamic current loop, and another slow-dynamic outer loop for the DC link voltage, is important because they can be separately designed. Having previous knowledge of the particular dynamics of the inner and outer loops, the design of current ($C_i(s)$) and voltage ($C_{vi}(s)$) controllers become more accessible.

From the model shown in Fig. 11, for the inner loop and not accounting for the current controller, the open loop transfer function (G_{wc_i}) is considered by the aggregation of some respective blocks, leading to eq. (3.28). Once again, it is worth mentioning that the adopted PWM transfer function already incorporates the intrinsic delay of its digital implementation.

$$G_{wc_i}(s) = PWM(s) \cdot V_{DC} \cdot G_i(s) \cdot K_i$$
$$G_{wc_i}(s) = \left(\frac{1}{2 \cdot c_{pk}} \cdot \frac{1 - s \cdot \frac{T_{sw}}{4}}{1 + s \cdot \frac{T_{sw}}{4}}\right) \cdot V_{DC} \cdot \frac{1}{L_{LC} \cdot s + r_L} \cdot K_i \tag{3.28}$$

And considering the parameters before calculated, the open loop current transfer function is given by eq. (3.29).

$$G_{wc_i}(s) = \frac{-4.896 \cdot 10^{-5} \cdot s + 2.35}{3.125 \cdot 10^{-8} \cdot s^2 + 0.0015 \cdot s + 0.056} \tag{3.29}$$

By analyzing the frequency response of this inner loop in Fig. 13, one can observe the system presenting cut-off frequency and phase margin of approximately, respectively, $250Hz$

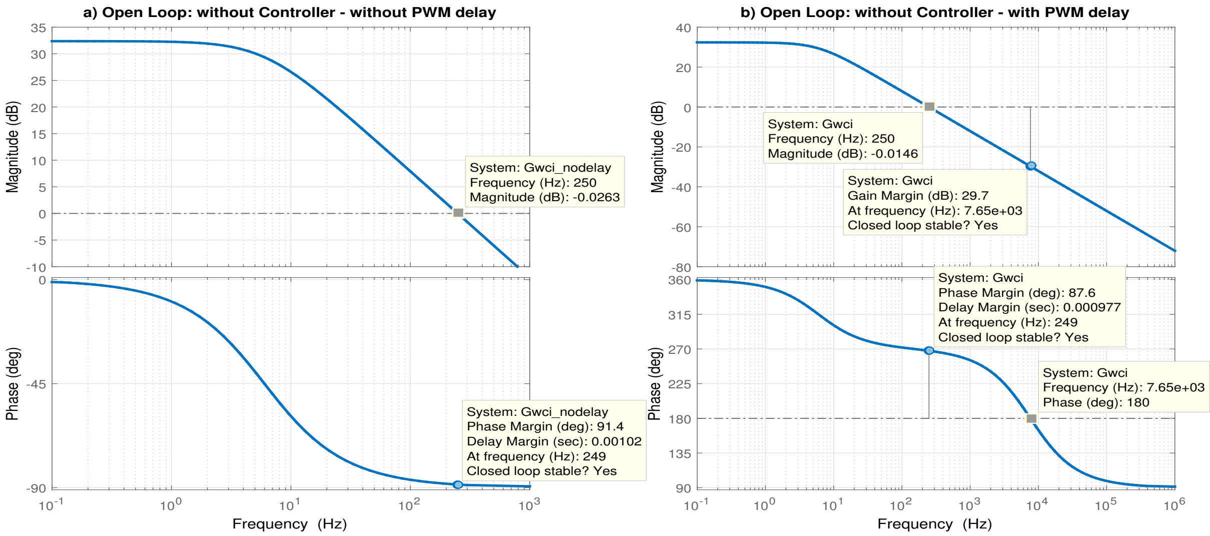


Figure 13 – Frequency response for the inner loop G_{wc_i}, disregarding (a) and regarding (b) the PWM delay.

and $90°$. Note that, if the response delay from the digital implementation of a PWM is taken into consideration, the system responds with a particular phase delay that is said to not be penalizing in closed loop stability conditions (BUSO; MATTAVELLI, 2006). Another interesting feature is that the system presents the behavior of a low pass, attenuating frequencies higher than the cut-off frequency.

Taking a similar approach, the open loop transfer function for the outer voltage loop without the controller (G_{wc_v}) is calculated. As idealized when designing the inner current loop, it is expected for $|G_{wc_i}|$ to respond like a unitary static gain loop, therefore, resulting in eq. (3.30) as transfer function for the outer control loop of the SPI. Note that, for this particular case, the inner current loop is modeled by an unitary gain in p.u. due to the use of $1/K_i$ (BRANDAO, 2013).

$$G_{wc_v}(s) = K_{VAC} \cdot V_{AC} \cdot \frac{1}{K_i} \cdot K_{DC} \cdot G_v(s) \cdot K_{VDC} \tag{3.30}$$
$$G_{wc_v}(s) = \frac{1}{300} \cdot 127 \cdot \frac{50}{1} \cdot 0.54 \cdot \frac{1}{1.2 \cdot 10^{-3} \cdot s} \cdot \frac{1}{500}$$
$$G_{wc_v}(s) = \frac{19.05}{s}$$

From Fig. 14 one can note the voltage open loop response in frequency. Note that, by having only one pole in the characteristic equation, as expected, the voltage loop does not present phase change. Yet, since its transfer function presents only one pole, it responds as a single integrator with a slope of $-20dB/Decade$.

This chapter discussed some of the most essential ideas required for the modeling and design of SPIs. The modulation technique based on a three-level PWM method provides a way of translating time variant analog signal into digital references that can be used for controlling the switches of the converters. A methodology for the adequate design of an LC filter also provides a way o interconnecting to a grid without degrading voltages and currents. Along

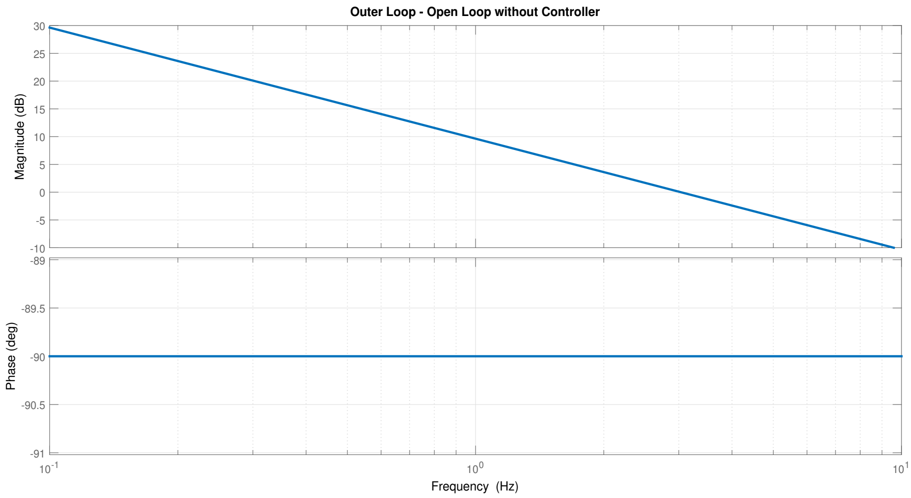


Figure 14 – Frequency response for the outer loop without controller.

with it, the PLL methodology showed how it allows a synchronized operation with the grid features. Furthermore, since the open loop dynamics of the current and voltage loops have been explained, discussions may evolve on the next chapter to the evaluation of some of the most adopted methodologies of current controllers, and one classical voltage regulation technique.

4 Design of Primary Level Controllers

In a hierarchical topology, the primary level is a fundamental layer that is responsible for the adequate operation of SPIs. Moreover, in order to do so, this layer usually relies on local controllers as means for achieving compliance with current and voltage synthesis, and does not rely on communication infrastructure. Among a wide range of possible control methodologies of such regulators, four of them are discussed and later evaluated here. They are: the proportional-integral, proportional-resonant, proportional-repetitive, and hysteresis controllers. Such methodologies were chosen to make easy the physical implementation in a future step of this work, and also due to the affinity with independent previous works done by the researchers related to this dissertation. Despite having only these four controllers discussed in this work, many other methodologies are found in literature based on predictive (MORENO *et al.*, 2009), dead-beat (BUSO *et al.*, 2016), internal model (GAONA *et al.*, 2017), H^{∞} control (HORNIK; ZHONG, 2011) and other strategies (DASGUPTA *et al.*, 2011), with each of them presenting pros and cons depending on the application and functionalities of the SPI (HOSSAIN *et al.*, 2017; HOJABRI *et al.*, 2012; BUSO *et al.*, 1998).

The main reason behind the evaluation of four control methodologies lies on the idea of determining the most suitable for the purpose of this dissertation, seeing how they behave as controllers of multifunctional SPIs operating for active injection plus reactive and harmonic compensation. As many studies have been discussed advantages and disadvantages of these and many other controllers under many conditions (BUSO *et al.*, 1998; BUSO *et al.*, 2015; ZENG *et al.*, 2015), herein we focus in comparing their capacity for synthesizing currents and voltages under given references, and how feasible it would be for implementing them in a given digital signal processor, considering restricted processing capabilities.

4.1 Proportional-Integral Controllers

Because of its intense usage in control systems of quite diverse natures, Proportional-Integral (PI) controllers are the most employed regulators. In power electronics their application is as well found, being designed for current and voltage control, frequency regulation, and many other cases. In this work, PI controllers are adopted for current control in SPIs and also for voltage regulation of the DC voltage link. For reasons that will be said along with the related discussions, it is mentioned in advance that the adopted PI controller for voltage regulation of the DC link will be the only approach used for such application. Yet, in general, inner loop controllers are first designed and then a corresponding outer loop regulator is implemented. However, since this work considers the same design parameters of cut-off frequency and phase margin for all of the current controllers, the PI control methodology for the DC voltage link is first discussed.

4.1.1 DC Voltage Link: Proportional-Integral Controller

Although modulation signals are responsible for controlling the AC output of inverter, without an efficient control of its DC voltage side, it would not be possible to achieved a steady behavior and reliable current injection. Taking that into consideration, a PI controller is then devised for stabilizing the stored voltage at the DC link capacitor. For designing such controller, the outer voltage loop of the VSI in grid-connected mode (as in a DG), which is represented in the block diagram depicted in Fig. 12, must be further explored. It has already been explained that the open loop transfer function of the DC link (G_{wc_v}) is given by eq. (3.30). Now, the transfer function of the voltage controller (C_{v_i}) has to be represented by the PI regulator.

From classical control theory (OGATA, 2001), PI controllers are built aggregating a proportional gain with an integral gain, resulting in eq. (4.1).

$$C_{vi}(s) = PI(s) = \frac{K_{P_{DC}} \cdot s + K_{I_{DC}}}{s} \tag{4.1}$$

Now, adding the PI controller to the system transfer function, we have the open loop transfer function with controller (G_{c_v}) as shown in eq. (4.2).

$$\begin{aligned} G_{c_v}(s) &= C_{vi}(s) \cdot G_{wc_v}(s) \\ G_{c_v}(s) &= \frac{K_{P_{DC}} \cdot s + K_{I_{DC}}}{s} \cdot G_{wc_v}(s) \end{aligned} \tag{4.2}$$

As stated by Marafao (2004), for such case, it is desired to attain a phase margin (ph_m) of 70°, and also a cut-off frequency for the open loop system to be around $1 - 10Hz$, having as chosen $\omega_{CL_v} = 2\pi \cdot 5$ rad/s (5 Hz). Thus, making $|G_{c_v}(j.\omega_{CL_v})| = 1$, along with the assumption that $K_{I_{DC}} \ll K_{P_{DC}} \cdot \omega_{CL_v}$, the proportional ($K_{P_{DC}}$) gain for the DC link PI controller can be calculated as in eq. (4.3).

$$\begin{aligned} |G_{c_v}(j.\omega_{CL_v})| &= \left| \frac{K_{P_{DC}} \cdot j.\omega_{CL_v} + K_{I_{DC}}}{j.\omega_{CL_v}} \right| \cdot \left| K_{VAC} \cdot V_{AC} \cdot G_v(s) \cdot \frac{1}{K_i} \cdot K_{DC} \cdot K_{VDC} \right| = 1 \\ K_{P_{DC}} &= \left| \frac{1}{K_{VAC} \cdot V_{AC} \cdot \frac{1}{j.\omega_{CL_v} \cdot C_{DC}} \cdot \frac{1}{K_i} \cdot K_{DC} \cdot K_{VDC}} \right| \\ K_{P_{DC}} &= \frac{\omega_{CL_v}}{K_{VAC} \cdot V_{AC} \cdot \frac{1}{C_{DC}} \cdot \frac{1}{K_i} \cdot K_{DC} \cdot K_{VDC}} \\ K_{P_{DC}} &= 1.64 \end{aligned} \tag{4.3}$$

Analogously, analysing the phase of the system, it can be demonstrated that the integral gain ($K_{I_{DC}}$) of the voltage controller is given by eq. (4.4).

$$\begin{aligned} K_{I_{DC}} &= \frac{K_{P_{DC}} \cdot \omega_{CL_v}}{\tan(phm)} \\ K_{I_{DC}} &= 18.84 \end{aligned} \tag{4.4}$$

Using the just calculated gains, one can note that the frequency response of the system is corresponding to the designed parameters. For instance, in Fig. 15 it is shown that the phase margin and cut-off frequency were very closely achieved and the system is also closed loop stable with such gains.

Through a computational simulation developed with PSIM, the calculated PI gains for the DC link controller could be evaluated in a more realistic scenario. Let's consider a case in which a SPI has to supply all the non-active current demanded by a load (e.g. operating as an APF), in a circuitry as in Fig. 4, with the same load parameters of Subsection 3.2, and also an additional step given by a parallel connected RL load $(10 + j \cdot 5.65\Omega)$ at a given instant. It is reinforced that a full-bridge SPI, as given in Fig. 3, replaced the ideal current source in the testbed shown in Fig. 4. In Fig. 16 it is possible to note the results of this simulation, with the expected steady state convergence of the DC link voltage, being around the desired V_{DC} value of $235V$. Also, presenting a voltage ripple around the $V_{ripple} = 3\%$ established. It can be noticed in Fig. 16-c that, even under a perturbation started in 1.8 seconds, which is given by the load step of approximately 40% higher current demand, the DC link voltage controller is able to respond appropriately, returning to a steady state condition without excessive voltage overshoot.

As aforementioned, inadequate control of the DC link voltage or excessive capacitor voltage ripple may lead to inappropriate operation of the SPI. Thus, it is important to demonstrate that the parameters adopted for these two features does not impact on the desired injected current. The complete results of the circuit on the just shown PI voltage controller simulation is brought in Fig. 17 to prove that, even after the load step at 1.8 seconds, neither the chosen voltage ripple value, overshoot, nor transient response of the controller practically caused instabilities or over-currents. The SPI's synthesized non-active current followed the reference,

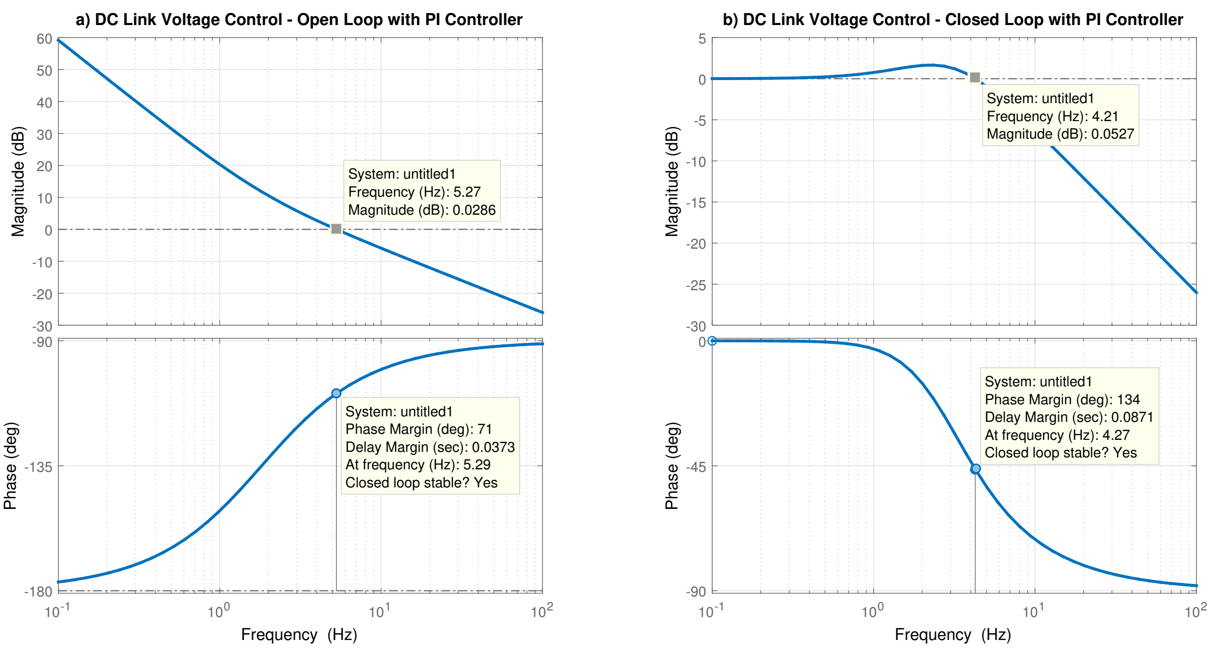


Figure 15 – Open (a) and closed (b) loop responses for DC link voltage with controller.

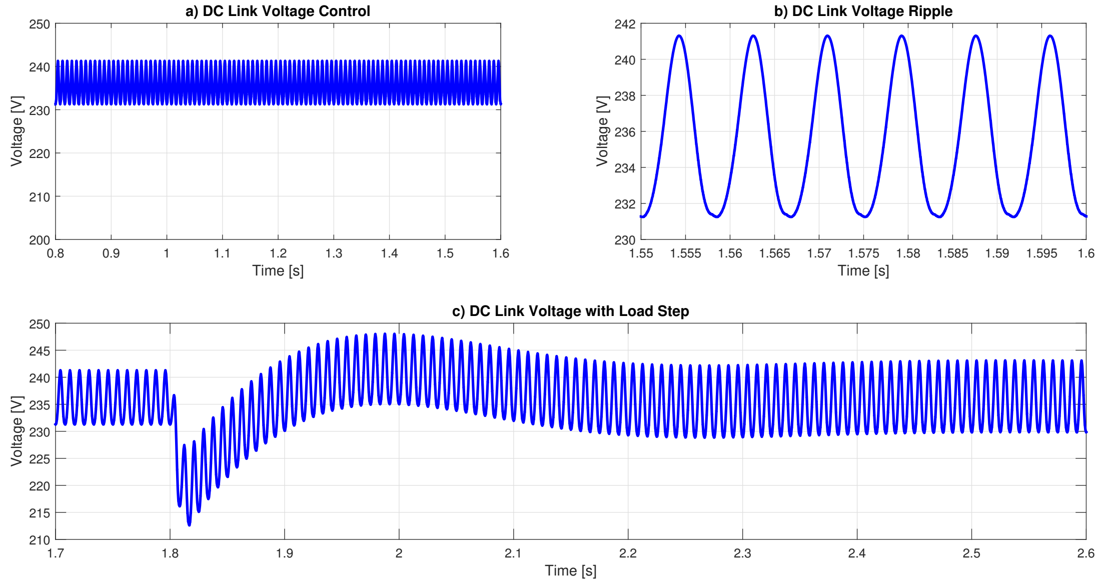


Figure 16 – Simulation of the DC link control.

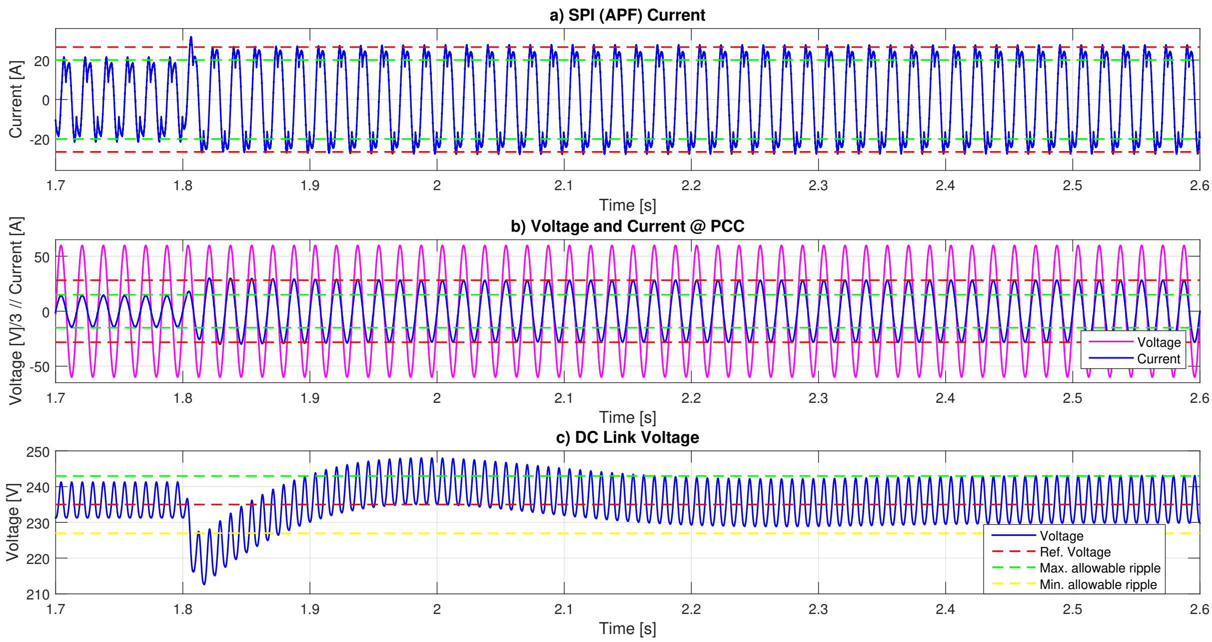


Figure 17 – Influence of DC voltage ripple on the SPI current.

constantly respecting the maximum limits at each given instant, allowing a very low distorted in-phase current with the voltage at the PCC, without requiring extra elements or control loops for DC link voltage ripple rejection (ZHU *et al.*, 2016; ENJETI; SHIREEN, 1992).

4.1.2 Proportional-Integral Current Controller

Within the primary control level of a distributed operation topology with SPIs, current control is a fundamental feature since power injection/absorption to/from a grid must occur under a synchronized and coordinated sharing approach. This requirement of controlled current sharing, considering the presence of SPIs with multifunctional capabilities, is required to adequately intervene on the expected electric current conditions at the PCC. As means for operating

SPIs under such conditions, one possibility is given by the most classic current control approach, which is based on PI regulators (BUSO *et al.*, 1998; MATAKAS; GIARETTA, 2011). The considerable acceptability of this current controller is due to its simple implementation and low computational requirement. However, as it will be later discussed, it presents drawbacks like, for instance, high error levels in steady state conditions for periodic signals, such as in the injection of sinusoidal quantities with constant frequency. Even though this negative feature would be enough to determine that this controller is not suitable for applications on multifunctional SPIs (ZAMMIT *et al.*, 2014), its design allows to comprehend the basic implementation of other controllers, especially those using a proportional term, such as the proportional-resonant and proportional-repetitive. Therefore, such statement justifies the presentation of the PI current controller in this dissertation.

The traditional implementation of a PI controller (OGATA, 2001) for current regulation in SPIs is given by the block diagram of Fig. 18-a. This controller operation mainly aims at a steady state error correction condition, doing that through the adjustment of a proportional (K_{P_i}) and integral (K_{I_i}) gains. Once a digital implementation of such controller is here intended, it is necessary to account for the discretization process of the respective proportional and integral parts.

For such digitized condition, as depicted in Fig. 18-b, the analog error reference is taken to a discrete condition by a zero order holder (ZOH), and later goes through the discrete controller, which now has its integral term computed by the Backward Euler method, resulting in the following equation of (4.5) to be implemented within a digital processor. It is reminded that T_s, m, and z^{-1} stand for, respectively, the ZOH sampling time, the modulation signal for the SPI, and the discrete unit delay at the respective k sample. Although the Backward Euler method is here mentioned, other methods like the Forward Euler or Trapezoidal (OPPENHEIM; SCHAFER, 2009) could be adopted without loss of effectiveness.

$$\begin{cases} m_I(k) = K_{I_i} \cdot T_s \cdot e_i(k) + m_I(k-1) \\ m(k) = K_{P_i} \cdot e_i(k) + m_I(k) \end{cases} \tag{4.5}$$

Despite the fact that this controller is imagined to be digitally implemented, (BUSO; MATTAVELLI, 2006) also explains that, in regard of the PI controller design, its respective analog and digital frequency responses present indistinguishable behavior. Therefore, resulting

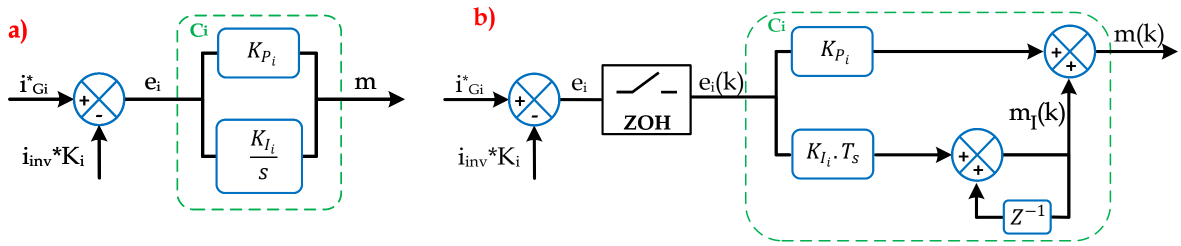


Figure 18 – Analog (a) and discrete (b) block diagrams for the PI current controller.

that the controller gains (K_{P_i}) and (K_{I_i}) can be considered the same for either an analog or digital use, being achieved by any of the two approaches.

It is worth mentioning that, when a PI controller is chosen for current control, anti-windup algorithms ought to be implemented along (MARAFAO, 2004). This sort of algorithm consists in not letting SPIs saturate under large transient responses, such as in initialization intervals or even steps on steady state conditions. This kind of saturation may occur in such PI controllers if their integral part accumulates the integrated error during transient intervals, impacting in slower response of the controller when a new set-point is defined, and consequently, in undesired levels of overshooting. When anti-windup solutions are employed, they provide a dynamic saturation of the integral controller, not letting error calculations to be considered in transients, and returning to be accounted again when the proportional controller outputs lies below a saturation limit (LI *et al.*, 2011). The anti-windup algorithm implemented in this work, based on an unitary limit (Lim) established for the p.u. error reference (ranging from -1 to +1), operates saturating the integral controller output according to the remaining limit after the proportional gain is accounted (i.e., $Lim = 1 - |e_i(k) \cdot K_{P_i}|$). Further explanation about this methodology is found in (MARAFAO, 2004). It is highlighted that, in the herein implemented cases no feedforward scheme was implemented in the control loops.

Being all that explained, the design of a PI controller is presented for the goal of making the generated currents of a multifunctional SPI to follow desired references, actively intervening in the power quality enhancement of a PCC. For such design we consider the SPI inner current loop of block diagram in Fig. 11, having the respective open loop transfer function (G_{wc_i}). When considering the PI current controller to be $C_i(s)$, the following open loop transfer function $G_{c_i}(s)$ given in eq. (4.6) is attained.

$$
\begin{aligned}
G_{c_i}(s) &= PI(s) \cdot G_{wc_i}(s) \\
G_{c_i}(s) &= (K_{P_i} + \frac{K_{I_i}}{s}) \cdot G_{wc_i}(s)
\end{aligned} \tag{4.6}
$$

To calculate the PI gains, (BUSO; MATTAVELLI, 2006) states that a phase margin of $ph_m = 60°$ is desired for the system, having the open loop crossover angular frequency (w_{CL}) to be $\frac{1}{10}$ of the switching frequency. Therefore, making the reasonable assumption of having $K_{I_i} \ll w_{CL} \cdot K_{P_i}$, the magnitude of $G_{c_i}(s)$ is said to be unitary at (w_{CL}), resulting in a proportional gain given by eq. (4.7).

$$
\begin{aligned}
|G_{c_i}(jw_{CL})| &= |C_i(jw_{CL})| \cdot |G_{wc_i}(jw_{CL})| = 1 \\
|G_{c_i}(jw_{CL})| &= \left| K_{P_i} + \frac{K_{I_i}}{jw_{CL}} \right| \cdot |G_{wc_i}(jw_{CL})| = 1 \\
K_{P_i} &= \frac{2 \cdot c_{pk}}{K_i \cdot V_{DC}} \cdot 1 \cdot \sqrt{(w_{CL} \cdot L_{LC})^2 + r_L^2}
\end{aligned} \tag{4.7}
$$

$$K_{P_i} = \frac{2 \cdot 1}{0.02 \cdot 235} \cdot 1 \cdot \sqrt{(2 \cdot \pi \cdot \frac{12000}{10} \cdot 1.5mH)^2 + (0.056\Omega)^2}$$
$$K_{P_i} = 4.81$$

Further exploring the just aforementioned assumptions, one can note that the integral gain is given by the phase of $G_{c_i}(jw_{CL})$, being denoted by eq. (4.8).

$$\begin{aligned} -180^\circ + ph_m &= -90^\circ - \arctan\left(\frac{K_{P_i}}{K_{I_i}}\right) - 2 \cdot \arctan\left(\frac{w_{CL} \cdot T_{sw}}{4}\right) - \arctan\left(\frac{w_{CL} \cdot L_{LC}}{r_L}\right) \\ K_{I_i} &= \frac{w_{CL} \cdot K_{P_i}}{\tan\left(-90^\circ + ph_m + 2 \cdot \arctan\left(\frac{w_{CL} \cdot T_{sw}}{4}\right) + \arctan\left(\frac{w_{CL} \cdot L_{LC}}{r_L}\right)\right)} \end{aligned} \tag{4.8}$$

$$K_{I_i} = \frac{2 \cdot \pi \cdot \frac{12000}{10} \cdot 12.01}{\tan\left(-90^\circ + 60^\circ + 2 \cdot \arctan\left(\frac{2 \cdot \pi \cdot \frac{12000}{10} \cdot \frac{1}{12000}}{4}\right) + \arctan\left(\frac{2 \cdot \pi \cdot \frac{12000}{10} \cdot 1.5mH}{(0.056\Omega)}\right)\right)}$$
$$K_{I_i} = 7999.70$$

With the calculated PI gains, the frequency response of the open and closed loop systems can be evaluated, as demonstred in Fig. 19, showing that the SPI with the designed controller presents a stable steady state condition. As aforementioned, these results already takes into consideration the delay existing in the PWM transfer function. One can note how the open loop system with the PI controller presents a phase margin very close to 60°, and a crossover frequency of $w_{CL} = 1.22kHz$, which is also the expected value since $w_{CL} = \frac{2 \cdot \pi \cdot f_{sw}}{10} = 7539.82 rad/s = 1.20kHz$.

Yet, as shown in Fig. 20, the system presents a closed loop bandwidth of $1.23kHz$, which is a value consistent with the proposed actuation frequency for the SPI.

Finally, considering this discussed controller, a simulation with PSIM was carried out to evaluate the effectiveness of the SPI operation with such PI control approach. A nonlinear load with the earlier conditions presented in Subsection 3.2 was adopted, along with the circuitry of

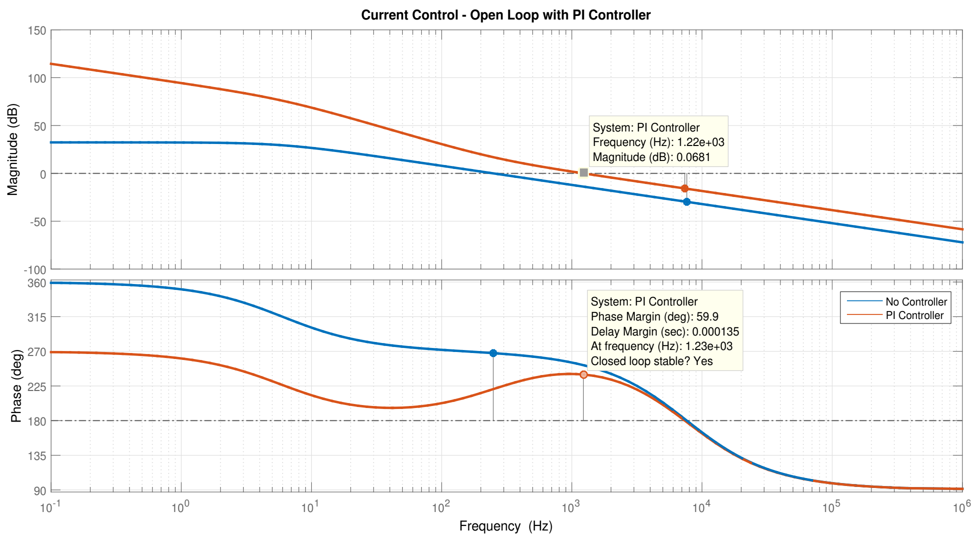


Figure 19 – Bode plot of the open loop current PI controller.

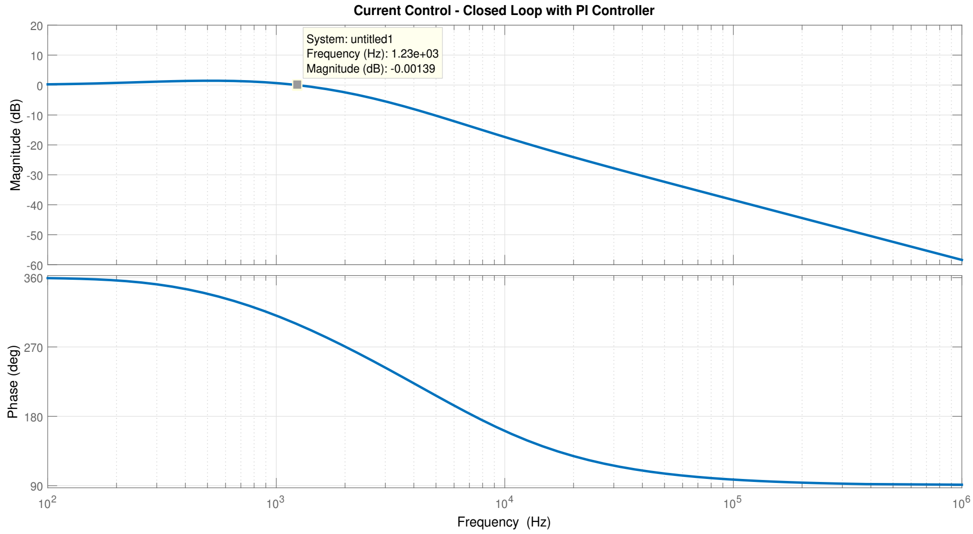


Figure 20 – Bode plot of the closed loop current PI controller.

Fig. 4 without line impedance, and with the same load step presented in the DC link voltage controller. It is reinforced that, since the following simulations intended to show the operation of the controller for active and non-active currents, an ideal DC voltage ($V_{DC} = 235V$) was inserted in parallel to the DC link capacitor of the SPI, simulating a DER which generates power to a multifunctional DG.

Only for exemplification, the generation of the compensation current references was implemented based on the Conservative Power Theory current terms decomposition, which was mentioned in Chapter 2 and is briefly detailed in Appendix B. Any other methodology able to provide current references could be used for this purpose, and would likely present similar results in a general view. The used controller gains were $K_{P_i} = 4.81$ and $K_{I_i} = 7999.70$.

As can be noticed in the simulation results shown in Fig. 21, from 2.4 to 2.5 seconds the SPI operates as a DG with the goal of supplying only active power into the PCC. For this case, the active current parcel of the CPT decomposition is used as control reference, and as aforementioned, it is highlighted that the power capability of the SPI is able to supply the entire power demand of the load at all instants. When active current is injected, as expected, the PCC current should be only composed by the non-active part of the demanded load current. After that period, from 2.5 to 2.6 seconds, the system begins working as an active power filter, not injecting active power, and providing the total demanded non-active current of the load, making the PCC current to approximately follow a pure sinusoidal condition with $THD_i^{PCC} = 4.92\%$. Note that the non-active current parcel injection (after 2.5 seconds) comprises reactive plus harmonic terms, therefore, remaining only low-distorted in-phase current at the PCC.

In 2.6 seconds a load step is simulated, aiming to show that, once within the range of the SPI capability, it is able to respond without losing effectiveness, reducing the current distortion to $THD_i^{PCC} = 2.83\%$. It is mentioned that this significant reduction in the THD_i^{PCC} is also due to the increase of the fundamental current parcel after the load step. For those two last stages, in this case and all other herein simulated, the control reference for the non-active

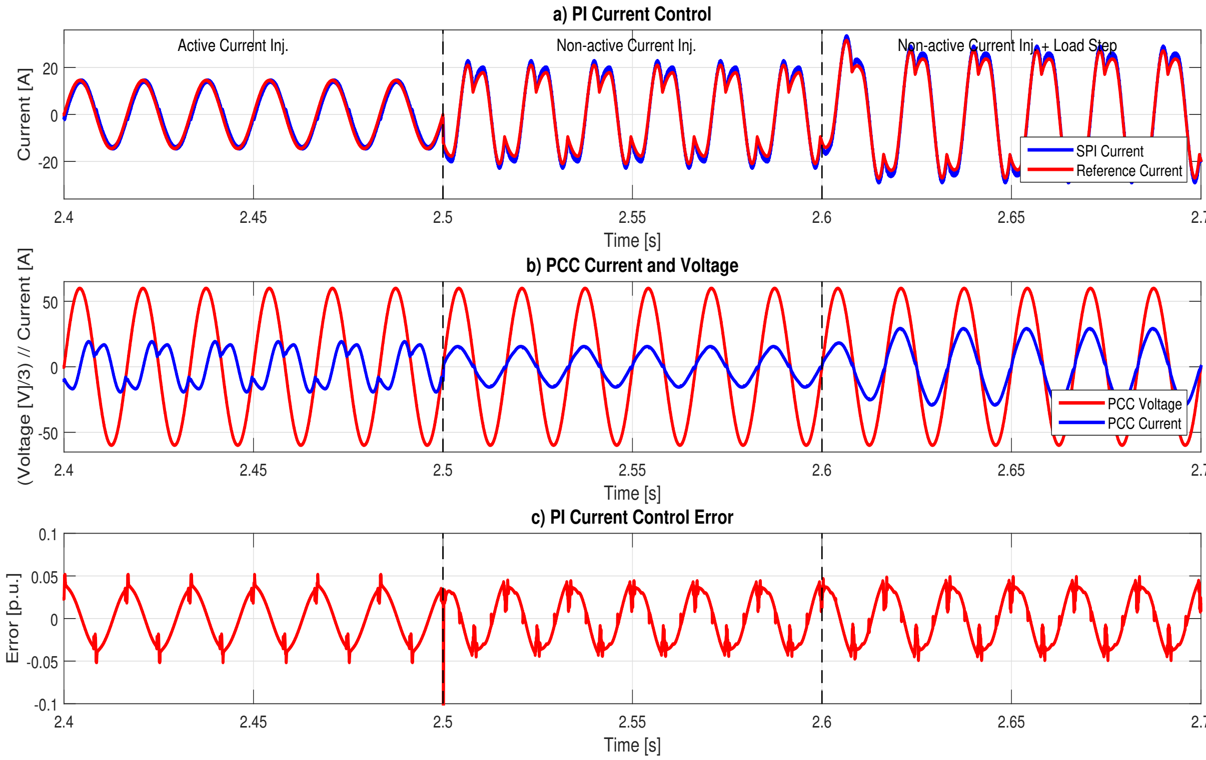


Figure 21 – SPI operating with PI current controller.

current injection is attained from the CPT, by summing of the reactive and void current parcels.

Although the PI current controller designed was able of providing a fair operation of a multifunctional SPI, it can be said in advance that other controllers later mentioned present lower error levels and/or better response time. Therefore, one should be cautious when adopting a proportional-integral AC current control, knowing that this controller may present reference deviations, being also easily affected by disturbances (MONFARED; GOLESTAN, 2012) that could lead to the inadequacy of the SPI operation. Nonetheless, some works as the one in (MARTINZ *et al.*, 2010) show that PI controllers can be effectively implemented for current control obtaining maximum and minimum operation limits for the proportional and integral terms, with interesting disturbance rejection capability and low magnitude and phase errors due to feedforward actions.

4.2 Proportional-Resonant Current Controller

When PWM based current controllers must be employed for power converter applications, proportional-resonant (PRes) topologies are likely one the most adopted alternatives (TIMBUS *et al.*, 2009). This sort of controller has the ability of incorporating the simplicity from proportional controllers, with the selective frequency control capability of resonant methodologies. Particularly focusing on DC-AC inverters, either on grid-connected or islanded operation, the flexibility to tune specific resonant frequencies in such controllers is highly desired, once it provides a way of precisely applying infinite gains in chosen harmonic frequencies

(TEODORESCU *et al.*, 2006). Consequently, PRes control methodologies for SPIs provide enhanced power quality interventions in electrical grids, with lower steady state error, specially in comparison to PI controllers.

Like many others (ZHANG *et al.*, 2014; MONFARED; GOLESTAN, 2012; TEODORESCU *et al.*, 2006), the PRes methodology described by (BUSO; MATTAVELLI, 2006), which is also the one here chosen for a controller design, is presented as an improved extension of a general PI methodology. As depicted in its operation in Fig. 22, this controller is composed of summing a proportional term with resonant parcels. The PRes block diagram is defined with the same proportional part as earlier discussed in the PI controller, presenting only particularities given by the syntonization of "h" resonant frequencies. For the sake of power quality enhancement, such frequencies are usually targeted to be the most significant lower odd harmonics present in the circuit, up to the a highest K_h order.

Looking at this controller in the frequency domain, its transfer function is given by the definition established in eq. (4.9) (BUSO; MATTAVELLI, 2006). For that case, h stands for the syntonized harmonic orders, and w_o for the fundamental angular frequency.

$$PRes(s) = K_{P_i} + \sum_{h=1,3,5,...}^{K_h} \frac{2 \cdot K_{Ih} \cdot s}{s^2 + (h \cdot w_o)^2} \tag{4.9}$$

Yet, the integrator gain (K_{Ih}), which is the resonant gain for each harmonic frequency, is attained from eq. (4.10), where $n_{oh} \cdot T_o$ is the desired transient response in relation to the fundamental frequency.

$$K_{Ih} = \frac{2.2 \cdot K_{P_i}}{n_{oh} \cdot T_o} \tag{4.10}$$

Having such definition, if one reminds the open loop transfer function of the proposed inverter with LC filter G_{wc_i}, the open loop accounting for the PRes controller is then given by eq. (4.11).

$$\begin{gathered} G_{c_i}(s) = PRes(s) \cdot G_{wc_i}(s) \\ G_{c_i}(s) = \left(K_{P_i} + \sum_{h=1,3,5,...}^{K_h} \frac{2 \cdot K_{Ih} \cdot s}{s^2 + (h \cdot w_o)^2} \right) \cdot G_{wc_i}(s) \end{gathered} \tag{4.11}$$

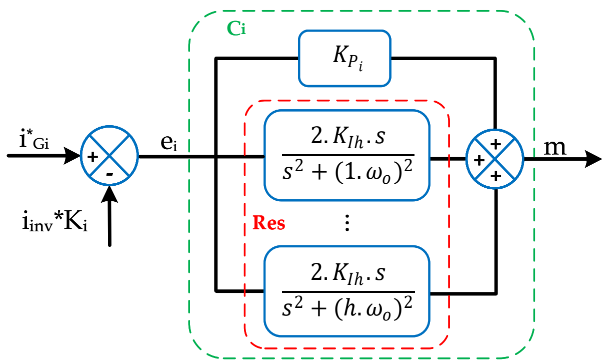


Figure 22 – Proportional-resonant controller block diagram.

Likewise the implementation of digital PI controllers, for embedding such controller in digital processors it is required to further employ a discretized approach of the PRes methodology. Taking advantage of the Tustin's discretization method, which is based on a bilinear transformation (OPPENHEIM; SCHAFER, 2009), the PRes controller modulation is then represented by eq. (4.12).

$$m(z^{-1}) = a_h \cdot e_i(z^{-1}) - a_h \cdot e_i(z^{-1}) \cdot z^{-2} + b_h \cdot m(z^{-1}) \cdot z^{-1} - m(z^{-1}) + K_{P_i} \cdot e_i(z^{-1}) \tag{4.12}$$

The respective a_h's and b_h's coefficients of the discrete equation are calculated by eq. (4.13).

$$a_h = \frac{2 \cdot K_{Ih} \cdot T_s}{4 + (h \cdot w_o)^2 \cdot T_s^2} \; and \; b_h = \frac{-8 + 2 \cdot (h \cdot w_o)^2 \cdot T_s^2}{4 + (h \cdot w_o)^2 \cdot T_s^2} \tag{4.13}$$

With the explanation of the PRes methodology, the discussion can be forwarded to the design of a controller considering the same conditions of the PI controller. As briefly aforementioned, the proportional gain of the controller is given by the same means as in a PI methodology (eq. (4.7)). Therefore, for this particular case, $K_{P_i} = 4.81$. Yet, it is chosen here for the PRes controller to present a transient response evaluated between 10%-90% of a step response for the fundamental frequency (BUSO; MATTAVELLI, 2006), $n_{oh} = 0.9$, resulting in eq. (4.14). This value for n_{oh} has been arbitrary chosen with the intention of complying with the step response range just mentioned, responding to a 90.0% condition. Note that this transient response evaluation is a feature given in relation to the application and behavior desired for the PRes controller. This means that if, for instance, it is desired for the system to present a slower rise time with lower overshooting, all that in relation to a step response (OGATA, 2001), higher values of n_{oh} should be chosen. Small percentages of n_{oh} would lead to exactly opposite features in relation to rise time and overshooting of the previously mentioned case.

$$K_{Ih} = \frac{2.2 \cdot 4.81}{0.9 \cdot 0.01666} \tag{4.14}$$
$$K_{Ih} = 705.86$$

Considering that multifunctional SPIs are expected to be controlled by this methodology, it is essential to set a bandwidth limit for resonant frequencies of the PRes controller. Otherwise, the controller could present loss of its effectiveness in a closed loop condition, or even become unstable. It is advisable to choose an upper boundary for the attenuation frequencies of about 1/10 to 1/6 of the switching frequency (TEODORESCU *et al.*, 2006). As an example, it would lead to a maximum resonance of around $w_{o_{max}} \leq \frac{f_{sw}}{10} = 1200Hz$.

In a previous discussion about Fig. 5, it was shown that the harmonic content of the load used on the simulations was mainly composed by resonances from the 3rd up to the 13th frequency. Thus, it was taken into consideration for the PSIM simulation, only the seventh odd lower harmonic frequencies. Note that the decision of such resonant frequencies should be made accordingly to the application of the converter and the limitation of its control bandwidth. The advantage of determining a lower number of resonant frequencies lies on relieving the computational burden of the hardware implementation (YANG; BLAABJERG, 2015).

In Fig. 23 the frequency response of the open loop system given in (4.11) is depicted, considering a PRes controller with the mentioned resonance frequencies and respective gains, and also accounting for the PWM delay. One can note how the system presents a particular resonant behavior at the seven selected resonant frequencies. Yet, from Fig. 24, it can be seen that in closed loop, the system with the controller presents a reasonable bandwidth considering the supposed bandwidth expected for the control actuation ($f_{sw}/10$). Under such conditions, the coefficients of the digitized PRes controller were calculated and summarized in Table 3. Another interesting matter to highlight is that, in Fig. 23, the peak of the resonance in the frequency response magnitude plot is lower for the harmonic orders than for the fundamental frequency. If one retrieves eq. (4.11), it can be noticed that for the resonant parcels, even though the same K_{Ih} is used, such term is divided by the harmonic orders $(h \cdot w_o)$. Yet, as previously seen in Fig. 13 for the SPI frequency response without a controller, the system magnitude starts to decrease for frequencies after 10 Hz, which comprises the bandwidth (between 60-780 Hz) of the resonant controllers and consequently reduces such peak gains.

Having all the coefficients of the discrete PRes controller, its implementation was created with the help of PSIM, under the same circuit conditions as the PI case. The same methodology was used, making the SPI controlled by the designed PRes controller to operate injecting active current from 2.4 to 2.5 seconds, supplying only non-active terms from 2.5 to 2.7s, also with a load step in 2.6s. The result of this simulation is presented in Fig. 25. Note how the PRes presents a lower steady state error, in comparison with the PI controller, consequently impacting in a less distorted current at the PCC when the SPI operates as an APF, presenting $THD_i^{PCC} = 3.48\%$ from 2.5 to 2.6s, and $THD_i^{PCC} = 1.18\%$ with the load step (2.6 to 2.7s).

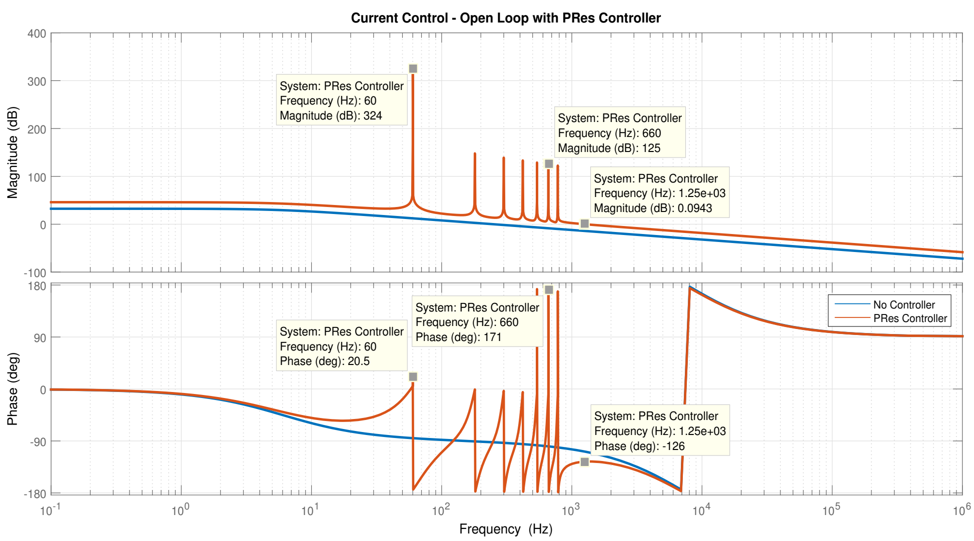


Figure 23 – Bode plot of the open loop current PRes controller.

Table 3 – Coefficients of the discretized PRes controller.

Discretized P+Resonant Coefficients				
Resonance	**a's**	**Value**	**b's**	**Value**
$1 \cdot w_o$	a_1	0.0147046041350297	b_1	1.99975327510920
$3 \cdot w_o$	a_3	0.0146973517300286	b_3	1.99778057115952
$5 \cdot w_o$	a_5	0.0146828683604729	b_5	1.99384099520882
$7 \cdot w_o$	a_7	0.0146611967490277	b_7	1.98794616811528
$9 \cdot w_o$	a_9	0.0146324005862951	b_9	1.98011341415995
$11 \cdot w_o$	a_{11}	0.0145965640647835	b_{11}	1.97036563428310
$13 \cdot w_o$	a_{13}	0.0145537912674624	b_{13}	1.95873113976699

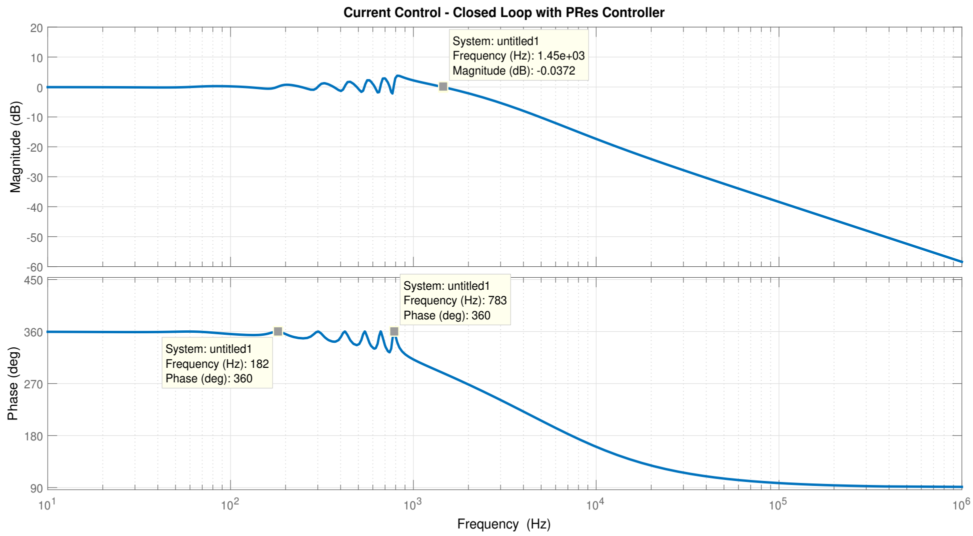


Figure 24 – Bode plot of the closed loop current PRes controller.

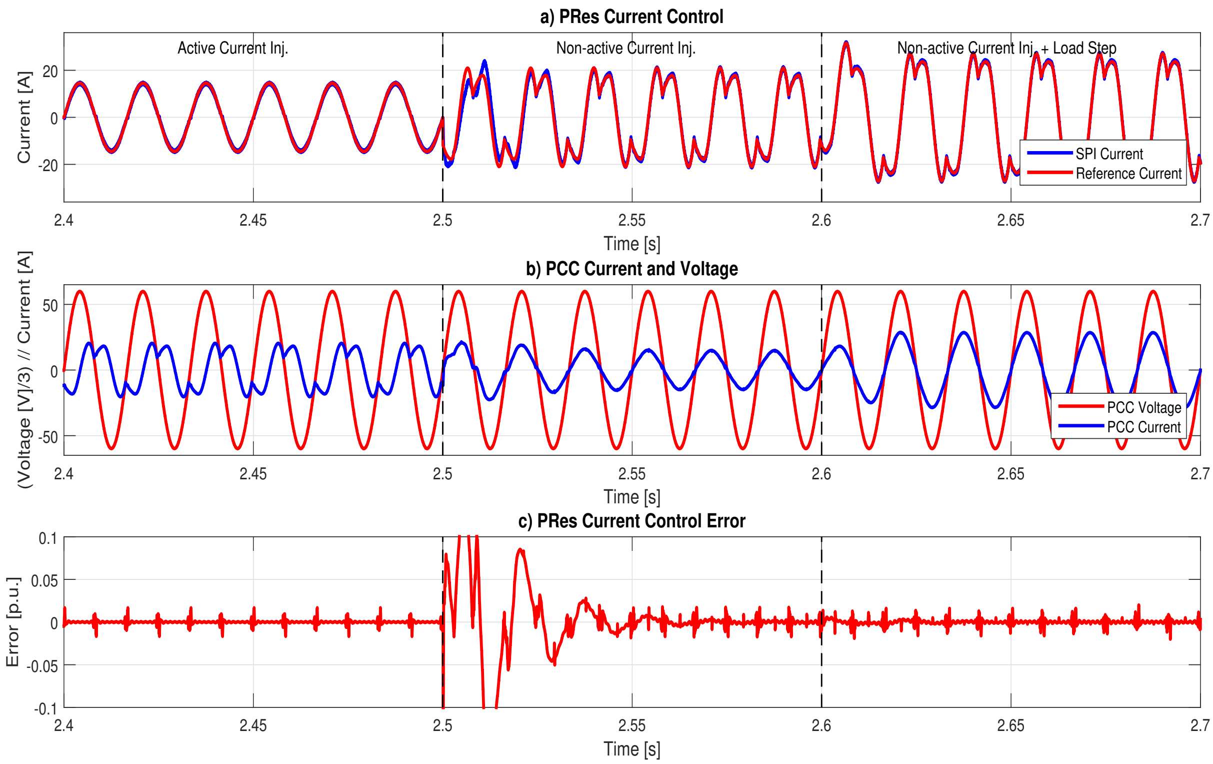


Figure 25 – P+Resonant Current Controller.

4.3 Proportional-Repetitive Current Controller

Reference tracking with zero steady state error is the ideal expected scenario of a current controller employed on power converter applications. One of the most efficient alternatives to achieve such condition is determined by repetitive control methodologies (MARAFAO *et al.*, 2004b; GARCIA-CERRADA *et al.*, 2007; TRIVEDI; SINGH, 2017). Under a superficial explanation, the main idea behind such controllers lies on the internal model principle (ROOVER; BOSGRA, 1997), and its effectiveness is dependent on having a closed loop system that accounts for the reference model.

For the proposal of a current controller focused on the implementation of multifunctional SPIs, a variation based on a proportional repetitive (PRep) regulator is chosen. This approach, as discussed in (BUSO; MATTAVELLI, 2006), provides an interesting way of achieving a desired dynamic response by the proportional term, and uses the repetitive part to contribute on steady state error mitigation in multiple frequencies. The block diagram shown in Fig. 26 gives an overview of the operation of such controller. Its proportional gain is again, as in the PRes case, designed as in any general PI controller. The repetitive loop intents to sum the error reference of the "k^{th}" stage with its past sample "$k-1$", which is attained from delaying the error by a period of the respective selected frequencies (fundamental and/or harmonics).

As well explained by (MATTAVELLI; MARAFAO, 2004), the particularities of the repetitive concept of this controller take advantage of filters implemented by means of the Discrete Fourier Transform (OPPENHEIM; SCHAFER, 2009), allowing selective compensation on desired frequencies. The methodology of such filters, which are built through moving windows, is based on a Z-domain cosine transform, being formulated by eq. (4.15).

$$F_{DFT}(Z) = \frac{2}{N} \cdot \sum_{i=0}^{N-1} \left(\sum_{h \in N_h} cos\left[\frac{2\pi \cdot h \cdot (i+N_a)}{N}\right]\right) \cdot Z^{-i} \tag{4.15}$$

The size of the filter window (N) is given by the number of samples in one cycle of the fundamental frequency. N_h stands for the set of selected harmonic frequencies of the filter, and N_a is the number delay steps. An appropriate value for N_a is to be chosen regarding the compensation of the current control delay, in which a leading of one to three sampling periods is said to be adequate (MATTAVELLI; MARAFAO, 2004). The gain K_f in eq. (4.16), being

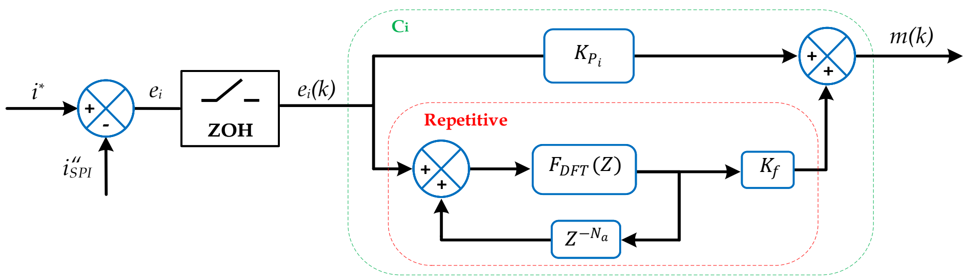


Figure 26 – Proportional-repetitive controller block diagram.

related to the K_{Ih} term of the PRes controller, refers to the transient response capability of the repetitive controller, which operates up to the highest frequency of the filter (w_s). Note the similarity between eq. (4.16) and eq. (4.10), it is clearly seen that K_f is related to K_{Ih} but it disregards the proportional gain K_{P_i}. Since the repetitive controller operates with delayed error samples, the use of K_f is justified by not constantly multiplying repeated error values by a high proportional gain K_{P_i}. In PRes controllers, K_{P_i} is considered in K_{Ih} since it is only accounted once and not in repeated loops.

$$K_f = \frac{2.2}{0.32 \cdot n_{oh} \cdot T_o \cdot w_s} \tag{4.16}$$

From the discussions made in (MATTAVELLI; MARAFAO, 2004), it can be inferred that such repetitive regulators present similarities with a general synchronous frame harmonic control, different from the previously discussed PRes controllers which operate in stationary reference frame. However, it is explained that such regulators are now approximated by a sum of pass-band filters, being determined by eq. (4.17), where F_h and ξ_h are formulated by eq. (4.18) and (4.19). Since band-pass filters are designed defining, in relation to a center frequency, a bandwidth of other passing harmonic orders, the term ξ_h has to be considered to model this span between lower and higher cutoff frequencies of these filters. Therefore, eq. (4.17) interacts with eq.(4.18) as in a regulator that gives a small proportional gain to repetitive inputs, which are filters syntonized in several selected harmonic orders ($h \cdot w_o$), being modeled as second order systems with pass bandwidth proportional to the term "$2\xi_h \cdot h \cdot w_o \cdot s$". Eq. (4.19) reinforces the relation of K_f as a proportional gain for repetitive parcels, which additionally deals with the transient response ($n_{oh} \cdot T_o$) of the controller just as in the PRes case.

$$R_h(s) = K_f \cdot \sum_{h \in N_h} \frac{F_h}{1 - F_h} \tag{4.17}$$

$$F_h(s) = \frac{2\xi_h \cdot h \cdot w_o \cdot s}{s^2 + 2\xi_h \cdot h \cdot w_o \cdot s + (h \cdot w_o)^2} \tag{4.18}$$

$$K_f = \frac{K_{Ih}}{\xi_h \cdot h \cdot w_o} \tag{4.19}$$

Taking into consideration the mentioned similarity with resonant regulator, from Fig. 27 it can be noted that the PRep controllers, in fact, work as band-pass filters, giving infinite gains with defined bandwidth in syntonized frequencies.

The closed loop frequency response of this designed PRep current regulator is shown in Fig. 28. It is highlighted how its bandwidth also presents a consistent value in regard to the expected controller bandwidth.

On the design of the PRep controller for a computational simulation with PSIM, the following considerations are made. For the same reasons discussed on the PRes controller case,

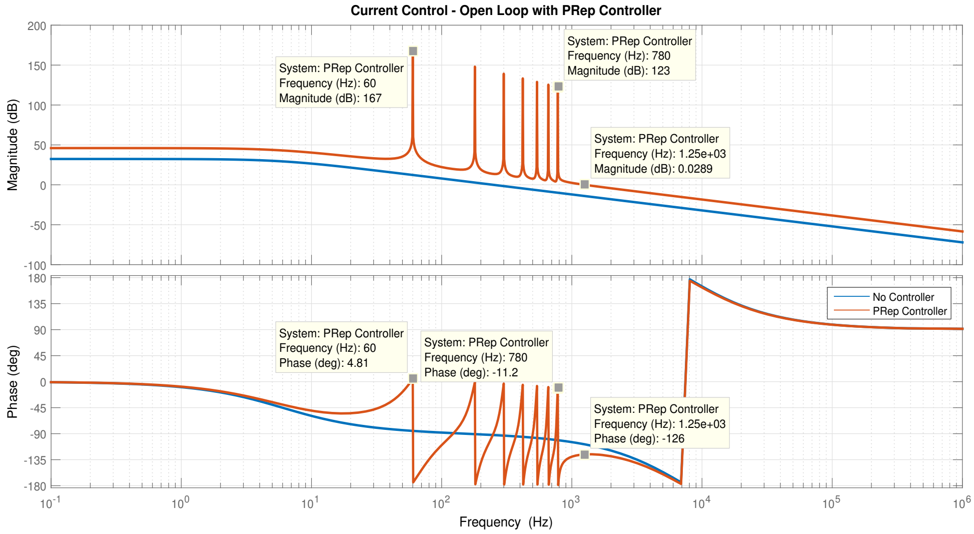


Figure 27 – Bode plot of the open loop current PRep controller.

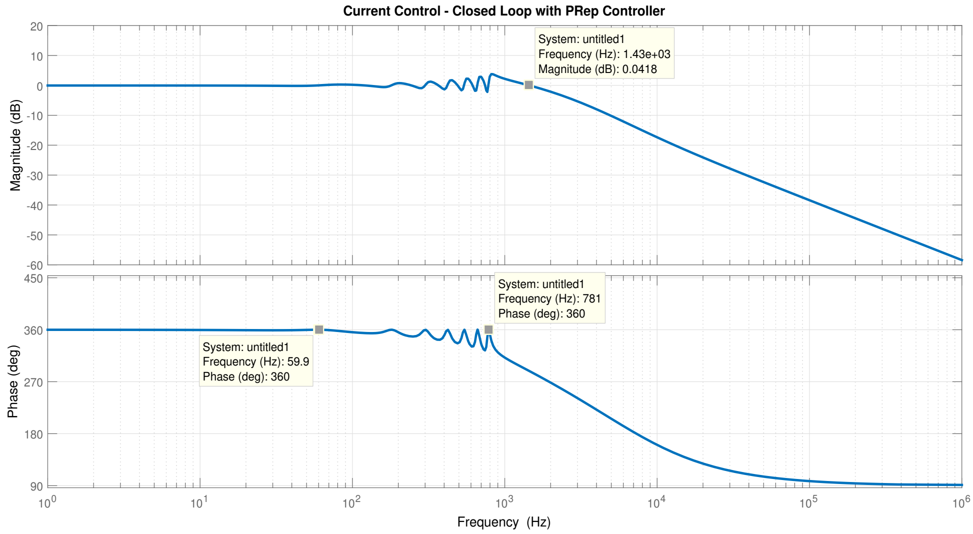


Figure 28 – Bode plot of the closed loop current PRep controller.

the cosine transform filter only targets the selected odd harmonics up to the 13$^{\text{th}}$. Being in double update mode, it is supposed a moving filter with a window of 400 samples, N_a being equal to two, and a transient response to be around 90% of the fundamental period. Therefore, resulting in eq. (4.20).

$$K_f = \frac{2.2}{0.32 \cdot 0.9 \cdot 0.01666 \cdot 2 \cdot \pi \cdot 60 \cdot 13} \tag{4.20}$$
$$K_f = 0.0935$$

As earlier, a simulation was carried out considering the respective mentioned features of the PRep controller. It is shown in Fig. 29 that, from 2.4 to 2.5 seconds the SPI only in injects active current. Later it injects only the non-active currents demanded by the load, resulting in low distorted current with $THD_i^{PCC} = 3.71\%$. If one reminds the previous simulations, when comparing to this case, the mismatching from the reference and the synthesized current decreases as time goes by, for instance, presenting in the last stage $THD_i^{PCC} = 1.62\%$. That is

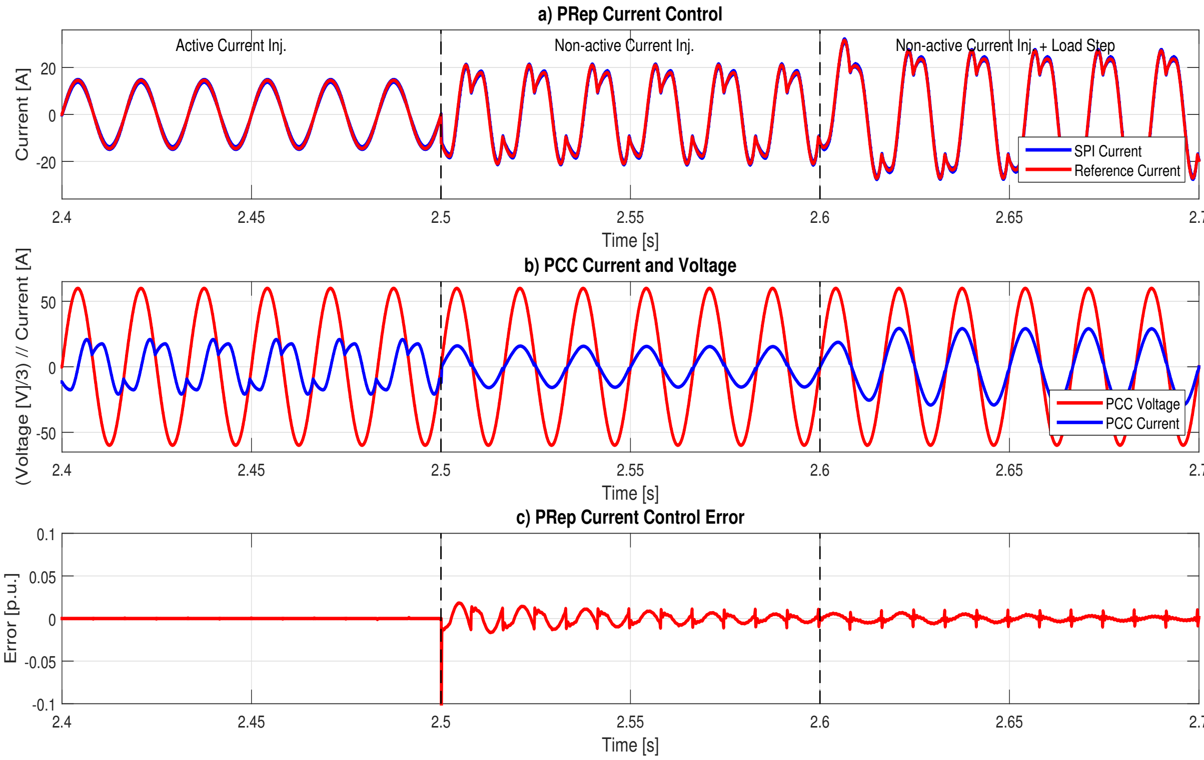


Figure 29 – Proportional-Repetitive Current Controller.

the expected condition, since repetitive controllers are capable of literally providing null error steady state condition as can be seen on the active current injection interval.

Although PRep controllers seem to be very suitable for power converter applications, in general, they are tied to constraints related, for instance, to limited processing capabilities of digital signal processors. Yet, with higher precision demanded or having more frequencies selected for the discrete filters, more robust computing is required. Nevertheless, more recent methodologies of PRep controllers based on recursive Discrete Fourier Tranform (ALMEIDA *et al.*, 2014; CHEN *et al.*, 2017) and other novel approaches (ZHENG *et al.*, 2017; TRIVEDI; SINGH, 2017) have been proposed in the literature, requiring less computational effort.

4.4 Hysteresis Current Controller

Hysteresis controllers (HC) are an interesting alternative for the implementation of current controllers, since they present rapid response, wide control bandwidth and many other interesting features for applications in DC-AC power converters (MALESANI *et al.*, 1997). Among several of the advantages of employing such controllers, one of the most interesting is its simple operation and implementation, functioning as an analog controller. In addition, considering some of the most traditional HC methodologies, they are mainly based on variable or fixed switching frequency approaches.

Here, two design methodologies of these two approaches are briefly discussed and implemented, with the intention of showing that both have advantages and disadvantages, being more or less suitable depending on the application and technology used for their employment. Regardless of being fixed or variable frequency based, the operation of an HC is basically presented in Fig. 30.

One can note that the operation of a HC depends exclusively on the comparison of an actual measured current value, which is generated by the inverter, with a superior (B^+) or inferior (B^-) hysteresis band that coordinates the switching control signals. When the inverter current encounters itself above or below these hysteresis bands, control commands of respectively OFF and ON status are sent to the gates of the switches. In some cases, this band comparison is strictly followed, not caring for the variation of the switching frequency, being therefore characterized as variable frequency HC (VFHC). When this band is considered, but not taken as a mandatory reference, giving priority to the maintenance of a determined switching frequency, fixed frequency HC (FFHC) is the target. As shown in Fig. 30, for this case of FFHC, the reference upper and lower hysteresis bands may be not respected, exceeding determined current ripple limits.

Without any particular reason, it is first presented here the operation of a VFHC, and later a methodology for FFHC.

4.4.1 Variable Frequency Hysteresis Controller

As demonstrated by (BODE; HOLMES, 2000), for a complete switching cycle period ($T_{VF}/2$) of the VFHC, considering a SPI with a DC link voltage of V_{DC} under a three-level PWM technique, the analysis of its synthesized instantaneous current is given by eq. (4.21) and eq. (4.22), where v_O is the SPI output voltage (BUSO *et al.*, 2015). It is important to mention that, as demonstrated by (ESPINOZA, 2011; BARBI, 2007), in three-level modulation the frequency of the SPI output voltage (before the filter) is twice the switching frequency. Consequently, this allows to obtain $T_{VF}/2 = T_{sw}$, since the hysteresis bands of the positive and

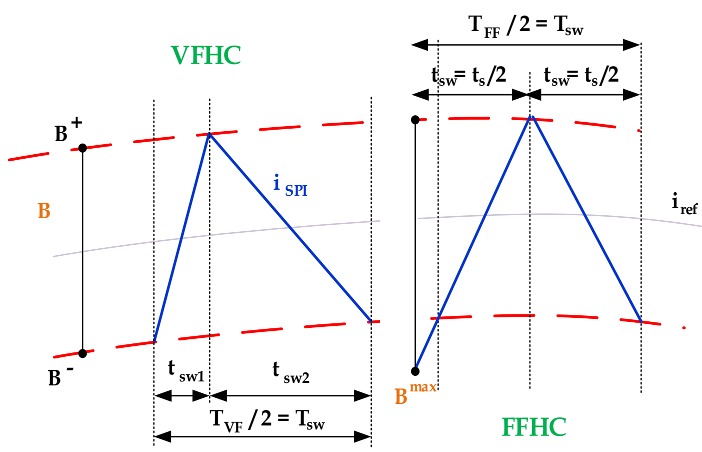


Figure 30 – Variable and fixed frequency hysteresis controllers.

negative output voltages of the SPI overlap (BODE; HOLMES, 2000).

$$t_{sw1} = \frac{-B \cdot L_{LC}}{-v_O} \tag{4.21}$$

$$\frac{T_{VF}}{2} - t_{sw1} = \frac{B \cdot L_{LC}}{V_{DC} - v_O} \tag{4.22}$$

Then, by summing eq. (4.21) and eq. (4.22), an expression given by eq. (4.23) can be attained for the relation between the most critical switching frequency of the HC and the parameters of the inverter in an unipolar modulation. Note that this equation depends on the hysteresis band term, resulting that the smaller B is, the higher the switching frequencies should be.

$$T_{sw} = \frac{2 \cdot B \cdot L_{LC} \cdot V_{DC}}{v_O \cdot (V_{DC} - v_O)}$$

$$f_{sw} = \frac{1}{T_{sw}}$$

$$f_{sw} = \frac{v_O \cdot (V_{DC} - v_O)}{2 \cdot B \cdot L_{LC} \cdot V_{DC}} \tag{4.23}$$

Since the interest here lies in knowing the maximum switching frequency of the system, the derivative of eq. (4.23) can be taken to find the maximum of the function:

$$f'_{sw} = 0$$

$$(v_O \cdot V_{DC} - v_O^2)' = 0$$

$$v_O = \frac{V_{DC}}{2} \tag{4.24}$$

For the most critical condition given by eq. (4.24), substituting in eq. (4.23), the maximum switching frequency is found by eq. (4.25). The main idea behind this equation is that, if one wants the current controller to not extrapolate the hysteresis bands (B^+) and (B^-), the switching frequency of the inverter will exceed, and a maximum switching frequency of f_{max} may occur.

$$f_{max} = \frac{V_{DC}}{8 \cdot B \cdot L_{LC}} \tag{4.25}$$

Therefore, if sequence is given to the design of a VFHC, assuming a 10% current ripple, and considering a hysteresis band to be $B = 2 \cdot \Delta I_{LC_{ripple}} = 0.2A$, the maximum switching frequency of the inverter is then calculated as follows.

$$f_{sw} \geq \frac{235}{8 \cdot 0.2 \cdot 1.5 \cdot 10^{-3}}$$

$$f_{sw} \geq 97.916\ kHz \tag{4.26}$$

Since the design of this VFHC here aims at a digital implementation, as stated by Ingram e Round 1999, there should occur the adequacy of the sampling frequency of the system,

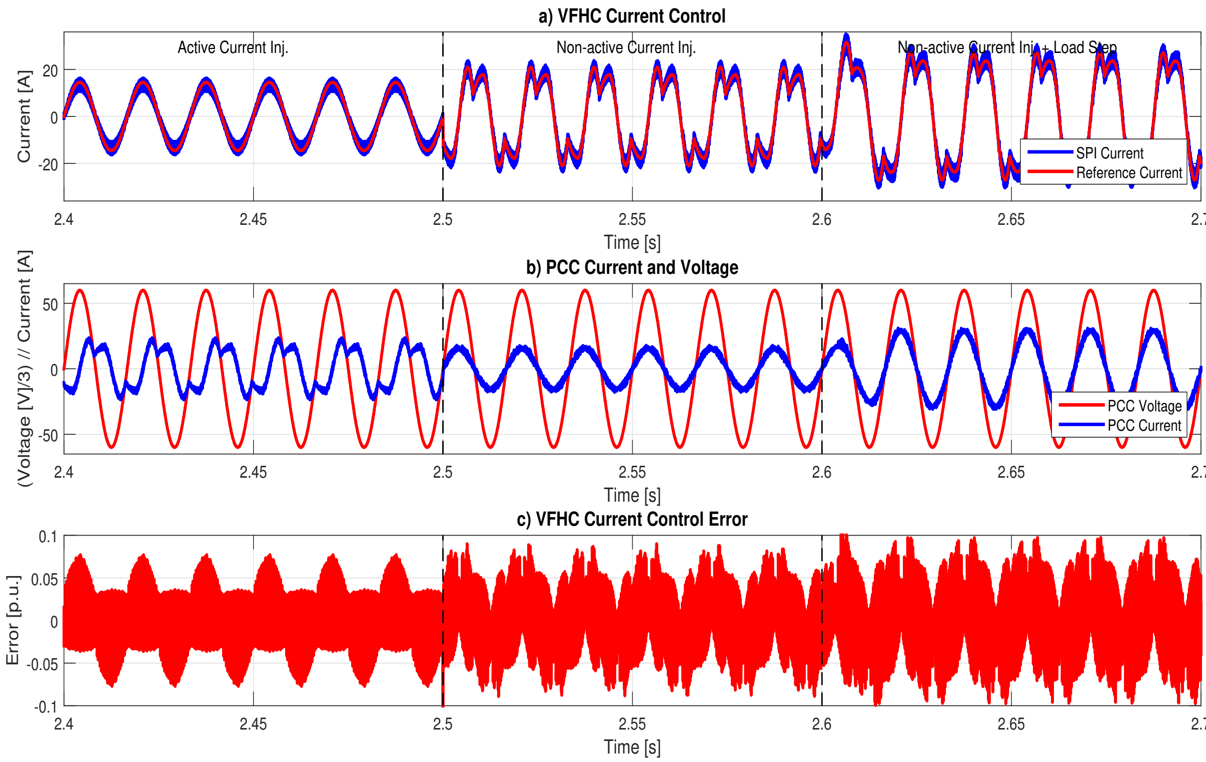


Figure 31 – VFHC - Hysteresis Current Controller.

which should be high enough to provide at least one sample per switching period. Thus, selecting $f_s = 97.920kHz$ for the reason of having an even number of samples in respect to the grid $60Hz$ frequency, a simulation was carried out with PSIM, showing the results of the VFHC operation as depicted in Fig. 31. Between 2.5 to 2.6s the remaining current presented $THD_i^{PCC} = 14.22\%$, and in the following stage (2.6 to 2.7s) it was $THD_i^{PCC} = 9.14\%$.

From the results one can note that, when different operation conditions are set, the VFHC rapidly responds to this change and provides low error in steady state conditions. However, the main drawback about the employment of VFHC methodologies is that, in general, they turn out to demand high switching frequencies, which may be very limited in certain cases (e.g. when IGBTs are used, supporting frequencies, in general, of around 20 kHz). Besides, the precision of the controller to follow the current reference is dependent on small hysteresis bands, which once again is tied to faster switching updates.

4.4.2 Fixed Frequency Hysteresis Controller

FFHCs operate similarly to the just mentioned VFHC example, however, not being directly commanded by band comparisons. The control commands for switching occurs respecting a fixed frequency, which means that the ON-OFF control setpoints of the controller are only updated in periodic instants, regardless of the state of the current being generated by the SPI. An important thing to mention is that, having switching control commands being updated at fixed periods, it does not mean that the state of the switches will obligatorily change at those instants. Such changes occur when a switching period window is open, and also if the current value is either above B^+ or below B^-.

An important consequence of this operational condition is related to, in some switching periods, the current exceeding the hysteresis band. This may be critical since, in some cases, the overcurrent generated could likely reach safety boundaries or any other electrical limits of the system. The maximum current excess over the FFHC band ($I_{B_{max}}$), as demonstrated by PRAKASH *et al.* 2016, can be obtained by eq. (4.27). As described in the literature, when the attained values of this hysteresis band are not acceptable, adaptations on system parameters would have to be adopted. It is important to note that, since a three-level PWM has been used for the FFHC, meaning that $T_{sw} = 2 \cdot T_{FF}$, the resultant hysteresis band should take "$2 \cdot f_{sw}$" into consideration in (4.27) (PRAKASH *et al.*, 2016).

$$I_{B_{max}} = \frac{V_{DC} + V_g^{peak}}{2 \cdot f_{sw} \cdot L_{LC}} \tag{4.27}$$

For instance, if it is considered the same inverter parameters adopted so far for the design of a FFHC, a maximum current extrapolation of $I_{B_{max}} = 11.52A$ is attained. This value would not be acceptable, since it consists of about 30% of the SPI possible peak current. Therefore, an adjustment of the inductor (L_{LC}) and other elements of the LC filter must be done, considering a maximum 10% current ripple, resulting in $L_{LC} = 4.94mH$. With such parameters readjusted, the design of the hysteresis regulator is as trivial as for the just mentioned VFHC, only requiring the determination of the hysteresis band and the switching frequency. Once again, considering a general implementation of SPIs based on IGBTs, a commutation frequency of $f_{sw} = 12kHz$ is adopted. In addition, the hysteresis band for this case can be calculated by eq. (4.28) (PRAKASH *et al.*, 2016).

$$\begin{aligned} B &= \frac{(V_{DC} - V_g^{peak})}{(V_{DC} + V_g^{peak})} \cdot I_{SPI}^{peak} \cdot \Delta I_{LC}^{ripple} \\ B &= \frac{235 - 180}{235 + 180} \cdot 33.29 \cdot 0.1 \\ B &= 0.44A \end{aligned} \tag{4.28}$$

The digital implementation of this controller is made likewise, requiring the project of a system that behaves as a SR flip-flop, and follows the logic given in Fig. 32.

The results of this simulation are presented in Fig. 33. It can be noticed how the FFHC adequately follows the given reference, however, presenting higher error than the VFHC. This

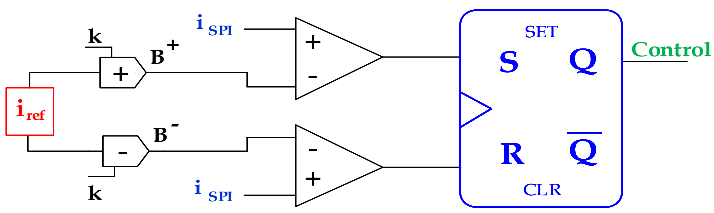


Figure 32 – Operation of hysteresis controllers.

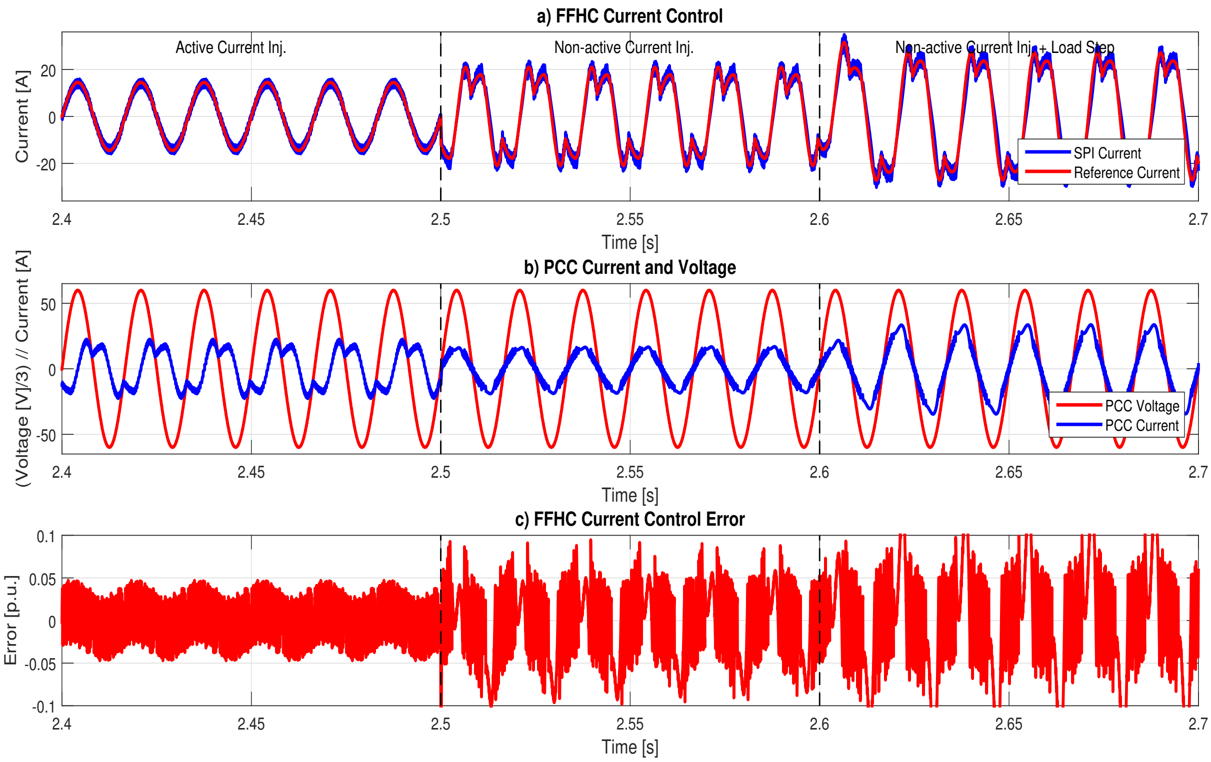


Figure 33 – Hysteresis Current Controller.

is reasonable since the fixed switching frequency limits the capacity of the converter to pursue lower error conditions. From 2.5 to 2.6s the PCC current presented $THD_i^{PCC} = 14.24\%$, and $THD_i^{PCC} = 10.86\%$ for the last interval.

By designing and simulating all these proposed controller methodologies, from the PI to the FFHC, a short section is then following presented, trying to rise discussions regarding a quantitative comparison of their adequacy to this dissertation.

4.5 Comparison of Controllers

The current controllers discussed earlier are here compared based mainly in three quantifiers, which are an error related analysis, the evaluation of the total harmonic distortions of the injected SPI current and the current at a PCC, and as last, the assessment of the processing time demanded for the algorithm in a real implementation with a digital processor. To produce more clear and consistent comparisons, the data used for this section comes from the simulations presented in Figs. 21, 25, 29, 31, 33. Another relevant consideration that must be said is that the data range of the following analyses, for all the current controllers, were taken from the interval between 2.5 and 2.6s of the respective simulations.

4.5.1 Mean Absolute Error

One of the most widely used approaches for statistical analysis of error quantities is the Mean Absolute Error (MEA) (MONTGOMERY; RUNGER, 2003). This methodology consists in finding the mean of the absolute error of a set of samples, giving a quantity that can be used for qualitative comparisons. The MEA is calculated as given by eq. (4.29), where "n" is an error sample of a set with "N".

$$MAE = \frac{\sum_{n=1}^{N} |e_n|}{n} \tag{4.29}$$

For the comparison of the current controllers, the respective MAE of the p.u. error was calculated for each of them under the mentioned time interval. Afterward, these quantities were plotted together, as shown in Fig. 34.

Some conclusions can be extracted from this figure. Firstly, it is noted that the FFHC controller is the one with highest MAE, and contrariwise, the PRep presents the lowest error feature. This was indeed the expected result, and it is one of many other justifications of why general approaches of PI controllers have not been extensively used in power electronics applications that required significant levels of current precision. By thinking about the hysteresis methodologies, the results make sense as well, since the harmonic content is expected to be higher and the fixed frequency approach reduces the capacity of the controller to adequately operate under a determined hysteresis band.

Finally it can be observed that the PRes controller is the one which presents the closest error amount to the best expected response, which is the one from the PRep. This also justifies the high employment of this type of controller (TIMBUS *et al.*, 2009), proving considerable low error conditions, with lower requirement of computational effort than PRep controllers.

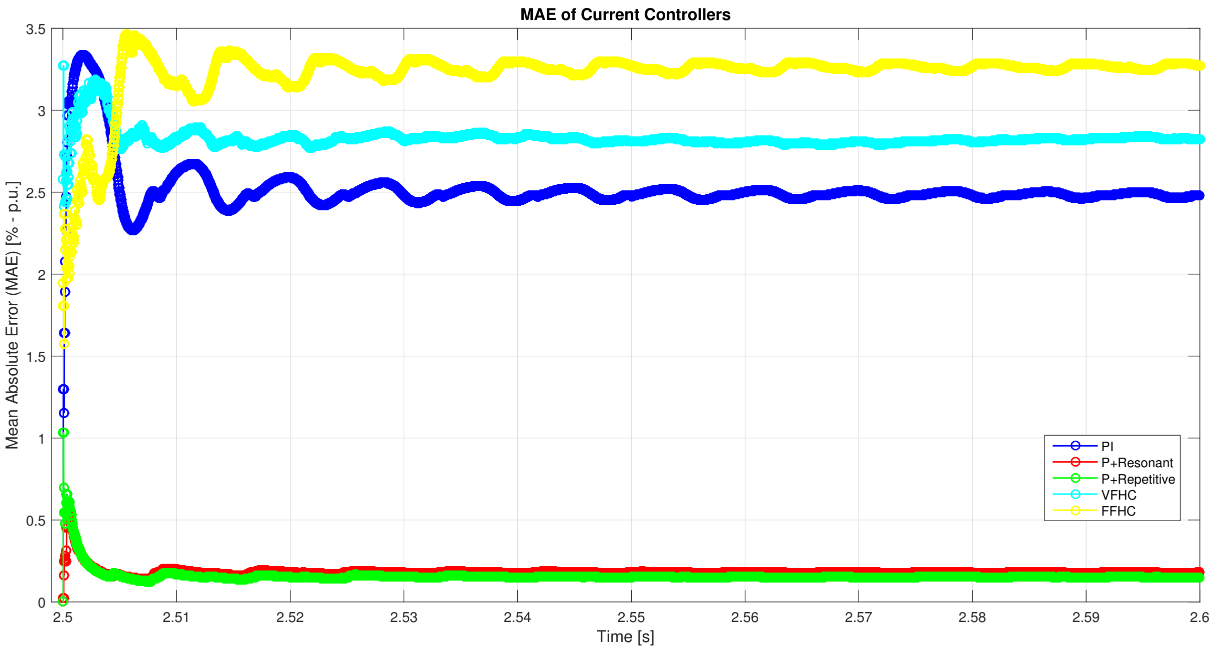


Figure 34 – Error comparison for current controllers.

4.5.2 Current Total Harmonic Distortion

The second comparison parameter for the current controllers is the harmonic content generated by their operation. Since this work pursues minimization of harmonic levels in networks, if heavy distortion is generated by the SPI of a DER, the effectiveness of the distributed compensation may be affected. Therefore, the harmonic content of the SPI current and the current drained from the PCC at the same previous simulation interval were analyzed for each controller.

The total current harmonic distortion (THD_i) is a parameter that determines how polluted a signal is regarding to harmonics. Its general definition used so far in the discussions of current controllers is expressed by eq. (4.30). This quantity is determined based on the amplitude of the fundamental component (I_1) of the respective signal, SPI or PCC current, in relation to the amplitude of a set "H" of other harmonic orders (I_h).

$$THD_i = \frac{\sqrt{\sum_{h=1}^{H} I_h^2}}{I_1} \tag{4.30}$$

The THD_i's of all the current controllers were calculated and plotted in Fig. 35, aiming at attaining a comparison perspective. When analyzing the PCC current, it can be noted how the hysteresis controllers are at upper levels. It occurs due to the fact they operate under an ON-OFF condition, not smoothly following the waveform of the reference current. Again as expected, the PRep is the one with the lowest harmonic content, together with the PRes controller. This is justified by their design procedures, since they are tuned to damp specific harmonics.

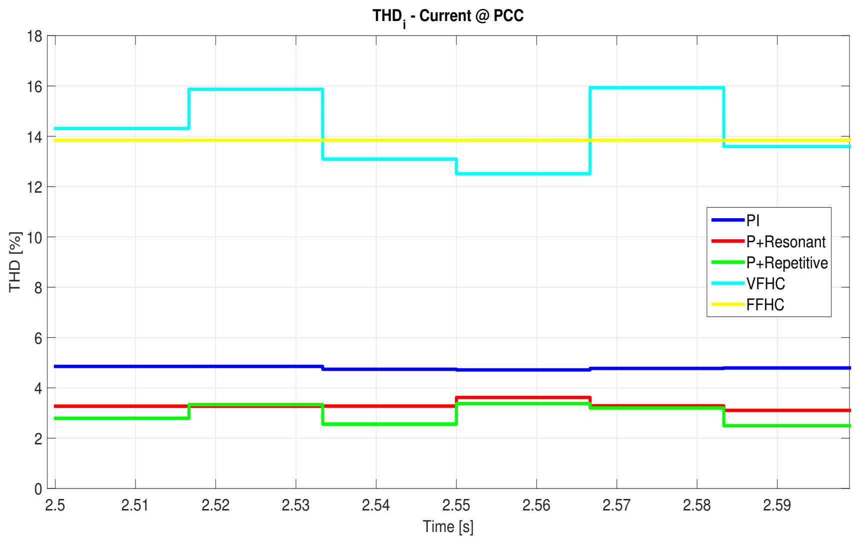


Figure 35 – THD_i comparison for current controllers.

4.5.3 Processing Time of Current Controllers

An important feature to be considered for current controllers is their computational effort in respect to a real implementation in digital signal processors. In general, it is desired for a controller to demand as little memory allocation as possible, therefore, in a comparative study, controllers presenting lower processing times for their control algorithms would present a more satisfactory feature. To evaluate such condition, the previous four current controllers were then implemented with a TMS320F28335 floating-point DSP. Some other few considerations taken for this experiment are highlighted as follows:

1. The code implemented for each controller was made in C language, considering the use of an auto-code generation tool from PSIM (ALONSO *et al.*, 2017), with tests run in flash memory. Note that this tool has some disadvantages, such as some prebuild libraries and procedures that does not directly offer code optimization and consequently may provide slower processing capabilities;

2. Only the current controllers were implemented, one at a time, disregarding any other algorithms related to matters of initialization of a real SPI or generation of current control reference (other than the following explained);

3. A double update mode has been simulated, resulting in a sampling frequency by the ADC of $f_s = 24kHz$, and a window size for the digital controllers of $M = f_s/60 = 400$ positions, unless said contrariwise;

4. Since, for the application here tested, the VFHC requires higher sampling frequencies than 24 kHz, this controller is neglected in the following comparison. Besides, as aforementioned, since the VFHC has the same operational procedure of the FFHCs (i.e., as in a set-reset flip-flop), only this last is taken as an exemplification for the processing time of classic hysteresis controller methodologies.

To determine the processing time of each controller, a "set-bit $\rightarrow$ clear-bit" routine was adopted. It means that, once an ADC interruption is triggered, an output pin of the processor is set to high (+3V), and before closing the interruption, the same pin is set to low state (0V). This experiment indicates the amount of time required for processing all the instructions of the respective controller analyzed at that instant. The results of this test are summarized in Fig. 36.

It can be noted that the FFHC presented the lowest processing time ($t_{C_i} = 1.96\mu s$) among all controllers tested. This is indeed the expected result since its operation is only based on comparisons between the actual current value of the SPI with a given hysteresis band. The PI controller comes as second with $t_{C_i} = 2.17\mu s$, demanding approximately 5.30% of the processing window size considering $f_s = 24kHz$. In regard to the PRes controller, it occupied around 20.30% of the DSP capacity with $t_{C_i} = 8.227\mu s$. In a brief comparison, if one remind the discrete implementation of the PI (eq. (4.5)) and PRes (eq. (4.12)) controllers, it is clearly seen that the PRes has more iterations with the error and delayed modulation signals, which implies in requiring more processing time. In addition, the higher is the number of designed resonant frequencies, the longer is the processing time for this last controller (the same seven resonant orders discussed in Chapter 3 were tested here).

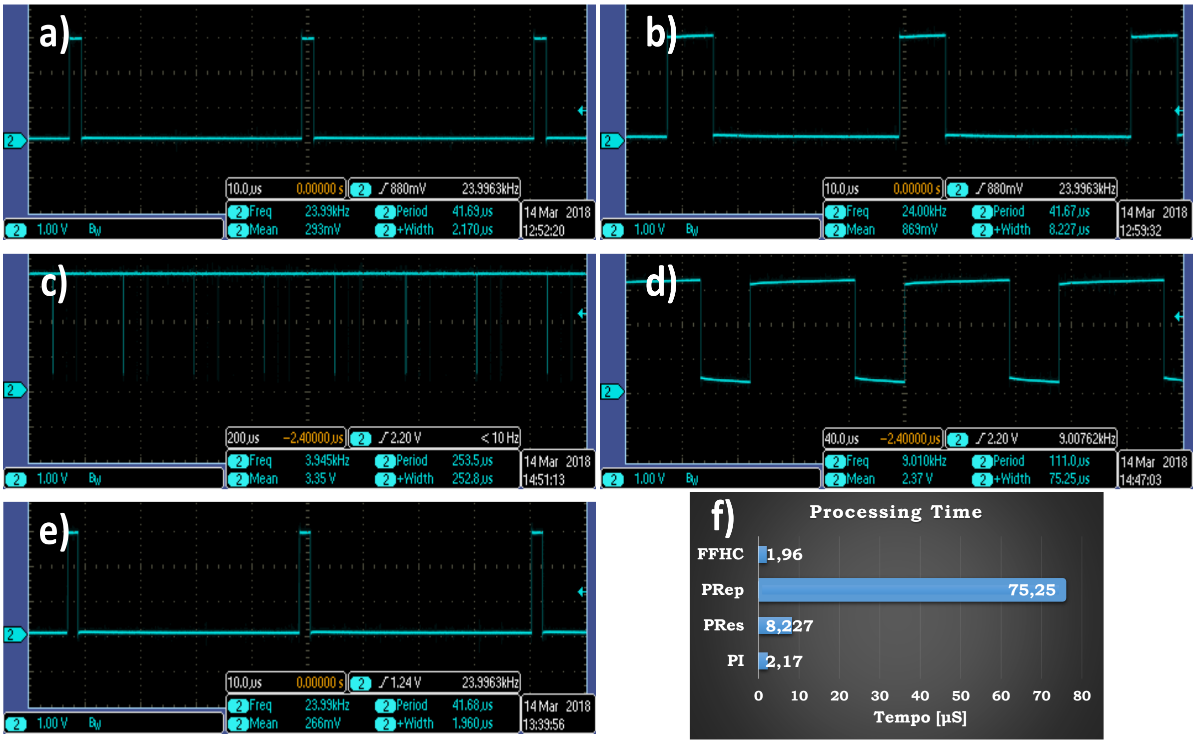


Figure 36 – Processing time experiment for current controllers: (a) PI; (b) PRes; (c) PRep; (d) PRep with $f_s = 9kHz$; (e) FFHC; (f) Comparative perspective.

PRep regulators are a particular case of this analysis, since the time to process its instructions is proportional to the window size (N) used on the cosine transform. For instance, as shown in Fig. 36-c, running the PRep controller with a high value of "N" ($N = M = 400$), there are too many instructions to be performed and it was not possible to fit this processing time within the interruption period of the ADC, not allowing the implementation of the controller. However, if the sampling frequency is reduced to, for instance, $f_s = 9kHz$, as shown in Fig. 36-d, the processing time is enough for the implementation of such regulator, with $t_{C_i} = 75.25\mu s$. The code considered variable with eight decimal digits for the floating-point processor. Note that, as done in (MATTAVELLI; MARAFAO, 2004), switching frequencies of around $10kHz$ should be enough to implement such controllers. Moreover, (MATTAVELLI; MARAFAO, 2004) also mentions that the window size considered for the cosine transform may be reduced up to $N = 50$ without losing the effectiveness of the controller.

As main conclusion of the above-mentioned discussions, it can be doubtlessly said that, in relation to the studied methodologies, the PRep, along with PRes present the best responses on the employment of current controllers for APFs and multifunctional SPIs focused on harmonic elimination in networks. The final decision of the most adequate controller to be considered for the herein sequence of this dissertation is then made between these two methodologies. Knowing that both regulators present satisfactory error and THD_i evaluations, the final choice is taken in regard of the computational costs of their respective digital implementation. Since PRep controllers require more significant processing capabilities, the PRes methodology is the chosen one for further implementation.

Hierarchical control methodologies for distributed systems are, in general, totally dependent on the reliable activity of each layer of its topology. The possibilities and discussions about current regulators appeared here, therefore, to emphasize that most of these approaches may be adequately employed locally on the primary level of a coordination scheme for distributed SPIs in a microgrid. Within the scope of this particular dissertation, since PRes current controllers are said to be the most suitable for the first layer of the proposed hierarchical strategy, they are herein used being driven by current references given by a secondary controller on an upper layer.

5 Secondary Control of DERs

Management of DERs based on hierarchical architectures are defined by scalable layers, in which the upper ones are responsible for providing their respective lower ones with operation setpoints (GUERRERO *et al.*, 2013; BIDRAM; DAVOUDI, 2012). As an example for that statement, it can be considered that primary level controllers of multifunctional SPIs conduct their adequate power flow interaction with a PCC under the orientation of control commands coming from a secondary layer, which does so according to pre-established power quality or energy generation goals (OLIVARES *et al.*, 2014) in the tertiary upper level. Having that in mind, it becomes clear the importance of designing a robust secondary control methodology, since it can make management of distributed system become inconceivable.

Among many possibilities of secondary controls, as briefly brought in the state-of-art discussions, herein attention is particularly given to a master-slave approach that relies on a new methodology of coordination based on current terms. Firstly, the adoption of a master-slave system relies on its interesting ability to coordinate the lower primary layer by being able to incorporate plug-and-play devices into a distributed architecture, without suffering with dynamic changes in the controllability of the entire electrical system.

Furthermore, secondary control based on analysis and dispatch of power components, as in the Power-Based Control (CALDOGNETTO *et al.*, 2015b), has been considered a compelling master-slave alternative, allowing central controllers to effectively coordinate several other distributed resources. Cooperative operation of active agents, by means of a master central controller, has also been proved efficient for power quality enhancement in low-voltage grids through an association named Power Quality Interface, under a novel demand-sharing methodology (LIBERADO, 2017).

Secondly, much has been discussed in literature for this and other mainstream power related approaches, nonetheless, there still remains a gap regarding the consolidation and assessment of proposals for distributed master-slave topology based on the sharing of electrical current components. Therefore, aiming to fulfill this still not well explored secondary control possibility for DERs, the herein called Current-Based Control (CBC) algorithm is presented as the main contribution of this dissertation.

This Chapter describes where this methodology of secondary control is grounded in, how it is able to take advantage of a master-slave topology to coordinate DERs, and also how it can be adopted in power quality interventions as in the focus of this dissertation, which is harmonic mitigation in low voltage networks.

5.1 The Current-Based Control

The most general idea behind the Current-Based Control (CBC) algorithm, which operates based on a master-slave topology and the premises of global goals acquired from possible upper control layers on the electrical network or microgrid, is to perform a centralized analysis of currents flowing through the PCC. Hence, for an adequate operation of the CBC, there must exist a system architecture where there is a central processing unit, called central controller (CC), and other slave units, which comprise DERs. By aggregating their multifunctional switching power interfaces with a communication module linked to the CC, and also with integration of energy storage systems (ESS), such DERs are then particularly renamed as energy gateways (EGs) (CALDOGNETTO; TENTI, 2014). Since energy storage is not directly approached in this work, an EG is herein generally defined by a DER (with multifunctional SPI) plus a communication module.

The architecture of the CBC may be easily understood if one reminds Fig. 2, but now instead, current quantities are being exchanged with the central processing unit. The herein adopted microgrid structure, as shown in Fig. 37, places the CC preferably close to the corresponding substation or coupling transformer, being implemented at the PCC or inside grid-forming converters, such as the aforementioned Utility Interface (BRANDAO, 2015). Advantages of this topology are given once SPIs are driven as current controlled sources, what is generally adopted for commercial inverters, also not requiring changes in the control algorithm whether in grid-connected or islanded condition. Voltage controlled source approaches could be implemented likewise, just by adjusting their respective generated voltage to follow a given current control reference (ROCABERT *et al.*, 2012).

To plainly explain the functioning of the CBC, its operation is broken down into three stages responsible for the fulfillment of the following needs of this centralized control methodology:

1. *Local Evaluation of Electrical Quantities*: At this step, for the purposes of power quality evaluation and synchronism, the voltages at each active node of the network (PCC and DERs) are decomposed by a time domain approach, allowing the identification of

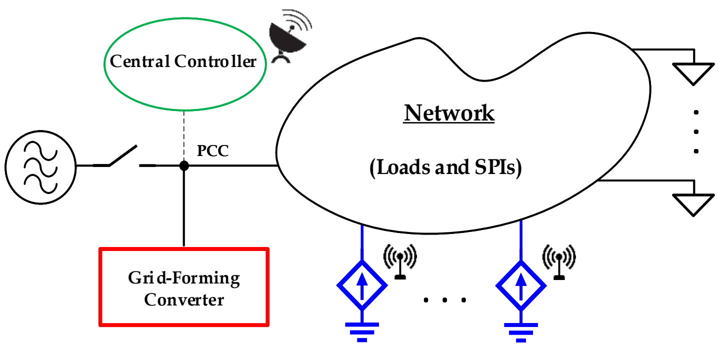


Figure 37 – Centralized network infrastructure.

in-phase and quadrature current terms for a set of selected harmonic frequencies. Afterwards, peak values of currents for each selected harmonic are detected for later use;

2. *Data Collection and Transmission*: Master-slave topologies rely on the transmission of data among active nodes of the control scope. Therefore, it is of importance the definition of how the information manipulated by the CBC flows around the participating units;

3. *Processing and Delegation of Setpoints*: The CBC algorithm is here discussed focusing on control purposes, presenting how it performs the processing of gathered information, doing it based on global goals. The respective processing results are then translated into setpoints for the operation of EGs, directly impacting power quality and energy flow conditions at the PCC.

An overview of the CBC operation, considering the stages abovementioned is shown in Fig. 38. From such representation, it becomes easier to understand where local evaluations are found in a distributed system, as well the paths of data transmission. Yet, it is shown the centralization of control data, and the broadcasting of operation setpoints. Note that, since the centralized coordination scheme is based on a closed-loop strategy, the CC periodically requires the obtainment of data related to the operational status of distributed units. That implies that the secondary controller implemented at the CC must present lower sampling frequency than the one adopted for the primary level controllers. In realistic applications this means that the CC's income data is usually sampled following a few cycles of the fundamental voltage frequency, or can even be implemented based on event-triggered methods (FAN *et al.*, 2017).

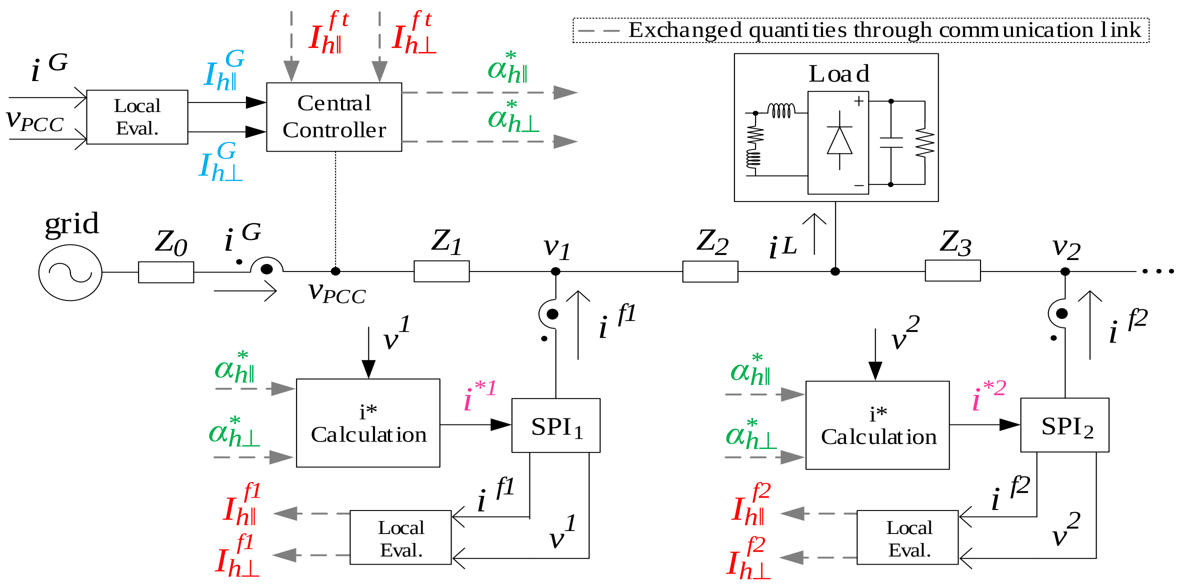


Figure 38 – Scheme of current sharing for the Current-Based Control.

5.1.1 Local Evaluation of Electrical Quantities

The CBC methodology presents an intrinsic useful selective *modus operandi*, since it bases itself on the identification of a set of most critical harmonic components of voltages at a targeted node. As presented in the following discussions, such decoupling of harmonic terms is based on a synchronization algorithm employed along with a peak detection scheme. When compensation of undesired terms at the PCC is the main goal of the centralized control, for instance, the CBC's selective capability may be employed as a powerful tool for the generation of control references for SPIs (BRANDAO *et al.*, 2016). The harmonic identification is investigated in this work, in a time domain approach, by means of a phase-locked loop (PLL), just as in the synchronism algorithm discussed in Section 3.6, and a further implementation of moving average filters for the detection of amplitude (peak) values of fundamental and harmonic currents.

Let's consider the same synchronization output angle (θ) of the block diagram from Fig. 8. Each active node uses its local voltage measurement as input for a locally processed PLL algorithm, considering the same methodology as before, aiming the detection of the synchronism angle θ_1 of the fundamental voltage component. This angle is then used as a reference for the detection of other θ_h angles, respective to the multiple harmonic frequencies selected, following the definition given by eq. (5.1). An interesting consequence of this approach is that, even if applied to systems under non-sinusoidal conditions, the PLL is able to provide a robust response for the synchronism angles (PADUA; MARAFAO, 2005).

$$\theta_h = h \cdot \theta_1 \tag{5.1}$$

Once in possess of such angles, through the calculation of cosines and sines, the in-phase and quadrature terms of the "h" harmonic selected, defined respectively as $x_{h_{||}}$ and $x_{h_{\perp}}$, may be attained. The definition of in-phase and quadrature terms for each harmonic order stands for the classical Fourier Series definition (DAS, 2015a), where a time periodic signal $f(t)$ with period T, is given by a sum of sine and cosine terms of its "h" frequencies, with amplitudes a_h and b_h, plus a mean value (a_0), as shown in eq. (5.2). Yet, the sine and cosine calculations of these two orthogonal quantities are related to eq. (5.3), which is the phasor representation of the discussed quantities.

$$f(t) = a_0 + \sum_{h=1}^{\infty} a_h \cdot \cos\left(\frac{h \cdot 2\pi t}{T}\right) + \sum_{h=1}^{\infty} b_h \cdot \sin\left(\frac{h \cdot 2\pi t}{T}\right) \tag{5.2}$$

$$e^{jhw_o t} = \cos\left(hw_o t\right) + j \cdot \sin\left(hw_o t\right) \tag{5.3}$$

The following step on the evaluation of local electrical quantities is, therefore, the processing of the in-phase (cosine related) and quadrature (sine related) references, which present unitary amplitude, being given by the Fourier representation and attained through the synchronization angles of each desired harmonic order, as presented in Fig. 39.

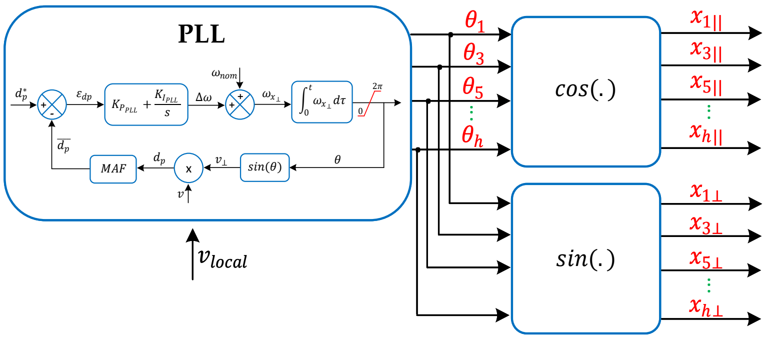


Figure 39 – Local detection of synchronization angles and reference signals for the CBC.

In general power conditioning applications, the mentioned set of multiple frequencies is composed of the lower even harmonic orders, or the most impacting harmonics present at the grid electrical quantities. However, the number of harmonic components and their respective orders must be taken in a case-by-case scenario, where the goals of the distributed operation should predominate on their choice.

By having the references of the in-phase and quadrature terms, the electrical current measured on each respective node is then used locally for the detection of peak values of fundamental and harmonic components. This peak detection occurs following a Fourier analysis, in which the previous a_h and b_h amplitude terms are calculated in function of a given period signal $x(t)$ as in eq. (5.4) and eq. (5.5).

$$a_h = \frac{2}{T}\int_0^T x(t)\cdot\cos\left(\frac{h\cdot 2\pi t}{T}\right)\cdot dt \tag{5.4}$$

$$b_h = \frac{2}{T}\int_0^T x(t)\cdot\sin\left(\frac{h\cdot 2\pi t}{T}\right)\cdot dt \tag{5.5}$$

Hence, based on this definition and considering the current (i_{local}) of each distributed active node of the microgrid, the in-phase ($I_{h_{||}}$) and quadrature ($I_{h_{\perp}}$) peak currents, respective to each "h" harmonic order, are then calculated by eq. (5.6) and eq. (5.7).

$$I_{h_{||}} = \frac{2}{T}\int_0^T i_{local}\cdot\cos\left(\frac{h\cdot 2\pi t}{T}\right)\cdot dt = \frac{2}{T}\int_0^T i_{local}\cdot x_{h_{||}}\cdot dt \tag{5.6}$$

$$I_{h_{\perp}} = \frac{2}{T}\int_0^T i_{local}\cdot\sin\left(\frac{h\cdot 2\pi t}{T}\right)\cdot dt = \frac{2}{T}\int_0^T i_{local}\cdot x_{h_{\perp}}\cdot dt \tag{5.7}$$

One can note that this definition of peak value of a periodic signal is then possible to be digitally implemented by means of simple moving average filters (MAF). As a consequence of using MAFs in such task, it must be said that the peak identification of the current terms is given by average values. Therefore, due to simplicity and matters of minimizing computational burden, this methodology is herein adopted in the CBC algorithm, allowing later generation of current references for SPIs following the arrangement shown in Fig. 40. Nonetheless, this arrangement is capable of attaining satisfactory results, when compared to general approaches of peak detection by Fast Fourier Transform (FFT) methods (OPPENHEIM; SCHAFER, 2009).

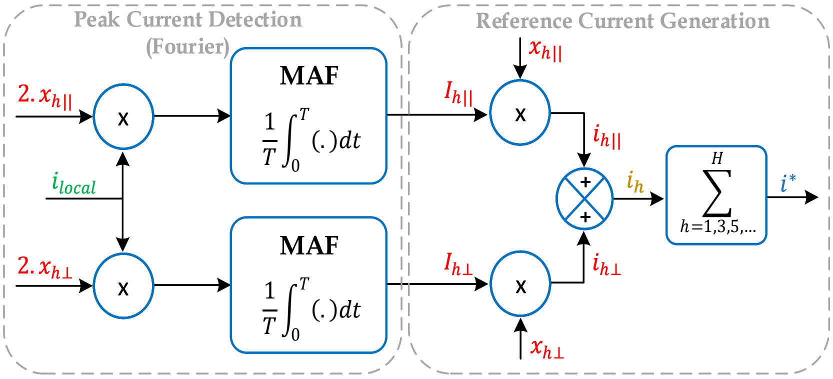


Figure 40 – Scheme for peak current detection and reference generation.

Besides, depending on how $x_{h_{||}}$ and $x_{h_{\perp}}$ interact with the local current (i_{local}), the peak currents identified by this arrangement can also be adequately represented by positive or negative values.

At any instant, the CBC methodology allows the currents to be restored to time domain by following eq. (5.8).

$$\begin{cases} i_{h_{||}} = I_{h_{||}} \cdot x_{h_{||}} \\ i_{h_{\perp}} = I_{h_{\perp}} \cdot x_{h_{\perp}} \end{cases} \tag{5.8}$$

This may be an interesting feature for cases when one wants to be sure of the adequacy of the generated peak references. Yet, an even more interesting feature of such definition is that it can be used for synthesizing current references (i^*) for multifunctional operations of those dispersed SPIs. By taking advantage of such references, current compensation is achieved at the PCC in a selective way, since the i_h terms can be chosen as desired and gathered by eq. (5.9).

$$i^* = \sum_{h=1,3,5,...}^{H} i_h \tag{5.9}$$

A simplified practical example is presented with the intention of better explaining how the CBC processes the in-phase and quadrature reference signals, peak current values and reference current generation. Let's consider the simplified circuit shown in Fig. 41, disregarding electrical losses, comprising an AC voltage source with peak voltage of $100V_{pcc}^{peak}$ supplying a 5Ω resistor, in presence of an ideal parallel current source (representing a SPI able to inject active power) in their intermediate node. In Fig. 42-a time domain analysis of the mentioned calculations performed by the CBC in this circuit, with a CC allocated at the PCC, is demonstrated.

Up to 1.05 seconds, no intervention occurs by the SPI, resulting in an in-phase current supplied by the power source with amplitude of $20A$. The AC voltage source measurements are used on a PLL, attaining the unitary in-phase and quadrature reference signals. The PCC current and unitary reference signals are then used for detecting the peak values of this current

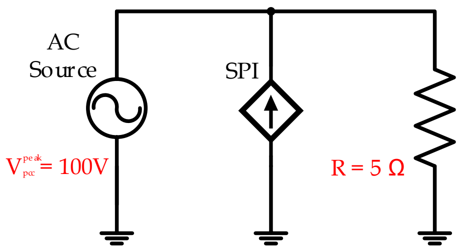


Figure 41 – Ideal circuit for explanation of the CBC peak current detection methodology.

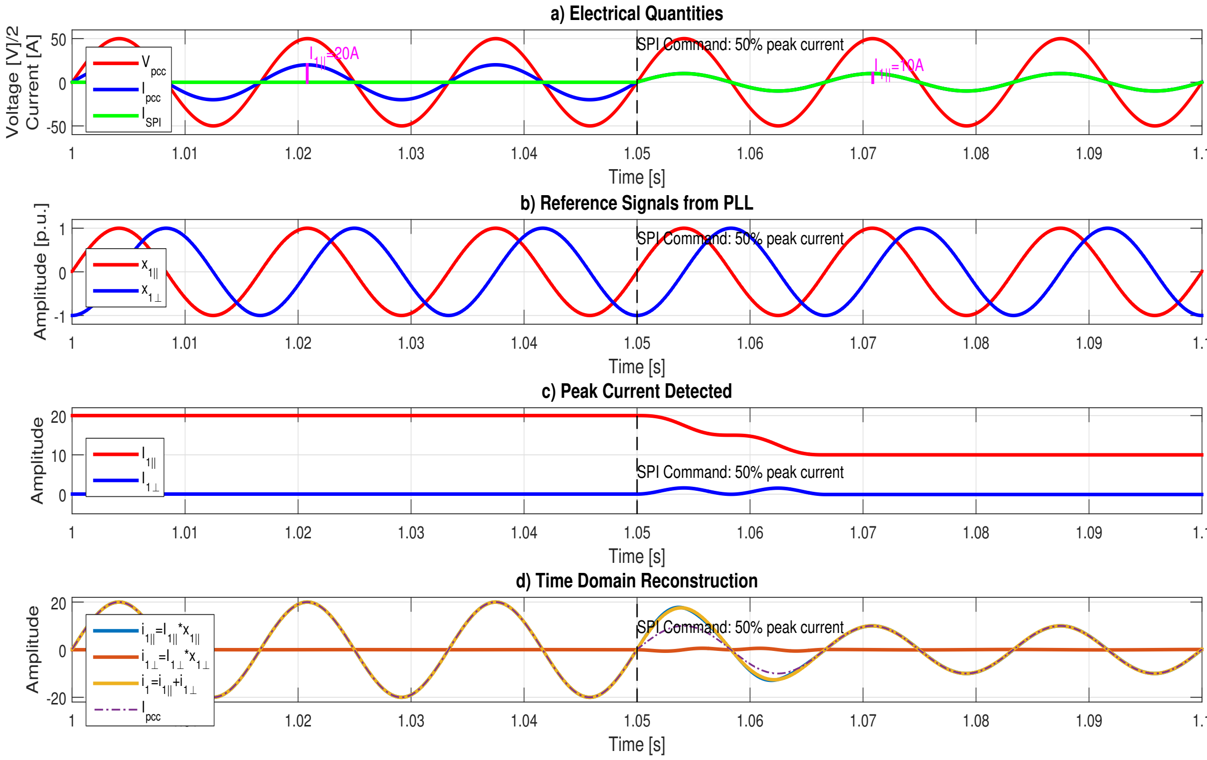


Figure 42 – CBC peak detection methodology and time domain reconstruction.

following the mentioned Fourier decomposition, as seen in Fig. 42-c. Since this is a purely resistive scenario, only the fundamental in-phase peak value ($I_{1_{||}}$) is not null; quadrature and harmonic terms would appear in presence of reactive/inductive impedance or nonlinear loads. The analysis here presented would be exactly the same for any of those components. It can be noted in the simulated result how the peak value matches the local (PCC) reference current amplitude.

Having the unitary reference signals and peak values of such current, it is possible to generate control references in abc frame to be sent to the SPI. For instance, after 1.05 seconds, the SPI is commanded to inject an in-phase current with half of the peak value detected in the PCC current ($i^* = 0.5 \cdot I_{1_{||}} \cdot x_{1_{||}}$). Consequently, 50% of the amount of current is now demanded by the grid, resulting in a quantity with amplitude equal to $10A$ at the PCC. It is shown that the current reconstruction also matches the real quantity. If one pay attention to this 50% amount of current demanded for this given example, it relates to a scaling coefficient which determines the peak current proportion to be injected by the targeted harmonic term (which in this case was the fundamental in-phase component $I_{1_{||}}$).

As later explained in detail, the CBC algorithm output feeds the primary layer of each local controller with such related scaling coefficients for in-phase and quadrature terms, which are herein called $\alpha^*_{h_{||}}$ and $\alpha^*_{h_{\perp}}$. Moreover, to attain a coordinated operation, these coefficients must account for not only the PCC current (as done in this example) but also for the amount of current being shared among the distributed SPIs. Yet, the peak value to be scaled by the α^*_h setpoints must be given in relation to the particular local current capability of the n-th SPI, herein called ΔI^n, since several elements with different power ratings might be connected to the microgrid and should not operate over their nominal limits.

As a conclusion, in a realistic and distributed scenario with several SPIs, a procedure similar to the one presented in the previous example has to occur at the CC and locally at each active node, due to the presence of line impedances and phase deviations. Furthermore, for providing a balanced and coordinated operation of these EGs, the following explained second and third stages of the CBC operation have to be performed as well. By having this abovementioned first stage processed adequately, the EGs may finally start to exchange data towards the CC, leading to the current sharing proposed by the CBC algorithm. The Pseudocode 1 gives an overview about how this local evaluation of electrical quantities occurs at each EG, and also briefly introduces how coordinated current references can be synthesized for SPI's inner loop controllers. Note that, as many discussions about the CBC (which are made in the following stages) are needed to fully understand the final equation responsible for the current synthesis of the n-th SPI, it is generalized at this point as i^{n*}. Besides, to clearly present the intended ideas, herein the in-phase ($I_{h_{||}}$) and quadrature ($I_{h_{\perp}}$) local peak currents of the n-th SPI are named ($I^{fn}_{h_{||}}$) and ($I^{fn}_{h_{\perp}}$) respectively.

5.1.2 Data Collection and Transmission

The hierarchical control proposed herein, based on a master/slave topology, is inherently dependent on a communication infrastructure. The centralization of the control methodology requires all active distributed units to engage on data exchange with the central controller, providing essential information regarding its nodal electrical conditions and respective power capabilities. Likewise, communication links are used for broadcasting control commands to all those units which contribute to the global goal of the network.

Firstly looking at the EGs, the following information is gathered for the transmission of a data packet to the CC, given their respective reasons:

- *Nominal Currents*: Each "n" active EG has to inform the nominal current capability (peak value) of its SPI, named as I^{fn}_{nom}. This characteristic is relevant for the CBC to assign a contribution to such SPIs that not exceeds their nominal power conditions. Otherwise, either a harmful operation could be expected for the inverter or it could be disconnected

Pseudocode 1 Primary Level Control Methodology in Each EG

Input: Scaling control coefficients from the CC ($\alpha_{h_{||}}$,$\alpha_{h_{\perp}}$)
Output: Current reference for the n-th SPI (i^{n*}) and dispatch of local current quantities to the CC

1: **preload**: LOCALQUANTITIES(v_{local},i_{local})
2: **preload**: READCONTROLDATAPACKAGE( ) ▷ Read CC's transmitted data: $\alpha_{h_{||}}$,$\alpha_{h_{\perp}}$
3: **function** ASSESSCURRENTCAPABILITIES( )
4: $I^{fn}_{max} \leftarrow$ DER's Generation ▷ Computes the max. current able to be generated by the DER
5: $I^{fn}_{nom} \leftarrow$ SPI Nominal Capability
6: QUANTITIESTOCC($I^{fn}_{max}, I^{fn}_{nom}$) ▷ Gather current quantities to send to CC
7: **end function**
8: **function** PRIMARYLEVELCONTROL( )
9: $i^{n*} \leftarrow 0$ ▷ The reference current of control cycle "k" is recalculated for "k+1"
10: **for** $h \leftarrow 1$ to H **do** ▷ For all harmonic orders targeted
11: **if** $h = 1$ **then** ▷ Compute active and reactive power injection
12: $\Delta I^n \leftarrow I^{fn}_{max}$ ▷ Power generation is available at the DER
13: **if** $\Delta I^n > 0$ **then** ▷ Priority is given to max. active power as possible
14: $i^{n*}_{h_{||}} \leftarrow \alpha_{h_{||}} \cdot \Delta I^n \cdot x_{h_{||}}$ ▷ Compute the fundamental in-phase term
15: **else**
16: $i^{n*}_{h_{||}} \leftarrow 0$ ▷ No active current is available
17: **end if**
18: $\Delta I^n \leftarrow I^{fn^2}_{nom}$ ▷ Limit capability is the nominal current rating
19: **goto** Line 27 ▷
20: **else**
21: $\Delta I^n \leftarrow \Delta I^n - I^{fn^2}_{(h-2)_{\perp}}$ ▷ Recalculate actual current capability
22: **if** $\Delta I^n > 0$ **then**
23: $i^{n*}_{h_{||}} \leftarrow \alpha_{h_{||}} \cdot \sqrt{\Delta I^n} \cdot x_{h_{||}}$ ▷ Compute the "h" order in-phase term
24: **else**
25: $i^{n*}_{h_{||}} \leftarrow 0$
26: **end if**
27: $\Delta I^n \leftarrow \Delta I^n - I^{fn^2}_{h_{||}}$ ▷ Recalculate actual current capability
28: **if** $\Delta I^n > 0$ **then**
29: $i^{n*}_{h_{\perp}} \leftarrow \alpha_{h_{\perp}} \cdot \sqrt{\Delta I^n} \cdot x_{h_{\perp}}$ ▷ Compute the "h" order quadrature term
30: **else**
31: $i^{n*}_{h_{\perp}} \leftarrow 0$
32: **end if**
33: **end if**
34: $i^{n*} \leftarrow i^{n*} + i^{n*}_{h_{||}} + i^{n*}_{h_{\perp}}$ ▷ Final local reference for the SPI
35: QUANTITIESTOCC($I^{fn}_{h_{||}}, I^{fn}_{h_{\perp}}$) ▷ Gather current quantities to send to CC
36: $h \leftarrow h + 2$ ▷ Only odd terms
37: **end for**
38: DISPATCHQUANTITIESTOCC( ) ▷ Dispatch gathered current quantities to CC
39: **end function**

from the grid under safety regulations (KELLER; KROPOSKI, 2010; MARAFAO *et al.*, 2018);

- *Maximum Currents*: Knowing that the energy flowing from each EG relies on DERs, it is fundamental for the central processor to know what is the maximum amount of electrical peak current (I^{fn}_{max}) that could be made available for the grid at that moment. Note that I^{fn}_{max} is related to only the maximum current that could be generated by the related DER for active power transfer purposes. This quantity is required since generation of active current may be limited or intermittent, and also because injection of any other of those current terms (reactive or harmonic) may not be locally allowed by standards, DSOs or even DER owners (CPUC, 2013).

- *Local Electrical Quantities*: As discussed in the first stage of the CBC operation, the processed current terms of each node, comprising the peak values of each "h" component being currently injected by the SPI, are as well required to be transmitted to the CC. Such quantities are needed for providing a feedback loop, in which the CC can rely on for updating how the current sharing occurs along the network, and how new setpoints will be determined. It is highlighted that, since an aforementioned centralized hierarchical control infrastructure manages the microgrid and its devices operation, the loss of this feedback loop would directly impacts on the termination of the coordination of distributed SPIs. However, the primary control layer implemented in each SPI can regulate its operation as in any other converter following the local goals given by an owner/regulator. Therefore, in brief, if the data transmission link fails for any reason, the distributed coordinated control is not performed, but the SPI maintain a robust operation under a local management mode. The main conclusion of such discussion is related to the maintainability of the electrical system stability, operating just as in the Power-Based Control coordination method (CALDOGNETTO *et al.*, 2015b).

Regarding the CC data transmission, it is essentially composed of control commands that are processed by the CBC algorithm, and then delegate duties for the network's dispersed inverters. A cooperative operation of such SPIs is therefore attractive, due to the ability of this control scheme to provide operation setpoints for all units, without knowledge of any grid parameters, and being plausible for plug-and-play inverters. In regard to grid parameters, the most interesting feature is related to independence from knowing line impedances among nodes, contrariwise to some droop control techniques (MICALLEF *et al.*, 2017). A generalized scheme of the data transmission among CC and EGs is presented in Fig. 43. It is reinforced that the PCC data is attained directly at the CC, since it is coupled at this same node. Nonetheless, as aforementioned, such quantities may also be measured by a grid-forming converter located at the PCC, then requiring an additional connection to the data transmission link.

As can be noted, and also seen in Fig. 38, the amount of essential data exchanged be-

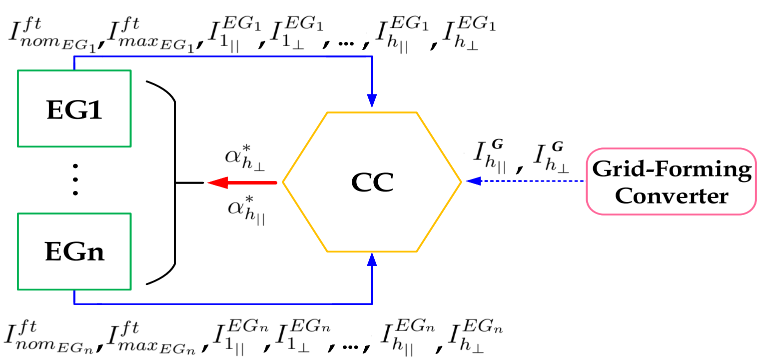


Figure 43 – CBC data transmission scheme.

tween the distributed EGs and the CC is not dense and they are average values. Consequently, allowing many topologies of low-rate communication used in Smart Grids (BUDKA *et al.*, 2014), to be suitable for the CBC implementation. Yet, it is highlighted that this control methodology is satisfactorily implemented defining specific data transmission periods. Transmission intervals in the order of a few fundamental cycles should be enough for an efficient performance. Yet, as reasonable, the faster data packets are transmitted, the better is the system performance. Although, one must be alert that sluggish transmission intervals may impact negatively on to the system's stability, a concern that will be later discussed in this work.

5.1.3 Data Processing and Delegation of Setpoints

After data packages from all active distributed units (slave agents) are collected by the CC, it starts processing such information with the purpose of obtaining operation setpoints that will be dispatched. This process basically consists in determining the actual amount of current provided by the EGs, the maximum current that they can generate, and also what is later expected at the PCC regarding electrical current terms.

The CC initiates the control algorithm determining the total amount of current that is actually being provided by all EGs. This contribution of the "N" EG units takes into account each harmonic order of a pre-selected set determined to be monitored by the system. The current quantities respective to such frequencies are handled considering peak values of in-phase ($I^{ft}_{h_{||}}$) and quadrature ($I^{ft}_{h_{\perp}}$) terms at the actual control cycle "k", as given by eq. (5.10) and eq. (5.11). On the nomenclatures "f" and "t", the former stands for EG's quantity, and the later for the total amount of that quantity considering all the active elements of network. The physical meaning of these sums is a relation of the total amount of current (for in-phase and quadrature terms) that is being injected by SPIs throughout the network, later being used in a comparison with the total current demanded by the load.

$$I^{ft}_{h_{||}}(k) = \sum_{n=1}^{N} I^{fn}_{h_{||}}(k) \tag{5.10}$$

$$I^{ft}_{h_{\perp}}(k) = \sum_{n=1}^{N} I^{fn}_{h_{\perp}}(k) \tag{5.11}$$

Following the same idea, the CC also computes for the network, the total maximum active current availabilities (I^{ft}_{max}) and the nominal current capacities of all EGs together (I^{ft}_{nom}) at the control cycle "k", as shown in eq. (5.12) and eq. (5.13), always based on peak terms.

$$I^{ft}_{max}(k) = \sum_{n=1}^{N} I^{fn}_{max}(k) \tag{5.12}$$

$$I^{ft}_{nom}(k) = \sum_{n=1}^{N} I^{fn}_{nom}(k) \tag{5.13}$$

As aforementioned, an initial stage is performed at the CC before the processing of the CBC algorithm itself, providing the peak current detection of the in-phase and quadrature harmonic terms of the PCC current, which are herein resumed by $I^G_{h_{||}}$ and $I^G_{h_\perp}$ respectively. Such quantities are now important because, if one observes the complete operation of the CBC depicted in Fig. 38, by Kirchhoff's current law (KCL), the intervention of the currents injected by the SPIs of each EG leads to eq. (5.14) and eq. (5.15), where "L" stands for the load current terms demand. Note that the KCL is analyzed at this stage in terms of decomposed terms for each harmonic orders, which means that, the sum of the in-phase or quadrature components of in the load current should be equal to sum of the respective same current components flowing from the SPIs and PCC.

$$I^L_{h_{||}}(k) = I^G_{h_{||}}(k) + I^{ft}_{h_{||}}(k) \tag{5.14}$$

$$I^L_{h_\perp}(k) = I^G_{h_\perp}(k) + I^{ft}_{h_\perp}(k) \tag{5.15}$$

Considering such relationship among nodal currents along the network at a given control cycle "k", interventions may be realized at the PCC, since the current sharing provided by the CBC is able to be employed for the generation of current references, which are used for exploiting the multifunctional capabilities of the dispersed SPIs. For determining the setpoints used for controlling active, reactive and harmonic flow at the PCC, the CBC first estimates the reference current quantities of in-phase and quadrature terms by the relations brought in eq. (5.16) and eq. (5.17). This is done by the differential analysis between the current components present at the grid, on the actual control cycle, and the expected current conditions at the PCC at the next control cycle "k+1". Such desired PCC currents for the next cycle ($I^{G*}_{h_{||}}$) and ($I^{G*}_{h_\perp}$) come from a possible tertiary layer, or are pre-established condition set by the microgrid regulator in the CC. Usually power utilities, also called distribution system operators (DSOs), are the ones responsible for setting the ($I^{G*}_{h_{||}}$) and ($I^{G*}_{h_\perp}$) references.

$$I^*_{h_{||}}(k+1) = I^G_{h_{||}}(k) + I^{ft}_{h_{||}}(k) - I^{G*}_{h_{||}}(k+1) \tag{5.16}$$

$$I^*_{h_\perp}(k+1) = I^G_{h_\perp}(k) + I^{ft}_{h_\perp}(k) - I^{G*}_{h_\perp}(k+1) \tag{5.17}$$

For the sake of better explaining the relationship described in eq. (5.16) and eq. (5.17), an example considers the fundamental in-phase current component as reference and eq. (5.18) simplifies this explanation. When defining the desired active current reference to be shared in the next control cycle ($I^*_{1_{||}}(k+1)$), its first parcel is related to the actual fundamental in-phase current provided by the grid ($I^G_{1_{||}}(k)$) plus a second term, which represents the total amount of actual active current being injected by all distributed EGs ($I^{ft}_{max}(k)$). At last, the PCC current desired on the next cycle for this same in-phase first harmonic component ($I^{G*}_{1_{||}}(k+1)$), which comes from the tertiary level, has to be considered. Note that this third term must be subtracted from the other two parcels aiming at finding the amount of current that still needs to be processed to achieve the desired goal and can be used as reference for scaling the participation of distributed SPIs. Besides, since active current is always the main goal of the EG,

$I^{ft}_{1_{||}}(k) = I^{ft}_{max}(k)$ at all instants. For any other harmonic orders, the same idea can be extended and eq. (5.19) gives another example for the fundamental quadrature (reactive) current reference.

$$I^*_{1_{||}}(k+1) = I^G_{1_{||}}(k) + I^{ft}_{max}(k) - I^{G*}_{1_{||}}(k+1) \tag{5.18}$$

$$I^*_{1_{\perp}}(k+1) = I^G_{1_{\perp}}(k) + I^{ft}_{1_{\perp}}(k) - I^{G*}_{1_{\perp}}(k+1) \tag{5.19}$$

Possessing these current references ($I^*_{h_{||}}$) and ($I^*_{h_{\perp}}$), the CBC algorithm computes the coordinated scaling coefficients that will finally be transmitted to EGs for the generation of their respective SPI's current references. Such control commands for in-phase and quadrature terms, respectively, $\alpha_{h_{||}}$ and $\alpha_{h_{\perp}}$, are attained by relating the reference amount of current components for fundamental terms and all the other harmonic frequencies, with the actual current capability (ΔI) of the entire distributed system (all EGs), as given in eq. (5.20) and eq. (5.21). ΔI is a quantity that represents the total peak current sharing capability of the microgrid considering all the active EGs. This variable is responsible for adequately scaling how the global reference current ($I^*_{h_{||}}(k+1)$) is shared within the network, and must be recursively calculated in each control cycle after each harmonic order term is processed, avoiding SPIs operating under overcurrent conditions.

$$\alpha^*_{h_{||}} = \frac{I^*_{h_{||}}(k+1)}{\sqrt{\Delta I}} \tag{5.20}$$

$$\alpha^*_{h_{\perp}} = \frac{I^*_{h_{\perp}}(k+1)}{\sqrt{\Delta I}} \tag{5.21}$$

An example is now given to clarify how the parameter ΔI is obtained. Let's consider the beginning of a control cycle "k", with a microgrid where its EGs sum a global nominal current capability of $I^{ft}_{nom} = 10A_{peak}$ and that the total maximum active current generated by all DERs is $I^{ft}_{max} = 8A_{peak}$. Also it is considered that the hierarchical controller demands the SPIs to engage on ancillary services, sharing the goal of compensating $4A_{peak}$, $3A_{peak}$ and $2A_{peak}$, respectively for the fundamental in quadrature and third harmonic in-phase and quadrature components. An algorithm presented in sequence is shown to facilitate the understanding of this example. It can be noted that, as active current injection is in general taken as priority for any DG, ΔI is first considered as the total amount of current generated by DERs that has to be injected into the grid. Having such value, the scaling coefficient ($\alpha^*_{1_{||}}$) for this harmonic component can be calculated using eq. (5.20). The initial logic of this algorithm takes into consideration that the SPI is adequately designed for its EG, resulting that $I^{ft}_{max} \leq I^{ft}_{nom}$ at any instant.

Therefore, ΔI has to be recalculated to process the sequential fundamental quadrature term. The remaining actual current capability is given by the difference between the nominal rating of the SPI and the amount previously allocated for the fundamental in-phase term. After calculating $\alpha^*_{1_{\perp}}$, ΔI is similarly recalculated for the third harmonic component. Note that, since

1: $\Delta I = I_{max}^{ft} = 8^2 = 64A_{peak}^2 \Rightarrow \sqrt{\Delta I} = 8A_{peak}$ ▷ Capacity used for active current injection
2: $\Delta I = I_{nom}^{ft^2} - I_{max}^{ft^2} = 10^2 - 8^2 = 36A_{peak}^2 \Rightarrow \sqrt{\Delta I} = 6A_{peak}$ ▷ Capacity used for reactive current inj.
3: $\Delta I = 6^2 - 4^2 = 20A_{peak}^2 \Rightarrow \sqrt{\Delta I} = 4.472A_{peak}$ ▷ Capacity used for in-phase 3rd harm. current inj.
4: $\Delta I = (4.472)^2 - 3^2 = 11A_{peak}^2 \Rightarrow \sqrt{\Delta I} = 3.316A_{peak}$ ▷ Capacity used for quadrature 3rd harm. current
5: $\Delta I = (3.316)^2 - 2^2 = 7A_{peak}^2 \Rightarrow \sqrt{\Delta I} = 2.645A_{peak}$ ▷ Remained capacity for other current terms
6: $\vdots$ ▷ Proceed similarly to any other desired harmonic component until $\Delta I = 0$

the CBC algorithm deals with in-phase and quadrature terms, the actual current capability is always recalculated based on a magnitude value of a phasorial quantity. It means that its remaining peak value at each step is given by the square root of the difference between the two orthogonal quantities squared. As noted in the algorithm, the actual capability is likewise recalculated for the 3rd terms targeted. To conclude this example, it is mentioned that, if desired, ΔI could finally be recalculated to allocate any other sequential harmonic components until the total current capability of the system is reached.

Having defined the main features of this secondary control layer approach, the complete CBC algorithm processed at the CC is then presented in Pseudocode 2. It summarizes how the current sharing process occurs for obtaining the control commands α that are dispatched for the distributed SPIs, and then used for the calculation of control references. Some considerations are made in order to further clarify the usefulness of the CBC methodology. The first consideration, which is a reinforcement of the recent discussions about ΔI, states that the calculation of the $\alpha_{h_{||}}^*$ and $\alpha_{h_{\perp}}^*$ the actual current capability must be updated following the computation of each harmonic term. Otherwise, the reference currents generated for the SPIs will likely demand current injection/absorption that exceeds their power capabilities.

Secondly, the main goal of having DERs is to provide active power injection into the grid, resulting that $\alpha_{1_{||}}$ commands are processed first. Therefore, in case the actual power generation is lower than the nominal capacity of SPIs, other commands can be further processed for multifunctional interventions. However, in applications such as the proposal in this dissertation, there are no constraints that prevent the computation of whichever other terms that best attend the global goals of the microgrid. The CBC algorithm can be easily adapted for both attending any logic on the allocation of the current capability, and setting preferences on the injection of specific current terms.

The third consideration is relative to the range of scaling α coefficients. They can be determined as being $-1 \leq \alpha \leq 1$, in which, considering $\alpha_{1_{||}}$ for instance, positive values represent current injection of the respective term by the SPIs, and negative ones define absorbed energy (storage). For $\alpha_{1_{\perp}}$ this range would mean, respectively, injection of inductive or capacitive reactive power. This feature shows that the CBC may be employed in most of, if not all, the discussed operations of smart energy networks (FANG *et al.*, 2012). Yet, only requiring the adjustment of its operation range following the goals of the hierarchical model and the features of present entities. Note that special attention has to be payed to $\alpha_{1_{||}}$. Even though the CC may

Pseudocode 2 CBC methodology at the CC for processing α coefficients

Input: Local electrical quantities (v_{pcc},i_{pcc}) and EGs' quantities ($I^{ft}_{nom_{EG_n}}$,$I^{max}_{nom_{EG_n}}$,$I^{EG_n}_{1_{||}}$,$I^{EG_n}_{1_{\perp}}$,$I^{EG_n}_{h_{||}}$,$I^{EG_n}_{h_{\perp}}$)
Output: Control coefficients to distributed SPIs ($\alpha_{h_{||}}$,$\alpha_{h_{\perp}}$)

1: **preload**: LOCALQUANTITIES(v_{pcc},i_{pcc})
2: **preload**: READEGSDATAPACKAGE( ) ▷ Read EGs' transmitted data: go to Pseudocode 4 in Appendix A
3: **function** CURRENTBASEDCONTROL( )
4:     **for** $h \leftarrow 1$ to H **do** ▷ Compute power availability and α's for fund. and harm. terms
5:         **if** $h = 1$ **then** ▷ Compute active and reactive power injection
6:             $\Delta I \leftarrow I^{ft}_{max}$ ▷ Priority is given to max. active power as possible
7:             **if** $\Delta I > 0$ **then** ▷ Power/current is being generated by the DER at the SPI's DC side
8:                 $\alpha_{1_{||}} \leftarrow$ SATURATION(Eq. (5.20),1,-1) ▷ Compute active fundamental scaling coefficient
9:             **else**
10:                 $\alpha_{1_{||}} \leftarrow 0$ ▷ Generation of active power is not available by DERs
11:             **end if**
12:             $\Delta I \leftarrow I^{ft^2}_{nom} - I^{ft^2}_{max}$ ▷ Each SPI must respect its nominal power
13:             **goto** Line 22 ▷ Second priority is support to reactive power injection
14:         **else** ▷ Compute harmonic terms
15:             $\Delta I \leftarrow \Delta I - I^{ft^2}_{(h-2)_{\perp}}$ ▷ Remaining power for "h" order in-phase term
16:             **if** $\Delta I > 0$ **then**
17:                 $\alpha_{h_{||}} \leftarrow$ SATURATION(Eq. (5.20),1,-1) ▷ Compute "h" order in-phase scaling coefficient
18:             **else**
19:                 $\alpha_{h_{||}} \leftarrow 0$ ▷ No power availability for "h" order in-phase term
20:             **end if**
21:         **end if**
22:         $\Delta I \leftarrow \Delta I - I^{ft^2}_{h_{||}}$ ▷ Remaining power for "h" order quadrature term
23:         **if** $\Delta I > 0$ **then**
24:             $\alpha_{h_{\perp}} \leftarrow$ SATURATION(Eq. (5.21),1,-1) ▷ Compute "h" order quadrature scaling coefficient
25:         **else**
26:             $\alpha_{h_{\perp}} \leftarrow 0$ ▷ No power availability for "h" order quadrature term
27:         **end if**
28:         CONTROLDATAPACKAGE($\alpha_{h_{||}}$,$\alpha_{h_{\perp}}$) ▷ Gather control commands on a package: go to Pseudocode 5
29:         $h \leftarrow h + 2$ ▷ Only odd terms
30:     **end for**
31:     DISPATCHCONTROLDATAPACKAGE( ) ▷ Dispatch control commands to EGs: go to Pseudocode 6
32: **end function**

process $\alpha_{1_{||}} \geq 0$, if APFs coexist with EGs on the integrated cooperative operation of the microgrid, the individual current capability of the formers are always considered null ($I^{fn}_{max_{APF}} = 0$) and they can operate with the outer voltage loop controllers active, allowing safe and adequate operation of the entire system. Analogously, $\alpha_{1_{||}} \leq 0$ can only be implemented in a real application where energy storage systems are present, otherwise such operation could inflict power quality issues (LU *et al.*, 2012).

Finally as fourth point, with the received α coefficients, each EG computes locally the current control references for their SPIs based in eq. (5.22). This definition takes into account the set of selected harmonics "H", respecting the operational limitations of each inverter. From this relation for synthesizing control references, it can be demonstrated why the α coefficients are analogously called scaling coefficients along this work. They provide selective means for scaling the peak values of the local current terms. Note that the ΔI^n is presented by a square root. This is needed because the available current capability is readjusted after every current demand allocation for the in-phase and quadrature terms, which are orthogonal between each

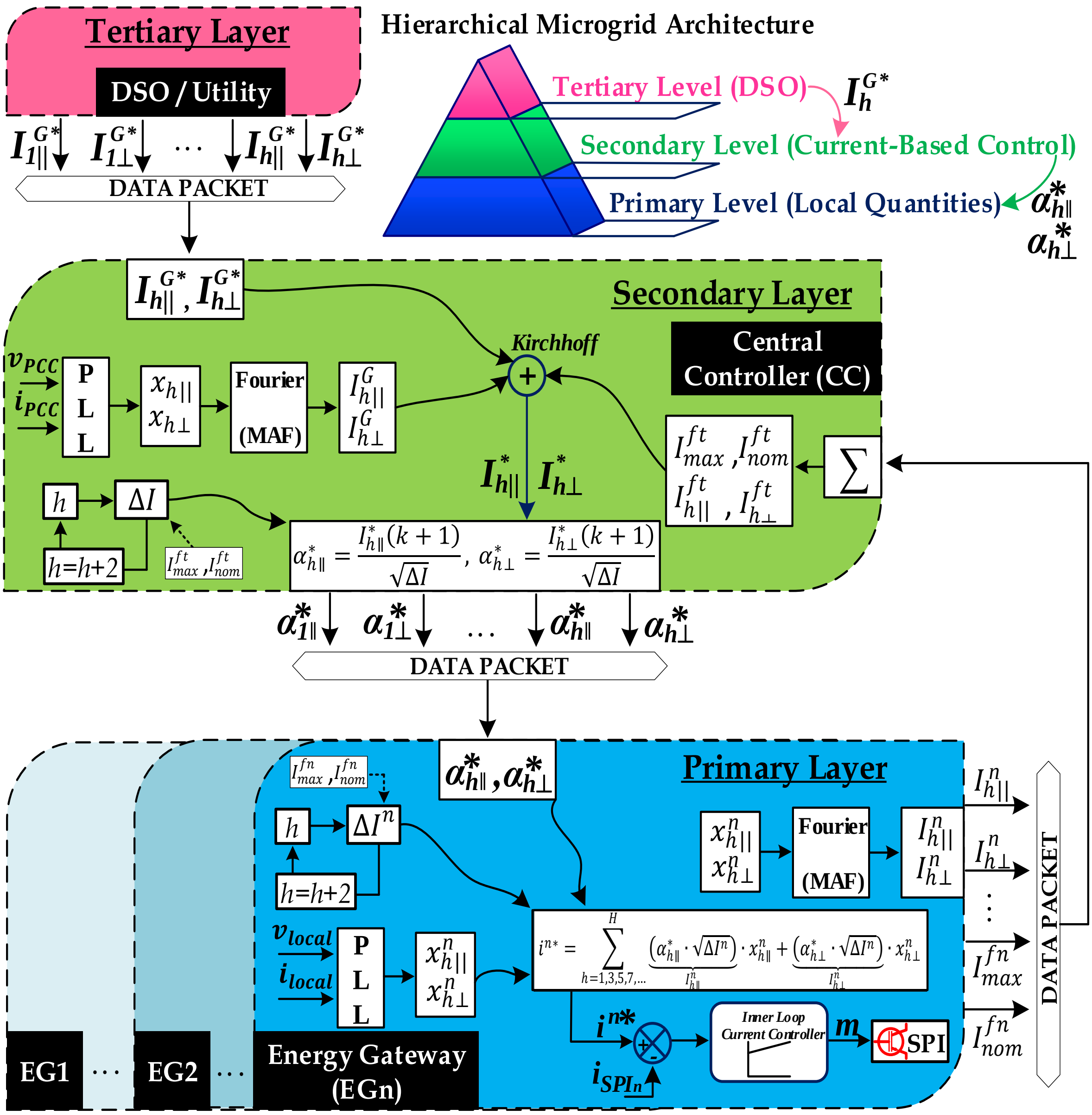


Figure 44 – Summary of the CBC operation in a hierarchical microgrid.

other, just as presented for the ΔI calculation. For instance, after determining the value to be inject by an in-phase term, the respective remaining capability evaluated for the quadrature parcel is given by the residual absolute value.

$$i^{n*} = \sum_{h=1,3,5,\ldots}^{H} \left[\left(\alpha^*_{h_{||}} \cdot \sqrt{\Delta I^n} \right) \cdot x_{h^n_{||}} + \left(\alpha^*_{h_{\perp}} \cdot \sqrt{\Delta I^n} \right) \cdot x_{h^n_{\perp}} \right] \tag{5.22}$$

Aiming at summarizing the methodology proposed by the CBC algorithm, based on a hierarchical microgrid architecture, Fig. 44 is presented. It can be noted how the electrical quantities and control packets flow from and to specific control layers, where a particular approach is realized for each of those quantities.

5.2 Brief Discussion on Constraints

Although the Current-Based Control presents itself as a robust alternative for regulating power flow among distributed units, as any other related methodology, it presents some constraints that, at least until this moment, have not already been completely evaluated, and should be discussed. It is mentioned here two main important features, being related to the characteristics of the electrical conductors and components on the networks, and the transmission means for the current sharing data.

5.2.1 Voltage Phase Deviations

Since the nature of the CBC is related to the resources that are spread out over a microgrid, each node of the network may present voltage phase deviations in relation to the PCC voltage, due to the current flowing through the network's power line impedances. Let's consider a fundamental PCC voltage which presents phase of $0°$, and also that the n-th node of the network presents a phase shift of θ_n° in relation to the PCC node. The SPI current reference locally calculated by eq. (5.22), thus, is now calculated by eq. (5.23).

$$i^{n*} = \sum_{h=1,3,5,\ldots}^{H} \left[(\alpha^*_{h_{||}} \cdot \sqrt{\Delta I^n}) \cdot \cos\left(hwt + h\theta_n^\circ\right) + (\alpha^*_{h_\perp} \cdot \sqrt{\Delta I^n}) \cdot \sin\left(hwt + h\theta_n^\circ\right) \right] \quad (5.23)$$

The relation in this equation leads to the conclusion that, the higher is the harmonic order, the bigger is the voltage phase deviation on the respective node. The example shown in Fig. 45 quantifies that, considering a node with fundamental phase deviation of $\theta_n = 5°$. One can note how the phase deviation is evident among the sinusoidal signals, and also that this difference increases proportionally as the harmonic order rises. For instance, paying attention to the voltage waveforms in Fig. 45, it is noticeable how the synchronism among the signals presents more deviation, in relation to the fundamental term, as the harmonic order increases.

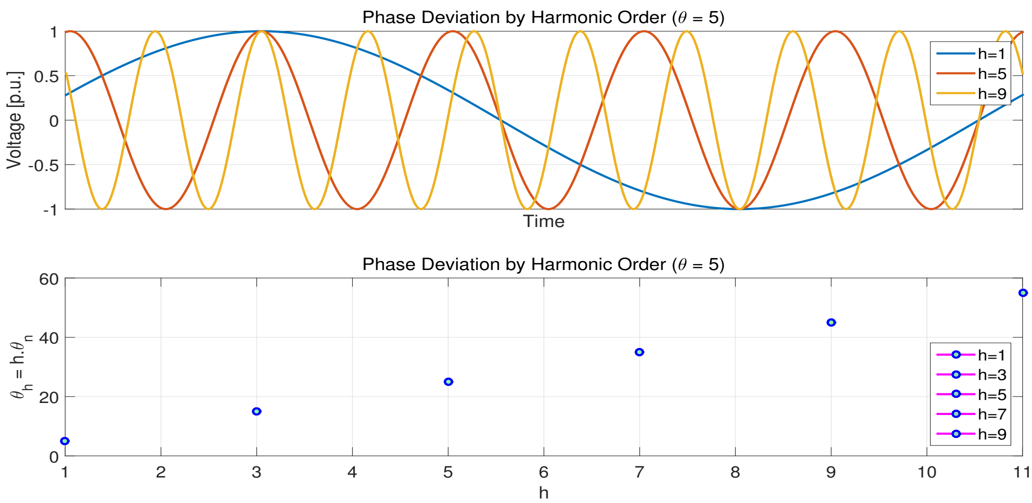


Figure 45 – Impact of harmonic order in phase deviation.

The most critical impact of such condition relates to an error term, which introduces a coupling between the in-phase and quadrature components, and the PCC current. Yet, likely having as consequence, undesired resonances in the vicinity of the system natural frequency, caused by a decrease in the system damping ratio, as $h \cdot \theta_n$ increases. However, this voltage phase error is usually small and can be compensated by an inherent slow closed loop control at the CC for the grid current. Moreover, even if this voltage shift is said to be considerably significant, low-cost synchronophasors (ALMASABI; MITRA, 2016) or GPS can be used for the elimination of such issue. The work presented in (GOLSORKHI *et al.*, 2017), although focusing on power sharing in microgrids based on droop control, discusses an implementation of the mentioned voltage phase error correction through GPS that could be similarly implemented on the CBC algorithm. This methodology would allows to obtain a global reference angle for the hierarchical secondary layer controller, which may be used on improved harmonic decomposition and synchronization of current terms. Lastly, it is also relevant to remember that in case of low-voltage grids, which presents high R/X ratio (ROCABERT *et al.*, 2012), these voltage phase deviations are usually not critical.

5.2.2 Data Transmission Related Issues

Although it is undeniable that the CBC methodology relies on communication infrastructures, its control scheme depends only on a few periodic transmissions of setpoints, also not requiring the gathering of a dense amount of information from the distributed units. This is a positive feature, since it allows this topology to efficiently work using low-rate data links, not involving time-critical communications. Besides, it can accommodate many communication architectures, such as tree-shaped communication topology. Nevertheless, so far, it is already known that the slower or more delayed its two-way communication link is, negative impacts may be evidenced. The higher negative impacts have been initially identified by oscillatory behaviors in the adequate expected system operation and longer accommodation periods.

This is a complex topic, which requires deep immersion on matters of stability analysis of the distributed system and knowledge about communication topologies and data flow issues. As consequence, this study is left as a future work, not being further discussed herein.

5.3 Current Sharing Application Examples with CBC

To test the concepts about the methodology of the CBC, this section brings some simulations carried out with PSIM, demonstrating how the algorithm is effectively used for active, reactive and harmonic control at the PCC. On the PSIM environment, as demonstrated in Fig. 46, a simulation circuitry was created considering a distributed system with two EGs and a nonlinear load. This implementation is a lean version of the topology briefly discussed in Fig. 38.

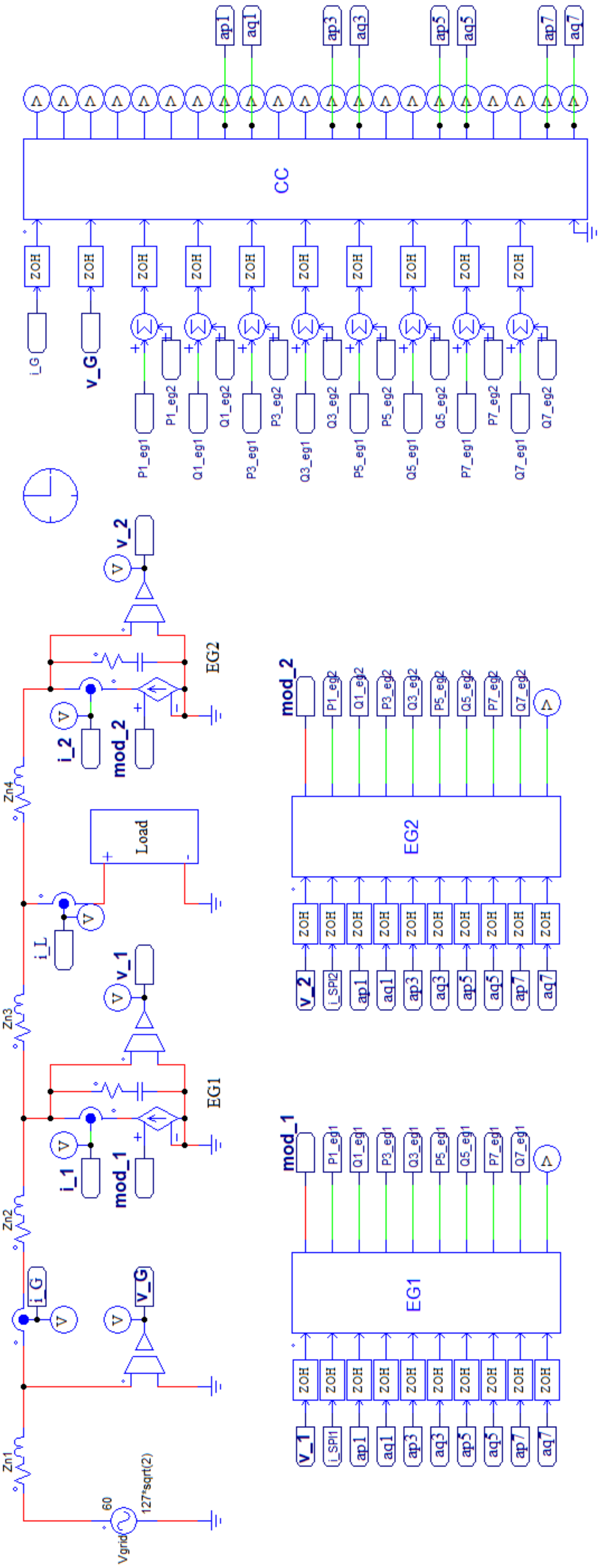


Figure 46 – PSIM circuitry for CBC simulations.

The CBC algorithm was implemented in C language blocks for both the EGs and CC. Since the focus here is only the demonstration of the CBC algorithm, ideal current sources were adopted for representing the distributed SPIs. This is reasonable since inverters operating as current sources are designed to ideally provide unitary static gain. Since this approach was chosen, if the DC link voltage of the SPI was implemented for this case, it could be represented by a constant DC voltage source feeding the parallel DC link capacitor. Realistic examples with grid-tied inverters, designed to operate with LC filters and proportional-resonant controllers, will be presented in the following sections of this work.

Considering a single-phase grid, with nominal phase voltage of $127V$ at $60Hz$, the first EG was then simulated having peak current capability of $33.30A_{peak}$, and the second one of $9.99A_{peak}$. The same nonlinear load mentioned in Chapter 3 was used, disregarding the load step, and the circuit presents equal line impedances (Z_n) of $0.1 + j0.02$.

5.3.1 Active Current Sharing

The most basic applicability of the CBC is the active current sharing control along the network. Considering that the major reason for having DERs in grid-connected mode is active power injection, the CBC can coordinate such demand as shown in Fig. 47. In all the simulations herein, for demonstration purposes, it is taken the assumption that the energy being generated at the DC side of the SPI is constant and is always accessible when required by the energy manager. This can be justified by the fact that, for such short simulation period, about the order of milliseconds, the energy generation and load demand may be said to not vary over time. At all three cases following discussed (active, reactive, and harmonic sharing), the CBC is only commanding the injection of the in-phase and quadrature terms for the respective current parcel (active, or reactive, or harmonic).

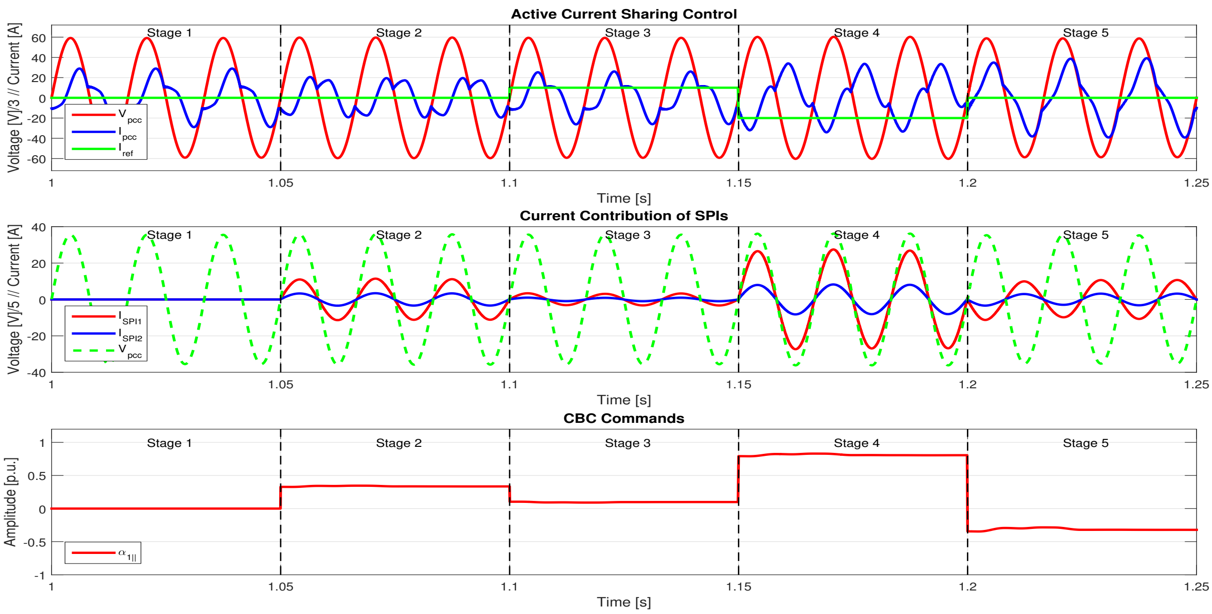


Figure 47 – Active current control at the PCC.

The simulated coordination of the active power flow at the PCC is given as follows. From 1 to 1.05 seconds, the CBC is standing by, not performing any control. After that instant, until 1.1 seconds, it is demanded that distributed SPIs operate cooperatively, following their power capabilities, aiming to obtain zero current active flow at the PCC. Paying attention to the characteristics of the active current sharing performed, it is possible to observe that, as no active current is present at the PCC, only reactive and other nonactive terms remain. It means that the SPIs take responsibility on fully supplying the active current demanded by the nonlinear load. One can also note that, since the second SPI presents higher current capability than the first, the CBC makes this unit have a proportional higher contribution as well.

Between 1.1 and 1.15 seconds, an active reference current at the PCC, $I_{h_{||}}^{G*} = I_{ref}$, of $10A_{peak}$ is set. Thus, one can note how the grid returns to provide an amount of current to the load that is a little over $20A_{peak}$. Since non-active currents are not being mitigated at the PCC current, even with injection of only the fundamental in-phase term, the resultant current is not sinusoidal. Finally, before last stage of the simulation, determined from 1.15 to 1.2 seconds, it is shown how opposite active power flow is performed by the CBC under a reference of $-20A_{peak}$. Although being phase-shifted due to the reactive content, the PCC current is now opposite. This is possible because the SPIs are injecting surplus active current compared to the load demand.

Paying attention to the behavior of $\alpha_{1_{||}}$, one can observe how it changes its amplitude at the adequate moments when new operation setpoints are needed. The final stage of the simulation shows how the CBC operates in case storage systems were present in the circuit. Note that after 1.2 seconds $\alpha_{1_{||}}$ becomes negative, indicating absorption of active current, and consequently, the PCC current increases, once it has to meet the load and the storage demand. As now current is flowing inversely, the SPI active currents must be in opposite phase in relation to the grid voltage.

The application of the CBC for active power flow at the PCC can, therefore, be considered effective, providing also flexibility to adapt itself as orchestrated by the central controller.

5.3.2 Reactive Current Sharing

Let's now take the same simulation as the one for the active power control, however, only selecting the reactive current sharing features of the CBC. This kind of operation is a recent significant matter, since even standards already establish that inverters should provide reactive power control ancillary services, such as described in the IEEE 1547-a amendment (IEEE, 2014b). It is taken a case in which the distributed SPIs should provide, respectively, 50% and 100% of the load reactive current in leading phase shift (capacitive), and later 100% and 50% in lagging current (inductive). Regardless of being related to active, reactive or harmonic current, when said that a SPI provides these respective current parcels, it comprises both the in-phase and quadrature terms. Fig. 48 shows the functioning of such operation.

Analyzing the simulated results it is possible to note that from 1.05 to 1.15 seconds, as

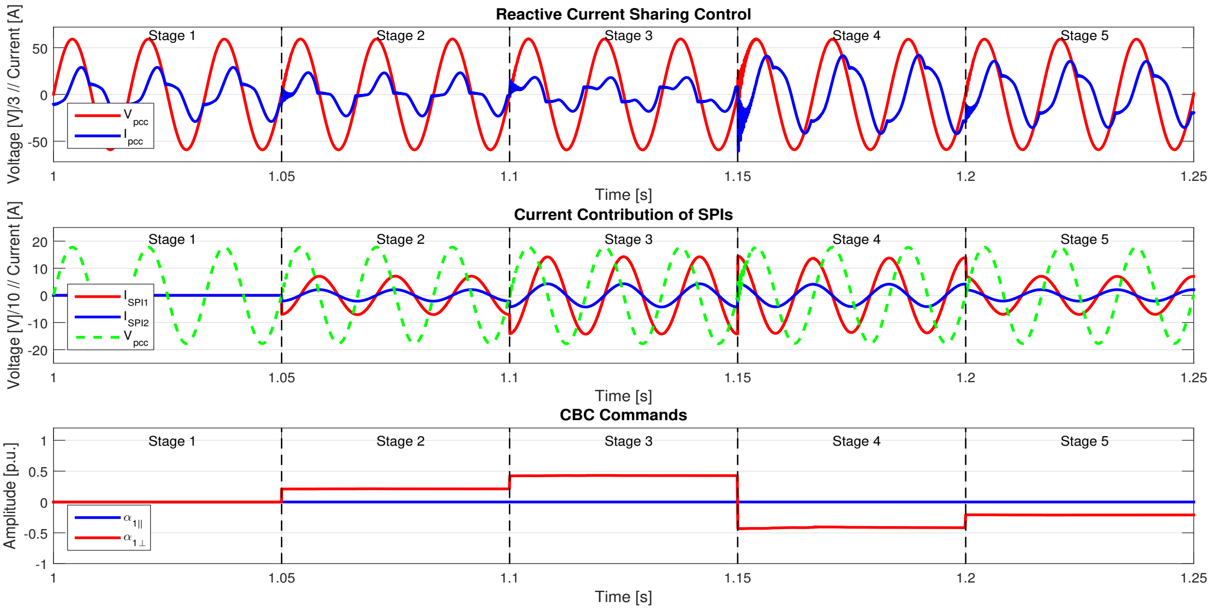


Figure 48 – Reactive current control at the PCC.

the reactive control command $\alpha_{1_\perp}$ rises up, in Stage 2, from 50% to a Stage 3 with 100% of the total reactive current demanded by the load, this respective current is not supplied by the PCC current anymore. Therefore, remaining only the active and other harmonic currents. Besides, one should note the phase shifting between the PCC voltage and the SPI injected currents. After 1.15 seconds, it is evidenced the influence of the positive or negative value of $\alpha_{1_\perp}$, injecting a 100% of the load reactive current in Stage 4 and 50% in Stage 5. As previously mentioned, the scaling coefficients is capable of changing the functionality of the SPIs, providing capacitive or inductive current interventions at the PCC. It is also noticeable how the control command responsible for the fundamental in-phase term ($\alpha_{1_{||}}$) remains null at all stages, as expected.

It is lastly reiterated that, in regard of so far available products and regulatory matters, the CBC's ability just demonstrated for active and reactive control would be sufficient to support real applications of power sharing in distributed electrical systems.

5.3.3 Harmonic Current Sharing

Even though regulations and commercialized SPIs do not present multifunctional capabilities other than active and reactive control, technologies for the employment of additional harmonic control applications are being fast consolidated. The CBC algorithm provides as well efficient means for selectively realized harmonic power sharing in networks with DERs. Through the adjustment of the control commands given by the CBC algorithm, $\alpha_{h_{||}}$ and $\alpha_{h_\perp}$, that can be determined for any set of harmonic orders, harmonic mitigation may be achieved as desired.

A simulation carried out with PSIM, following the same parameters of the active and reactive control cases, is presented in Fig. 49 and shows that flexible harmonic control is possible through the CBC. It is defined that, after 1.05 until 1.1 seconds, the SPIs should be operating injecting 3^{rd} harmonic component, under the commands of $\alpha_{3_{||}}$ and $\alpha_{3_\perp}$. It can be seen that,

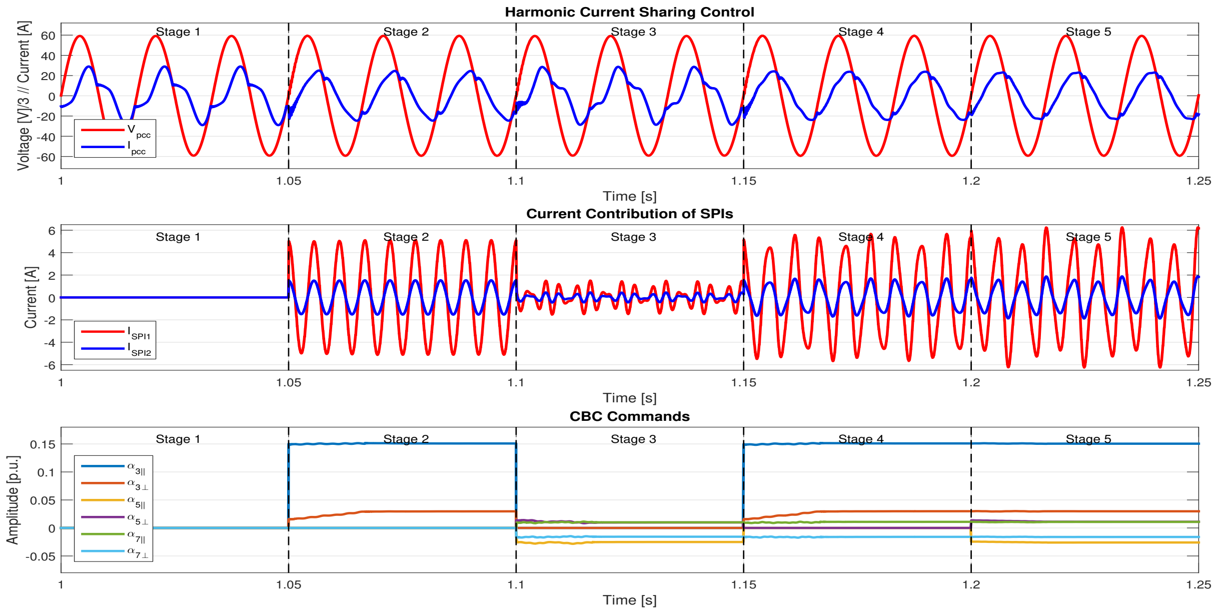


Figure 49 – Harmonic current control at the PCC.

since this component is one of the most relevant lower harmonics, the current at PCC suffers a significant change towards a sinusoidal wave shape, presenting $THD_i = 7.14\%$. From 1.1 to 1.15 seconds, the 5^{th} and 7^{th} harmonic orders are tackled while the 3^{rd} harmonic is disregarded, and as their content is lower than the 3^{rd} frequency, the PCC current shape becomes more distorted than the previous stage, with $THD_i = 28.35\%$

As explained, the CBC is capable of working concomitantly on a set of harmonics, therefore, from 1.15 to 1.2 seconds, its control commands for the 3^{rd} plus the 7^{th} orders are activated, resulting in $THD_i = 6.18\%$. And finally, on the last stage, the 3^{rd}, 5^{th}, and 7^{th} harmonics are injected, obtaining an almost sinusoidal current at the PCC. For this case, the PCC current under operation of the CBC presented a $THD_i = 3.43\%$, which is a significant reduction in comparison to the initial condition of $THD_i = 28.79\%$. Even if this case presented distorted grid voltage, the sinusoidal current synthesis would still be provided, as it will be later demonstrated in a practical simulated example in Section 6.3.

The impact of this harmonic sharing control provided by the CBC can be better understood by analyzing Fig. 50. For each of the broken-down stages mentioned, the respective current harmonic content at the PCC is depicted. One can note that, with respect to the first stage, in which no harmonic intervention occurs, the respective injected harmonic orders are totally, or at least very significantly, reduced at the PCC. The conditions herein discussed prove how flexible the CBC methodology can be, providing selective harmonic control over the PCC, which can be a very useful functionality in power quality enhancement applications.

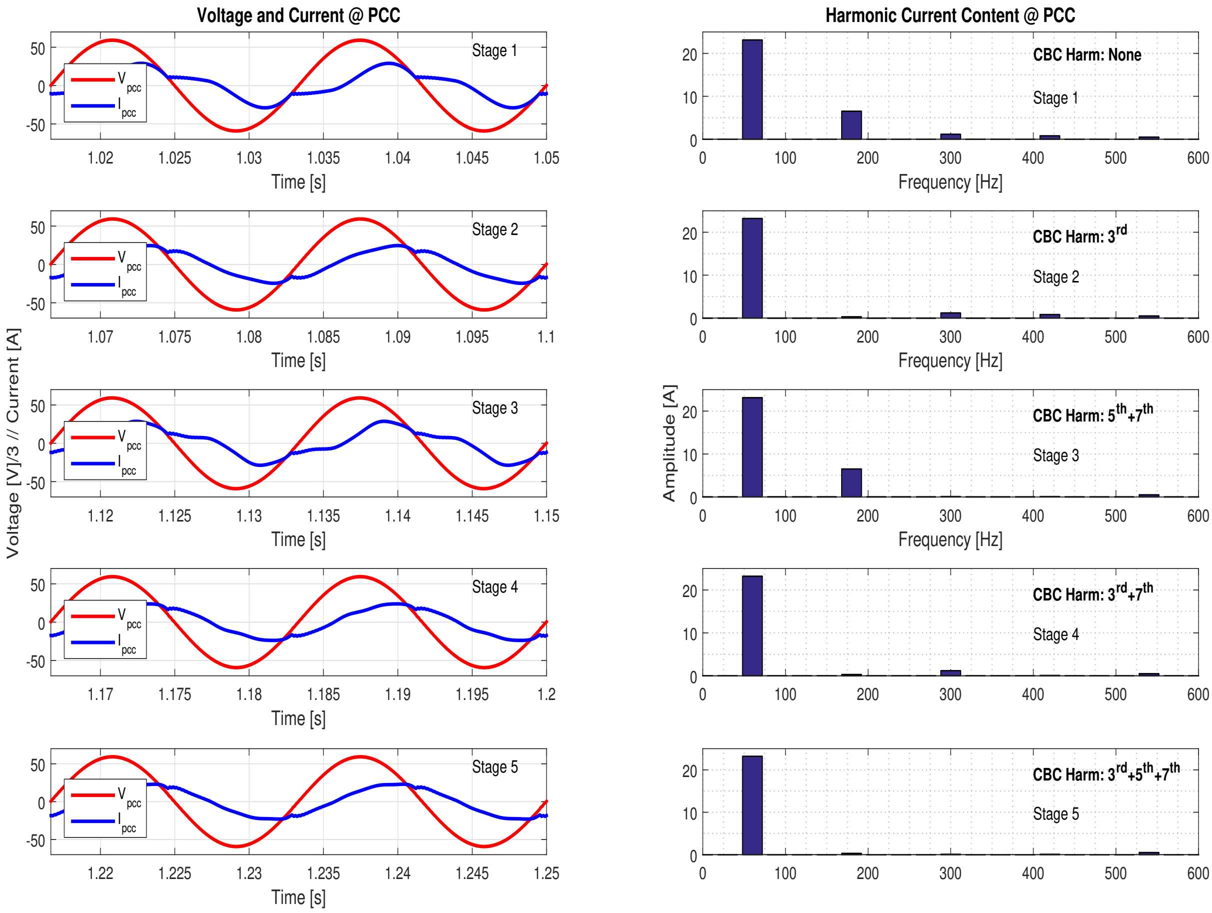


Figure 50 – Improvement of harmonic current content at the PCC with CBC.

6 Simulation of Harmonic Compensation with Distributed SPIs

On the pursuit of attesting the benefits of employing the Current-Based Control on harmonic suppression, by means of distributed multifunctional SPIs, some proposed cases are simulated trying to reproduce major common conditions that could be expected in single-phase low voltage microgrids with DERs. An initial case portraits the CBC operation, providing selective compensation of reactive and harmonic terms, along with injection of active currents, following the power restrictions established by each SPI. After that, simulations intent to show the adequate functioning of the discussed primary and secondary controls under different grid conditions. In a third case, the operation of the system is examined under very non-sinusoidal conditions, e.g. representing practical cases that could occur in microgrids. At last, a final case is presented considering a diversified scenario with distorted grid voltage, load step, different line impedances, and also showing the controllability of the DC link control, with SPIs operating as APFs.

Regardless of the case, the proposed scheme depicted in Fig. 51 serves as reference topology for the simulation circuitry. Since several conditions are intended to be tested during different time intervals, this circuit topology takes into account two main distributed SPIs, SPI_1 and SPI_2, and a third one, SPI_3, is connected in parallel to the load at determined instants of the simulation. The nonlinear load used is the same in Section 3.2 and other past cases.

All the SPIs were designed following the same methodology of the PRes controller described in Chapter 4, considering a three-level PWM modulation and with LC filters for filtering the pulsed voltage output of the inverters. Some of the main features of the system are summarized in Table 4 as well. Yet, the implementation of the SPIs was performed with PSIM,

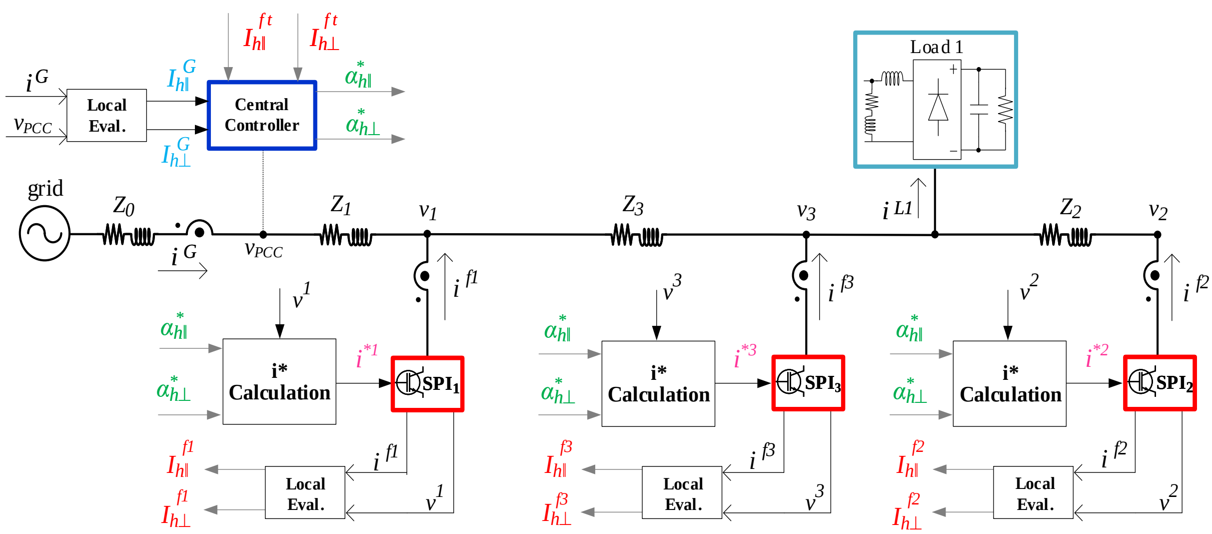


Figure 51 – Schematic of circuit used on simulated cases.

being modeled as VSIs controlled by current and operating as DGs. Fig. 52 shows the circuitry developed with the PRes controllers coded within C language blocks. Note that, since most of the simulated cases consider EGs with capability to process active power, an ideal voltage source was placed in parallel to the DC link capacitor of each SPI to provide means for active current injection. A particular case implemented for the last proposed simulated example is shown in Fig. 52-b, comprising now the SPIs implemented as APFs, in which no active power is processed in its DC link, therefore requiring the outer voltage control loop to be enabled.

All the simulations were carried out with the respective complete schematic shown in Fig. 53. It can be seen that the CBC algorithm has been coded in C language blocks, and there is a central unit, which represents the central controller of the operation, and other EGs in which the α commands are computed and transmitted to the primary level control of full bridge SPIs. Each EG has its SPI, which are implemented by the circuit shown in Fig. 52, having particular LC filter components and PRes controller gains designed for each inverter.

Regarding the simulation environment, a 9.1 PSIM version was used, and a time step of $4.16667e^{-7}$ seconds was adopted on a computer platform with the following specifications. An Intel Core i5-2540M, with 2.50 GHz cache capacity, and RAM memory of 8 GB. Considering such features, for instance, the first simulated case took 8min 56s to complete.

Table 4 – Parameters adopted for simulations with CBC.

Feature	**Specification**
SPI1 Nominal Peak Current (I_{SPI1}^{peak})	$33.30A$
SPI2 Nominal Peak Current (I_{SPI2}^{peak})	$23.31A$
SPI3 Nominal Peak Current (I_{SPI3}^{peak})	$9.99A$
SPI1 LC Filter Inductor (L_{SPI1}^{LC})	$1.47mH$
SPI2 LC Filter Inductor (L_{SPI2}^{LC})	$2.10mH$
SPI3 LC Filter Inductor (L_{SPI3}^{LC})	$4.90mH$
Switching frequency (f_{sw})	$12kHz$
Sampling frequency (f_s)	$24kHz$
Grid nominal voltage (V_g)	$127V$
Grid frequency (f_g)	$60Hz$
Line Impedances† (Z_n)	$0.1 + j0.02\ \Omega$
CC-EGs Transmission Time* (t_{data})	$16.66ms$

†Case 4: $Z_0 = Z_3 = 0.1 + j0.02\ \Omega$ // $Z_1 = 2 \cdot Z_0$ // $Z_2 = 3 \cdot Z_0$

*Case 4: $t_{data} = 50ms$

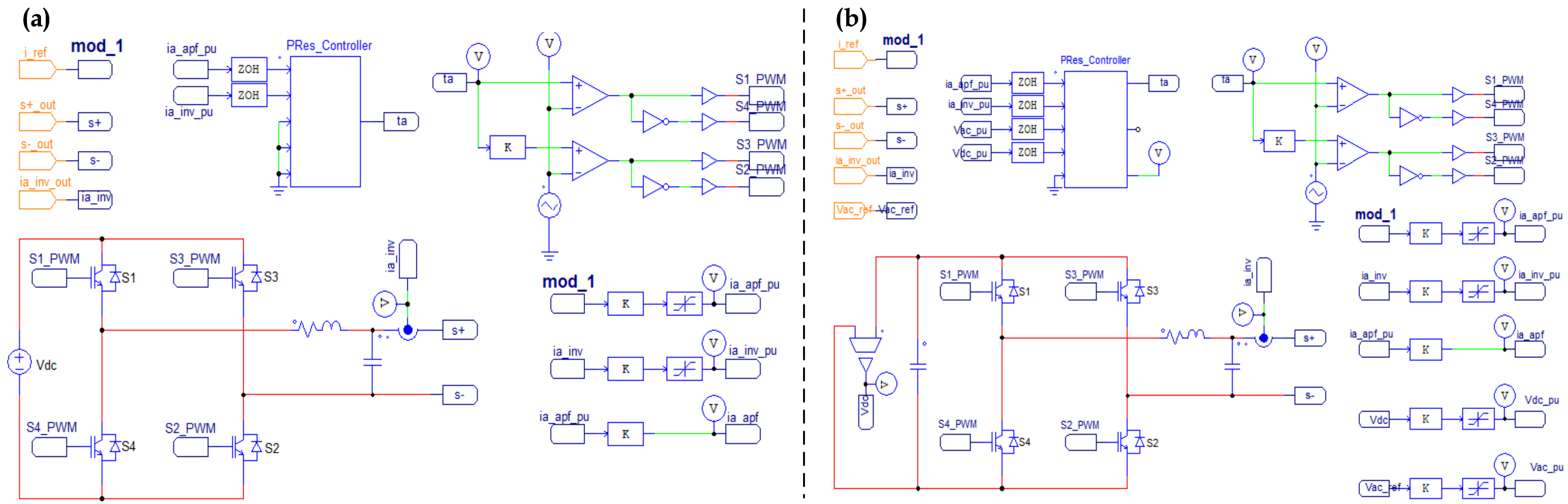


Figure 52 – PSIM circuitry for the SPIs as EGs (a) in Cases 1-3, and APFs (b) in Case 4.

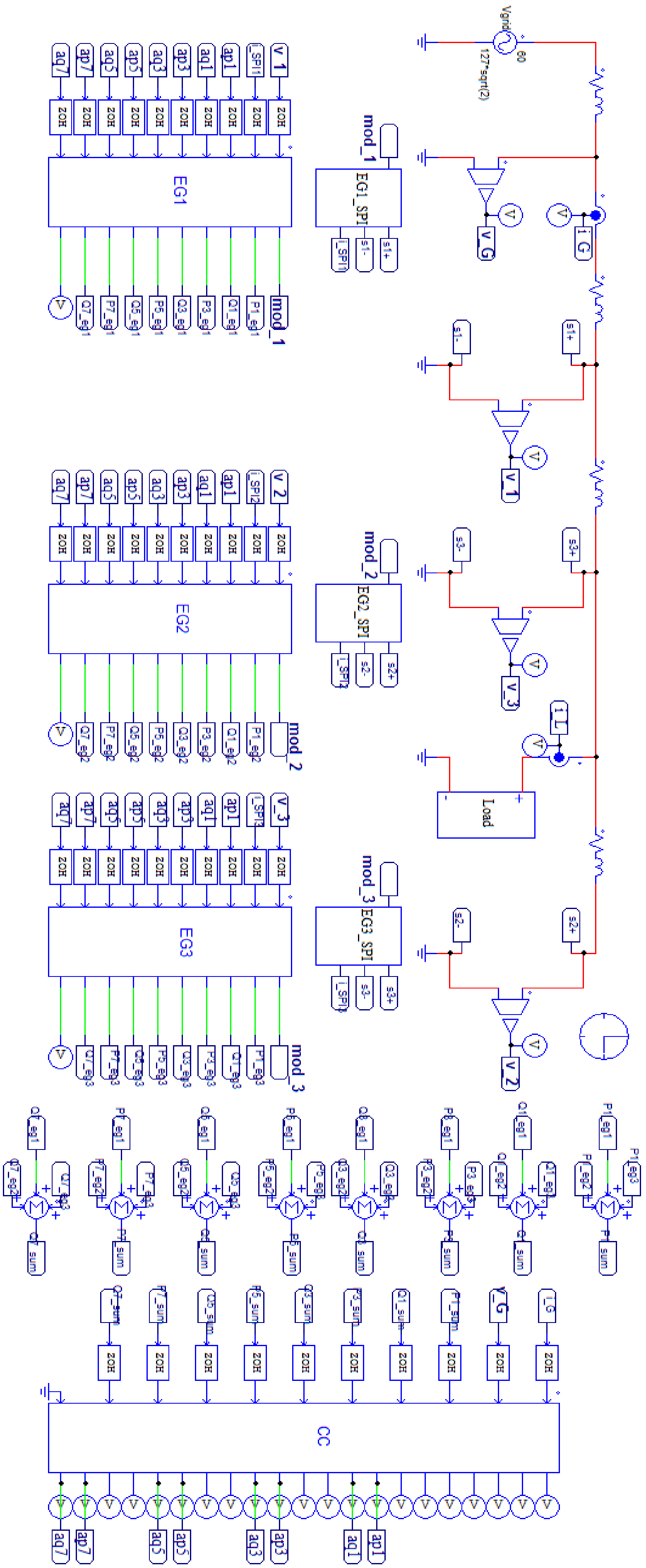


Figure 53 – PSIM circuitry for the simulations with three SPIs and CBC.

6.1 Distributed Selective Harmonic Compensation

To demonstrate the operation of the CBC on current sharing and mitigating harmonics at the PCC, this case study was split into six stages, as shown in Table 5. These stages define the contribution of each SPI in the respective time intervals, allowing selective and multifunctional operation. It is important to mention that, the defined contribution in each of the following stages are basically the control references desired to be handled on the current sharing within the microgrid I_h^{G*}, which come from the tertiary level. In all simulations, the transmission of I_h^{G*} was idealized with no time delay within the secondary layer controller, changing in a specific predefined time. Therefore, the final results of the current sharing by means of the CBC is shown in Fig. 54, along with the generated control references presented in Fig. 55. Stage 1 shows an overview of the current at the PCC without any intervention coming from the SPIs. One can note the nonlinear behavior of the load, even under a grid voltage purely sinusoidal. For the second stage, the SPIs start to operate injecting active and reactive current, remaining only harmonic terms at the PCC.

The particular harmonic compensation starts in Stage 3, in which currents of specific harmonic frequencies are injected driven by the CC and based on the available capability of each SPI. This configuration stands as an analogy for the possible local desired configurations, on which each DER owner may establish for its operation. As a result, injecting active current, giving support to reactive or contributing with selective harmonic compensation occurs under the supervision of a local or higher level regulator within a tertiary control layer.

Table 5 – Operation Parameters for Simulation - Case 1

	Time [s]	**SPI**	**Contribution**
Stage 1	1.000 - 1.033	1	-
		2	-
		3	-
Stage 2	1.033 - 1.100	1	Active+Reactive
		2	Active+Reactive
		3	-
Stage 3	1.100 - 1.167	1	3^{rd} Harm.
		2	3^{rd} Harm.
		3	-
Stage 4	1.167 - 1.234	1	Reactive + 7^{th} Harm.
		2	Reactive + 7^{th} Harm.
		3	Reactive + 7^{th} Harm.
Stage 5	1.234 - 1.301	1	React. + 3^{rd} + 5^{th} + 7^{th} Harm.
		2	React. + 3^{rd} + 5^{th} + 7^{th} Harm.
		3	React. + 3^{rd} + 5^{th} + 7^{th} Harm.
Stage 6	1.301 - 1.367	1	Act. + React. + 3^{rd} + 5^{th} + 7^{th} Harm.
		2	Act. + React. + 3^{rd} + 5^{th} + 7^{th} Harm.
		3	Act. + React. + 3^{rd} + 5^{th} + 7^{th} Harm.

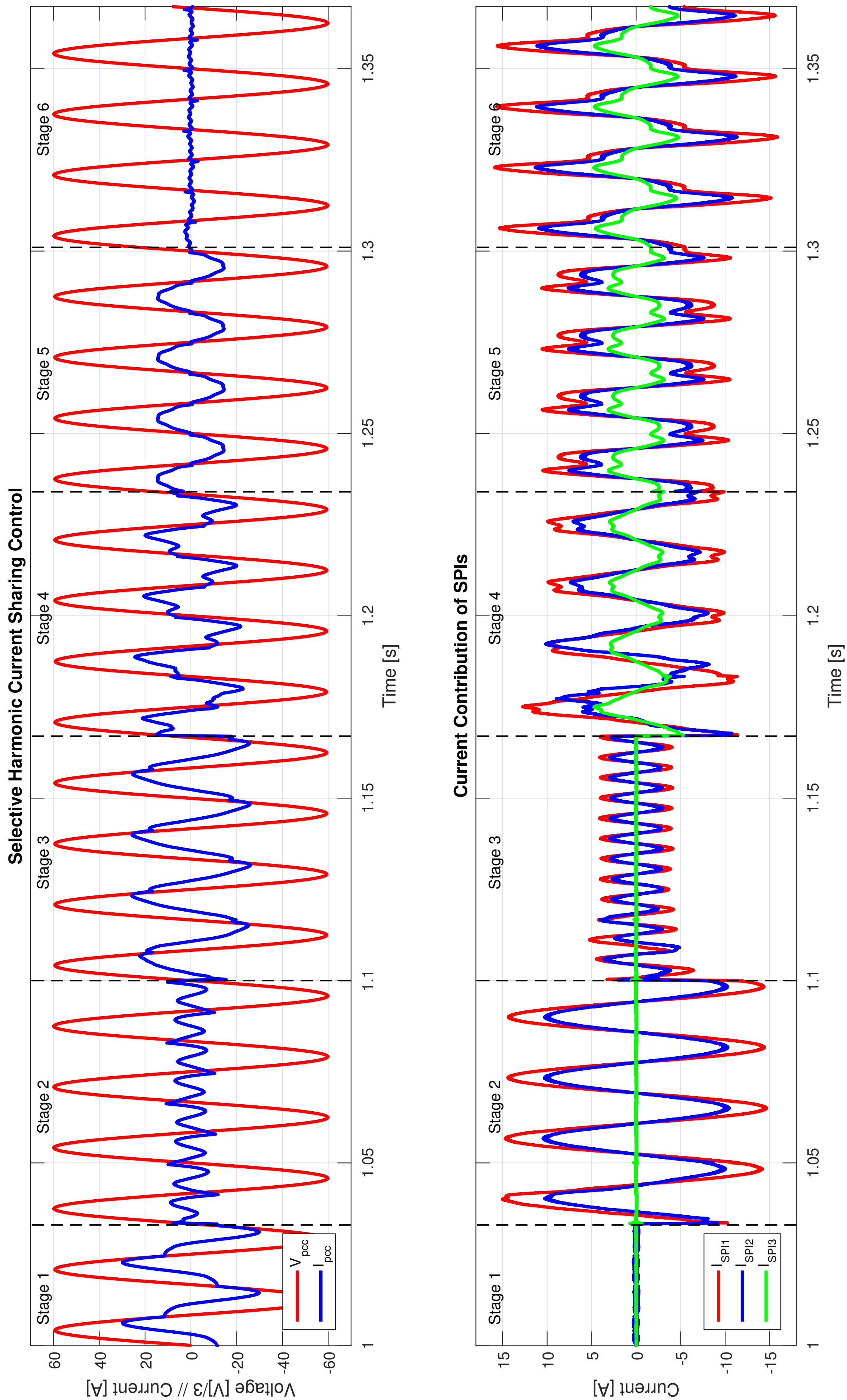


Figure 54 – CBC operation with three distributed SPIs and selective harmonic compensation.

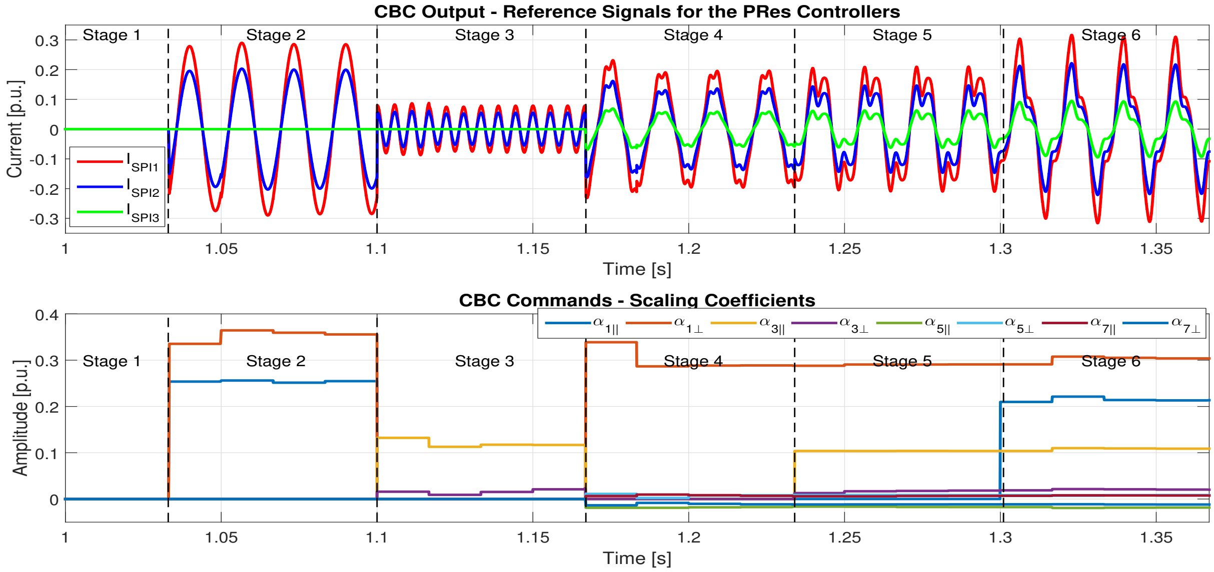


Figure 55 – References from CBC: Control currents of PRes controllers and scaling commands - Case 1.

Knowing that, for this load, the third harmonic was the one with higher influence on the PCC current distortion, it can be noticed how its only compensation reshapes the nonlinear behavior of the PCC current waveform at this stage. Stage 4 shows two SPIs contributing on the mitigation of reactive current (fundamental in quadrature terms), along with 7^{th} harmonic order elements. The following Stage 5 simulates a scenario in which, although the DERs are not able to generate active power (e.g., PV based inverter during night), they operate as active power filters giving support to the grid in matter of non-active currents.

The last stage simulates the condition of limited active power generation, allowing the remaining power rate of the SPIs to be employed on ancillary services, reliving the grid from the burden of supporting the microgrid current demand. It is noticeable how the remaining PCC current presents, practically, no active, reactive, or any of the other harmonic terms selected. Another very important highlight is how each SPI contributes proportionally to their nominal current capacity, following $I_{SPI3}^{peak} < I_{SPI2}^{peak} < I_{SPI1}^{peak}$.

Looking at the harmonic bands of the PCC current demonstrated in Fig. 56, one can note that, for each different simulated stage, the CBC provides significant reduction of the band harmonic content around the target frequency. The CBC effectiveness is proved by looking at the results of stage 6, where significant harmonic mitigation has been shown at the PCC. Some other merit factors are also brought in Table 6, aiming at showing the impact of using the CBC on coordination of distributed SPIs. Such factors were calculated considering the last cycle of the PCC current at each stage, taking into consideration a steady-state condition of the proposed operation.

The THD_i measurements demonstrate that, for the cases (Stage 3 and 5) in which mitigation of the most critical harmonic terms is demand, the grid current is significantly less distorted. Additionally, these values even serve as a quantitative estimation, demonstrating that if standards were imposed, such as the IEEE 519 (IEEE, 2014a) that states a maximum current

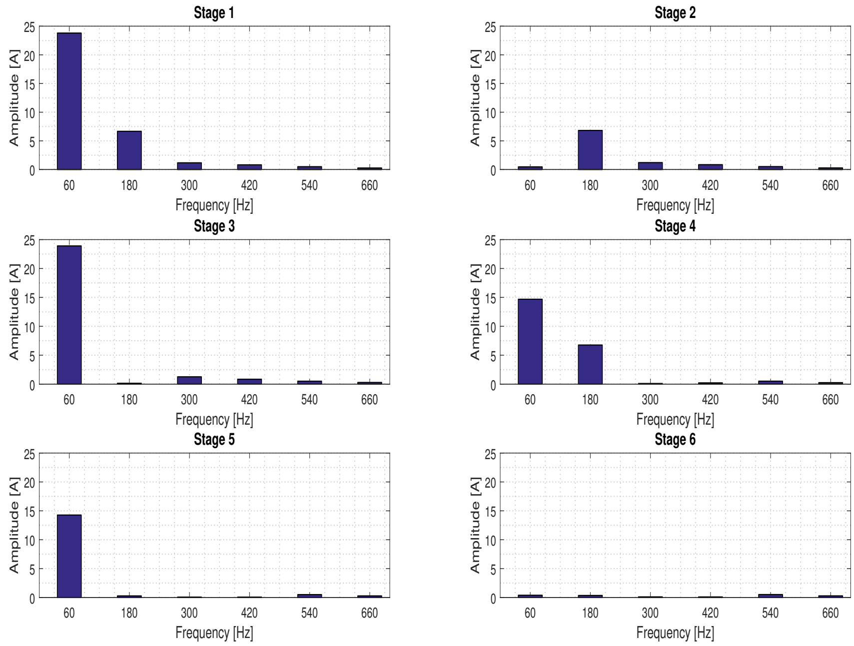


Figure 56 – Harmonic content at PCC with CBC operating with selective harmonic compensation.

Table 6 – Quantitative Analysis for Different Stages with the CBC - Case 1

	Stage 1	**Stage 2**	**Stage 3**	**Stage 4**	**Stage 5**	**Stage 6**
$\mathbf{THD_i}$ **[%]**	28.79	1422.09	6.95	49.25	5.32	187.60
$\boldsymbol{\lambda}$	0.5904	0.04962	0.60779	0.9062	0.99844	0.3104
$\boldsymbol{\lambda_v}$	0.2791	0.9976	0.06991	0.4234	0.0532	0.9187
$\boldsymbol{Z \cdot I^2}$: $\boldsymbol{Z_1}$ [W]	31.12	2.51	29.33	13.44	10.41	0.04
$\boldsymbol{Z \cdot I^2}$: $\boldsymbol{Z_2}$ [W]	0	5.09	0.38	2.36	2.63	4.03
$\boldsymbol{Z \cdot I^2}$: $\boldsymbol{Z_3}$ [W]	31.12	12.89	30.09	17.81	15.56	8.16

total demand distortion (TDD_i) limit of 5%, the system would comply with it. Although the matter of relating THD_i to TDD_i values is not appropriate, it is here used seeing that, due to their mathematical definition, this first factor is always smaller than the second one in steady state conditions (BLOOMING; CARNOVALE, 2006). It is important mentioning that, in Stage 2 and 6, a high value is found for the THD_i since active and/or reactive currents are being injected simultaneously, resulting in negligible current fundamental at the PCC. Some other work (POMILIO *et al.*, 2015) already discussed this matter, therefore, not being further explored herein.

Other two quantities, which are explained in Appendix B, being calculated based on the Conservative Power Theory current decomposition, also present unitary measurements respective to the power factor (λ), and how distorted the PCC current is (λ_v). For instance, it can be seen that, in Stage 2, λ is close to zero, representing a practical null active flow at the PCC in relation to the total power flow. On the contrary, when the SPIs operate as APF, in Stage 5, the power factor is almost unitary, since the reactive and harmonic content are compensated by the distributed systems. Likewise, a high value of λ_v shows that in Stage 2 mainly harmonic terms exist at the PCC, being contrasted by a very low value when the most critic harmonics are compensated in Stage 3 and 5.

A last quantity is presented, with intention of giving a representation about the power flow and losses over the microgrid. By analyzing the dissipated power on each line impedance of the circuit, as shown in Table 6, it can be seen that when no intervention occurs by the SPIs, Z_1 and Z_3 are the ones dissipating most and there is practically no current flowing through Z_2. When some SPIs start to operate, the dissipated energy decreases in Z_1 as the grid provides less current. This also happens when only harmonic terms are shared among the SPIs, however, since such terms present small amplitude in relation to the fundamental in-phase and quadrature, their respective impact is smaller. Finally, by having the inverters almost fully supplying the load, practically no power is dissipated in Z_1.

6.2 Distributed Harmonic Compensation With Grid and Load Variations

Low voltage grids with considerable number of DERs, and particularly microgrids, are weak networks that are very susceptible to grid voltage and load variations, although regulations and standards establish such deviations to be within an operational range. This reality adds complexity to the design of electronic devices and should as well be overcome regarding the operational capabilities of methodologies employed on power quality interventions with distributed inverters. Hence, this section aims at showing how the CBC behaves under certain grid conditions and load variations.

For the simulation of this proposed case, three main operation conditions are evaluated, being them: the disturbances of an instant grid voltage sag, later a swell, and also a condition with heavy load step. The same current ratings of Table 5 are considered here for the three SPIs, which are, at all the simulated periods, pursing the total offering of load demand for active, reactive and harmonic currents. This means that there is an expectation of alleviating the grid from the burden of providing any current terms to the loads. It is underlined that the used load is modeled as a constant impedance. This is relevant since there will occur voltage level changes over the simulation. Moreover, the adopted variation of the system parameters is given as shown in Table 7.

By analyzing the results depicted in Figs. 57 and 58, many considerations can be discussed. As in Stage 6 of Case 1, the simulation starts with Stage 1 operating with nominal voltage and load conditions, injecting active, reactive and the 3^{rd}, 5^{th} and 7^{th} harmonic terms. In the sequence, a voltage swell of 25% is set for the grid in Stage 2, causing a rise on the voltage level, reaching a peak of $224.50V$. Simply by Ohm's law, since the voltage level increased, the current demanded by the load will rise proportionally, therefore, demanding the CBC to adjust its gains for higher current interventions from the connected SPIs. This behavior is seen in the simulated case, and it is also shown that it occurs under a stable transition.

Table 7 – Operation Parameters for Simulation - Case 2

	Time [s]	System Condition	SPI	Contribution
Stage 1	1.000 - 1.033	Nominal Condition	1 2 3	Act. + React. + 3^{rd} + 5^{th} + 7^{th} Act. + React. + 3^{rd} + 5^{th} + 7^{th} Act. + React. + 3^{rd} + 5^{th} + 7^{th}
Stage 2	1.033 - 1.100	25% Voltage Swell	1 2 3	Act. + React. + 3^{rd} + 5^{th} + 7^{th} Act. + React. + 3^{rd} + 5^{th} + 7^{th} Act. + React. + 3^{rd} + 5^{th} + 7^{th}
Stage 3	1.100 - 1.167	Rest. Nominal Cond.	1 2 3	Act. + React. + 3^{rd} + 5^{th} + 7^{th} Act. + React. + 3^{rd} + 5^{th} + 7^{th} Act. + React. + 3^{rd} + 5^{th} + 7^{th}
Stage 4	1.167 - 1.234	25% Voltage Sag	1 2 3	Act. + React. + 3^{rd} + 5^{th} + 7^{th} Act. + React. + 3^{rd} + 5^{th} + 7^{th} Act. + React. + 3^{rd} + 5^{th} + 7^{th}
Stage 5	1.234 - 1.301	Rest. Nominal Cond. + 100 % Load Step	1 2 3	Act. + React. + 3^{rd} + 5^{th} + 7^{th} Act. + React. + 3^{rd} + 5^{th} + 7^{th} -
Stage 6	1.301 - 1.367	Rest. Nominal Cond. + 100 % Load Step	1 2 3	Act. + React. + 3^{rd} + 5^{th} + 7^{th} Act. + React. + 3^{rd} + 5^{th} + 7^{th} Act. + React. + 3^{rd} + 5^{th} + 7^{th}

Moreover, with restoration of the voltage level to nominal conditions, which is done in Stage 3, the SPIs return to the nominal operation as earlier in an initial state. Another power quality issue evaluated is the voltage sag simulated in Stage 4. The voltage level drops 25% of its nominal value, reaching $134.70V$, and again, the CBC is able to adjust its coefficients demanding lower active, reactive and harmonic current injection from the SPIs.

In Stage 5, coming back from another restoration to nominal voltage condition, the system then suffers an abrupt load step, with a 100% higher current demand in comparison to the initial state of the circuit. Once again, this is an often fact in low-voltage networks, where load keeps changing dynamically throughout the day. It can be noted how the inverters are able to double their current injection capability, reaching their maximum power ratings, and converging to a stable steady state operation as the CBC provides adjusted setpoints for the right intervention. Within the last period, the third SPI is also reconnected to the grid, helping the two others on the burden of supplying all the active, reactive and harmonic currents.

Presenting an overview of the harmonic bands of the PCC current for the main stages simulated, as in Fig. 59, it is noted how the CBC has been practically not affected by the different grid and load conditions. The harmonic content for the 3^{rd}, 5^{th} and 7^{th} orders remained significantly low when the sag and swell occurred. An interesting case appears in Stage 5, since the grid peak current doubled with the load step, the maximum capabilities of the two SPIs were reached, resulting in limited harmonic mitigation, increasing the THD_i. However, when the third SPI was reconnected in Stage 6, such harmonics at the PCC current decreased again.

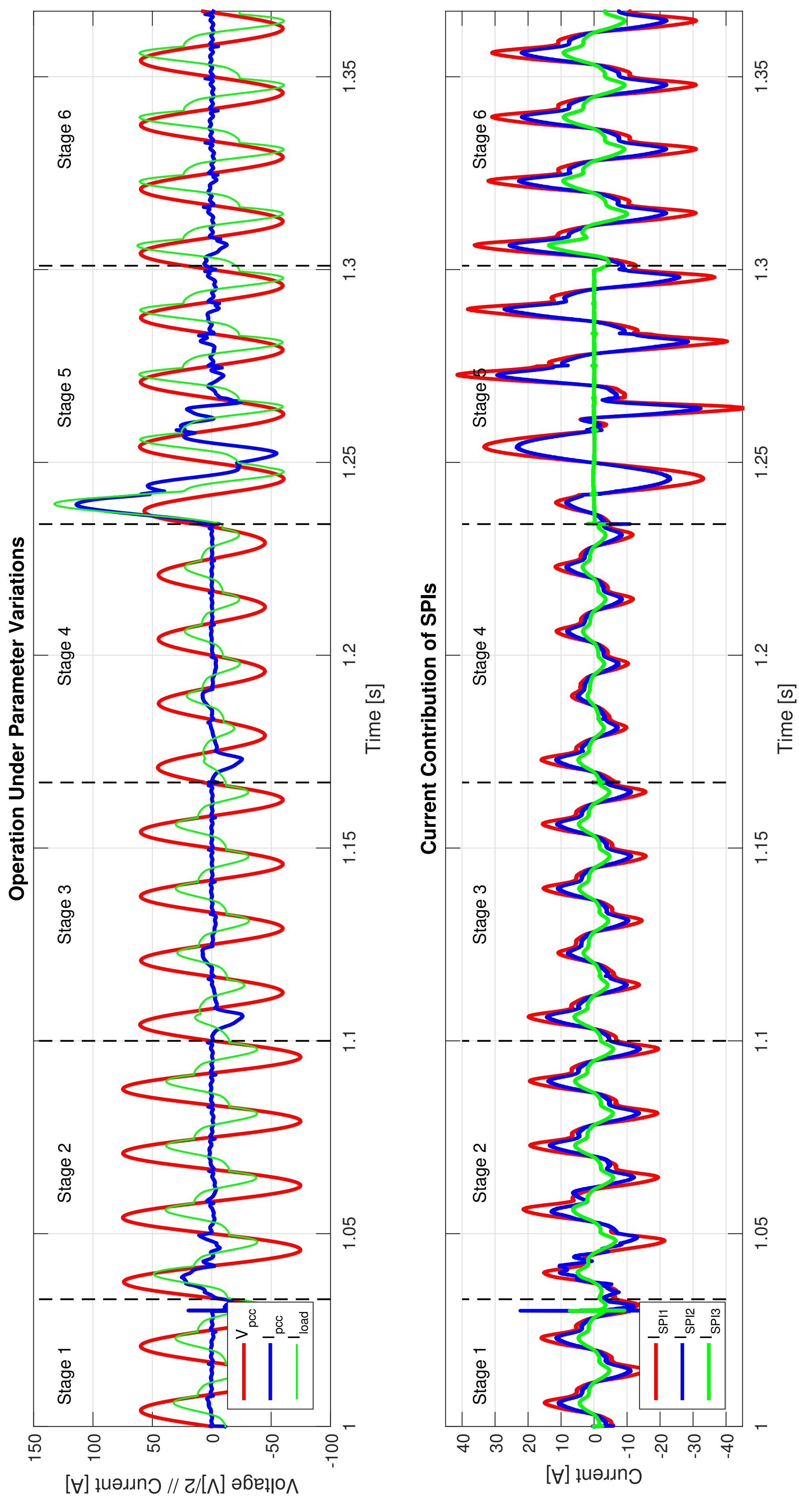


Figure 57 – CBC operation with system parameters variations.

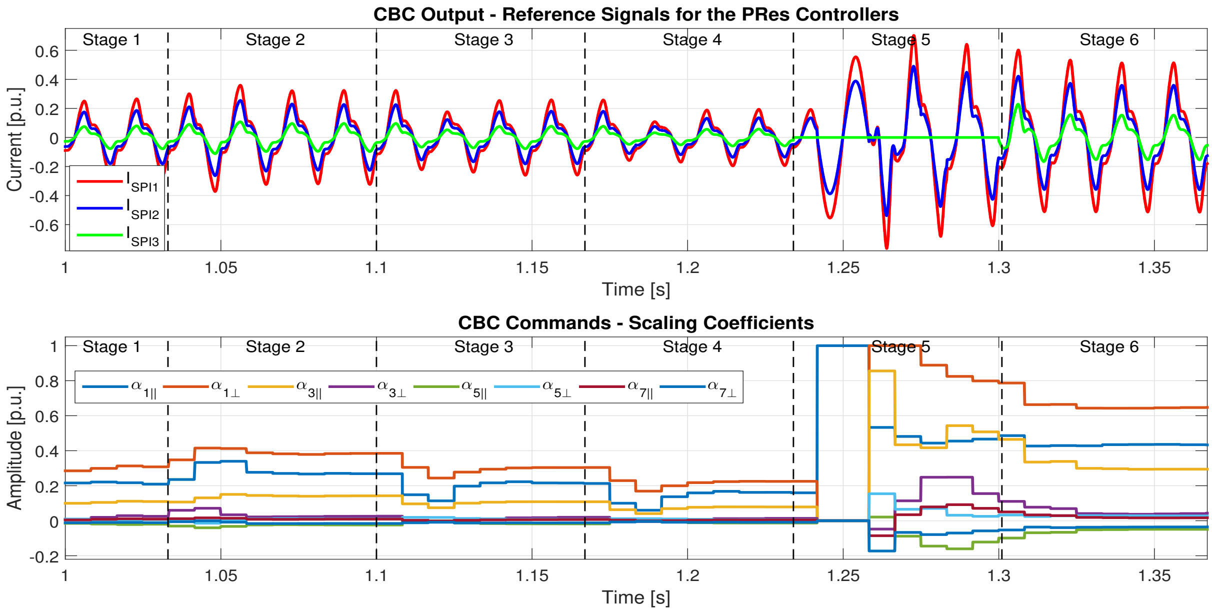


Figure 58 – References from CBC: Control currents of PRes controllers and scaling commands - Case 2.

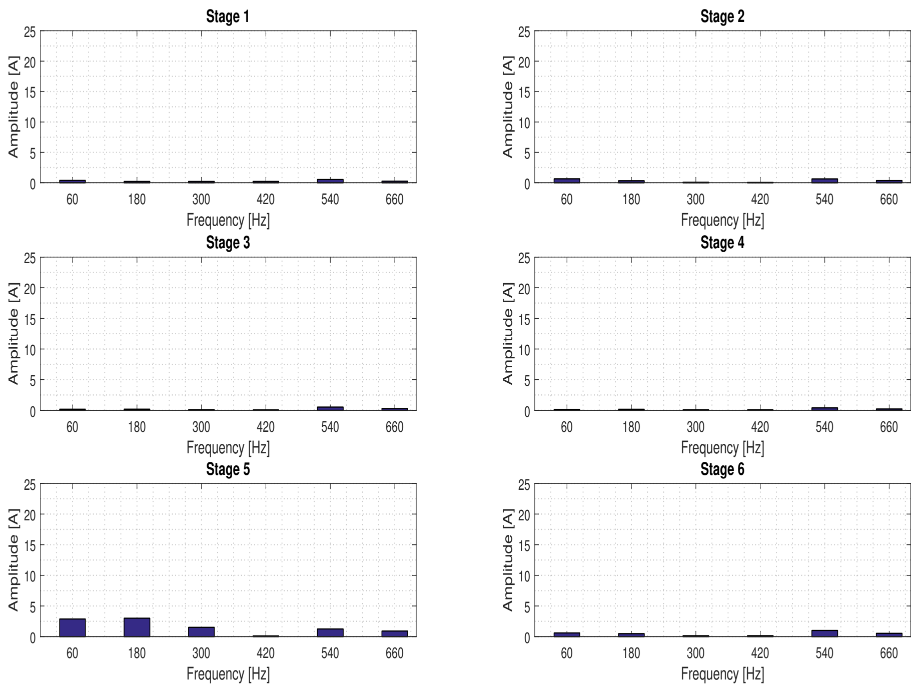


Figure 59 – Harmonic content at PCC with CBC operating under parameters variations.

Table 8 – Quantitative Analysis for Different Stages with the CBC - Case 2

	Stage 1	**Stage 2**	**Stage 3**	**Stage 4**	**Stage 5**	**Stage 6**
THD$_i$ [%]	187.60	191.02	353.13	346.40	151.65	239.84
$\boldsymbol{\lambda}$	0.3104	0.0756	0.0458	0.0556	0.1586	0.2192
$\boldsymbol{\lambda_v}$	0.9187	0.9191	0.9704	1.0	1.0	0.9370
$\boldsymbol{Z \cdot I^2}$: $\boldsymbol{Z_1}$ [W]	0.04	0.07	0.03	0.02	1.29	0.13
$\boldsymbol{Z \cdot I^2}$: $\boldsymbol{Z_2}$ [W]	4.03	6.26	4.07	2.29	23.13	15.88
$\boldsymbol{Z \cdot I^2}$: $\boldsymbol{Z_3}$ [W]	8.16	12.93	8.18	4.58	42.53	32.56

In respect to the other merit factors presented in Table 8, by having the SPIs injecting active, reactive and harmonic terms in all stages, almost a null current is seen at the PCC. Therefore, as previously discussed, although it results in high THD_i values, such quantity should not be considered as a depreciation in power quality due to the practically zero amplitude current flowing in this node. The CPT's power and distortion factors show a steady behavior in all stages where interventions occur, certifying that no active current was flowing at the PCC, as λ is close to zero. In spite of having high λ_v values, they can be understood to present no significant impact since practically no harmonic content with high amplitude is found at the grid current. The power dissipated on line impedances also emphasizes that when SPIs are injecting all the main current terms, null or very small energy losses occur at Z_1.

This simulation shows that the CBC is robust to be employed in weak networks, where dynamic control is fundamental for the maintainability of stable operation conditions for DERs. Considering the same processing configuration, this simulation took 8min 34s to be performed in PSIM.

6.3 Distributed Harmonic Compensation With Heavy Voltage Distortion

In spite of several positive features related to the presence of DERs in microgrids and low-voltage networks, drawbacks such as voltage distortion in nodes away from a distribution feeder may be encountered (BRANDAO *et al.*, 2016). Under such cases, any control methodology employed on the management of related power devices should be robust enough to provide reliable operation. The proposal of the CBC also aims at standing unaffected on grids with high level of non-sinusoidal conditions. Therefore, now a simulation focus on showing how this feature is presented by this secondary control methodology, overcoming heavy voltage distortion and allowing current sharing among DERs.

For this particular attempt to show harmonic suppression at the PCC, it is chosen as grid condition the same $127V_{rms}$ pure sinusoidal voltage source used so far, in addition to another 180Hz source (3rd harmonic), presenting peak value equal to $0.25 \cdot 127V_{rms}$ and with $-30°$ phase deviation. Thus, resulting in a grid voltage condition as given in eq. (6.1).

$$v_g(t) = 127 \cdot \sqrt{2} \cdot \cos(2\pi 60t) + 31.75 \cdot \sqrt{2} \cdot \sin(3 \cdot (2\pi 60t - 30°)) \tag{6.1}$$

Regarding the simulated stages, they have been divided as shown in Table 9. Their respective results are then presented in Figs. 60 and 61. At Stage 1, one can note how the previous load condition, which already drained a non-sinusoidal current, now is even more distorted due to the voltage grid additional third harmonic content. From Stage 2, it is seen how the CBC controls the current sharing of active and reactive terms with three SPIs, impacting in only remaining low amplitude harmonic currents at the PCC. Once again, this is done proportionally considering the maximum power ratings of each distributed inverter.

Table 9 – Operation Parameters for Simulation - Case 3

	Time [s]	**SPI**	**Contribution**
Stage 1	1.00 - 1.033	1 2 3	- - -
Stage 2	1.033 - 1.100	1 2 3	Active + Reactive Active + Reactive Active + Reactive
Stage 3	1.100 - 1.167	1 2 3	3^{rd} + 5^{th} + 7^{th} Harm. 3^{rd} + 5^{th} + 7^{th} Harm. 3^{rd} + 5^{th} + 7^{th} Harm.
Stage 4	1.167 - 1.234	1 2 3	React. + 3^{rd} + 5^{th} + 7^{th} Harm. React. + 3^{rd} + 5^{th} + 7^{th} Harm. React. + 3^{rd} + 5^{th} + 7^{th} Harm.
Stage 5	1.234 - 1.301	1 2 3	Act. + React. + 3^{rd} + 5^{th} + 7^{th} Harm. Act. + React. + 3^{rd} + 5^{th} + 7^{th} Harm. Act. + React. + 3^{rd} + 5^{th} + 7^{th} Harm.
Stage 6	1.301 - 1.367	1 2 3	Act. + React. + 3^{rd} + 5^{th} + 7^{th} Harm. + Act. Control Act. + React. + 3^{rd} + 5^{th} + 7^{th} Harm. + Act. Control Act. + React. + 3^{rd} + 5^{th} + 7^{th} Harm. + Act. Control

Stage 3 shows a selective operation aiming to tackle the third, fifth and seventh order frequency current terms at the PCC. It noticeable that, even under a harsh grid distortion, no significant harmonic content seem to be present at the grid current. Then, Stage 4 shows the compensation of non-active terms. One can note how the CBC conducted the power quality intervention, letting the PCC current with no phase deviation in relation to the fundamental term of grid voltage, and also with a waveform lightly reminding a sinusoidal shape.

In Stage 5, the setpoints of the SPIs are adjusted conquering, practically, full harmonic compensation for all terms (3^{rd}, 5^{th}, 7^{th}) and support to the active and reactive currents demanded by the load. This operation, as expected, impacts in practically zero current at the PCC. Lastly, the reference of a sinusoidal active term with amplitude of 40A is given by the CBC control commands in Stage 6, allowing a practically sinusoidal in-phase current, with the respective desired amplitude, to be available at the PCC. Since the CBC operates processing periodic quantities and transmitting commands on periodic transmission windows, some processing delays may occur as evidenced in the PCC current in Stage 6. Note that, as example of such processing delay, in Fig. 61 (Stage 6) can be seen that even though the reference from the tertiary level was changed in 1.301 seconds, the scaling coefficients were only adjusted and sent to the SPIs when the one cycle transmission period was reached. The distributed SPIs had their control references completely adjusted after a few iterations and started to respond adequately, smoothly transiting through the abrupt change in the control references.

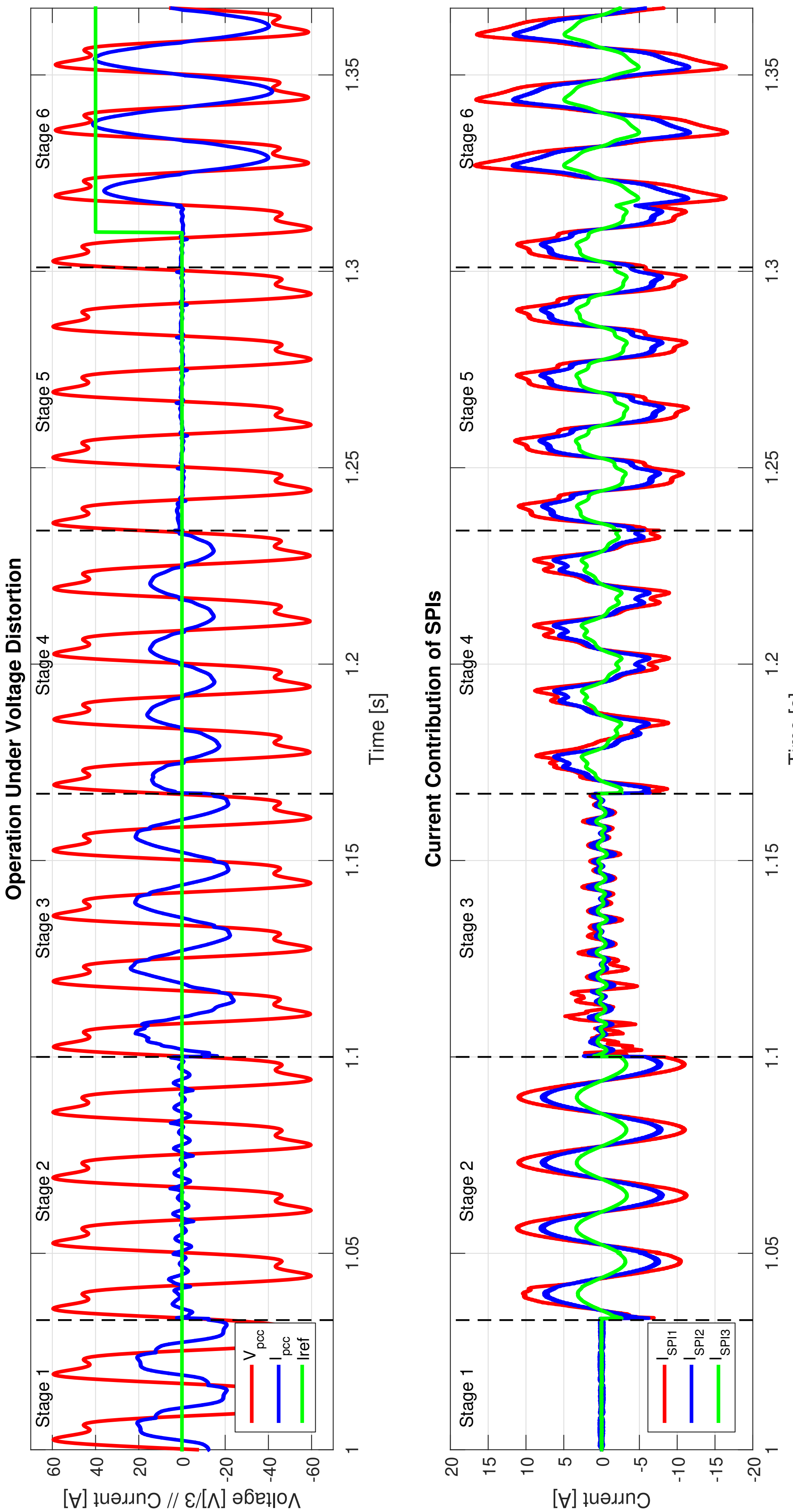


Figure 60 – CBC operation under heavy grid voltage distortion.

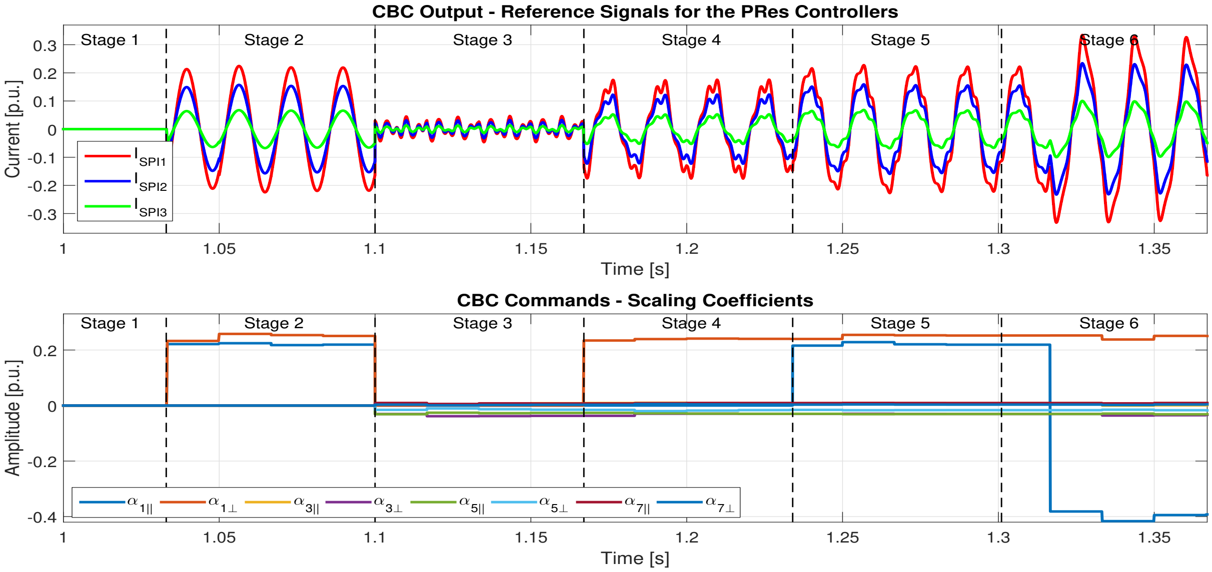


Figure 61 – References from CBC: Control currents of PRes controllers and scaling commands - Case 3.

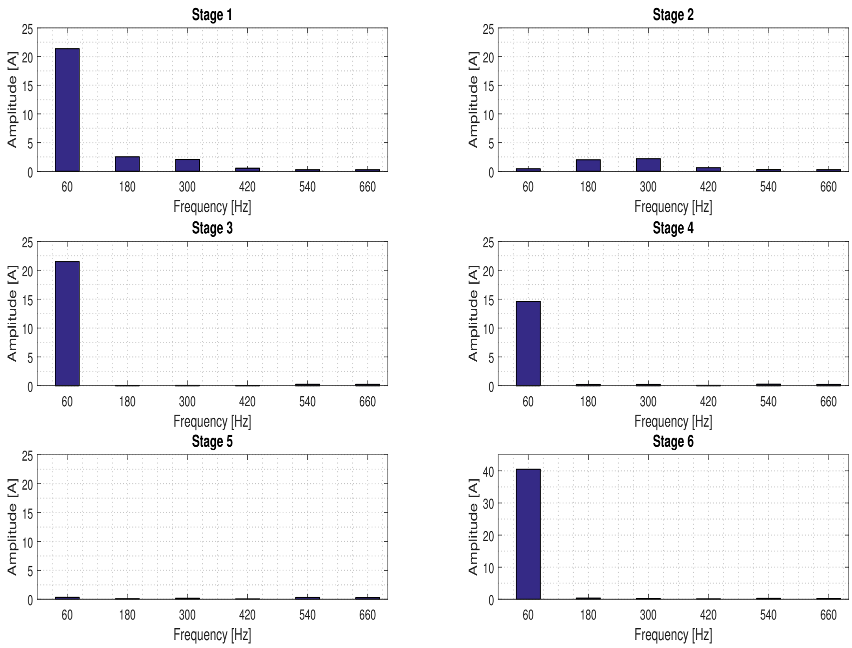


Figure 62 – Harmonic content at PCC with CBC operating under heavy voltage distortion.

Furthermore, by paying attention to the band estimation of the harmonic content at the PCC in the different mentioned stages, as depicted in Fig. 62, power quality enhancement is proved. It is interesting to note, for instance looking at Stage 2, that the harmonic content increased in relation to the other previous cases discussed. However, when demanded in other stages, the CBC provided adequate harmonic mitigation. Yet, as shown in Stage 6, by imposing active power control along with compensation duties, the harmonic bands overall remained low as in Stage 5, presenting practically only fundamental in-phase component with the expected peak value.

In comparison to the initial stage, the data presented in Table 10 shows how the grid current had its THD_i significantly improved in Stages 3 and 4, and also when mutual compen-

Table 10 – Quantitative Analysis for Different Stages with the CBC - Case 3

	Stage 1	Stage 2	Stage 3	Stage 4	Stage 5	Stage 6
THD$_i$ [%]	15.55	680.26	2.51	4.13	163.10	1.39
$\boldsymbol{\lambda}$	0.6448	-0.0502	0.6776	0.9696	0.3572	0.9698
$\boldsymbol{\lambda_v}$	0.2901	0.9961	0.17863	0.2450	0.8769	0.2453
$\boldsymbol{Z \cdot I^2}$: $\boldsymbol{Z_1}$ [W]	23.85	0.48	24.89	10.86	0.02	83.07
$\boldsymbol{Z \cdot I^2}$: $\boldsymbol{Z_2}$ [W]	0	3.01	0.06	1.66	3.07	57.89
$\boldsymbol{Z \cdot I^2}$: $\boldsymbol{Z_3}$ [W]	23.83	6.58	23.64	13.98	6.26	40.72

sation and active control was enabled in Stage 6. This result proves that, even if the bus voltage exceeds standard specifications, such as 8% THD_v delimited by the IEEE 519 regulation, the CBC could still provide low distortion current at the PCC, within harmonic limits. The λ values also reinforces that operations could be achieved with high power factor. Power losses at the PCC show that, depending on the terms injected by the distributed SPIs, the current flowing through Z_1 is either reduced when compensation occurs or increased when more grid active power is drained.

6.4 Distributed Harmonic Compensation Considering Diverse Scenarios

Microgrids are very complex and dynamic systems, presenting diversified topologies, line impedance characteristics between nodes, and intermittent power demands. The consequence of such conditions is, therefore, the requirement of robustness from the therein employed operational methodologies. Aiming at evaluating the functional capabilities of the CBC, it is here presented a final case in which a more diversified scenario is considered for the microgrid. Under the same topology of Fig. 51, the following changes are implemented.

First, different line impedances are adopted, trying to bring a more complex challenge to the distributed control approach of the CBC, as presented in Table 4. This is an interesting condition, since DGs are usually not symmetrically placed in a network (always located having the same distance from each other), resulting in contributions that interact with different line impedances over the microgrid. Once again a distorted grid voltage condition is selected, having the same features of Case 3. Yet, the same 100% load step presented in Case 2 is simulated, trying to demonstrate how the system behaves under disturbances on this new scenario.

The CBC usability is not limited to the implementation on DGs, but also extends to power conditioners distributed over the network, such as active power filters. Knowing that, this case focuses on having the three SPIs used so far, now implemented as APFs. DGs in general relay on MPPT adjustment when just a small amount, or none, of power generation is available at the inverter's DC side (AZEVEDO *et al.*, 2009; KADRI *et al.*, 2011). Different from them, active filters are totally dependent on the adequate operation of their respective outer voltage loop controllers, not exceeding design criteria. Otherwise, the entire distributed coordination of the system could be deteriorated, with interventions not fully responding to control references. The DC link voltage outputs of the three SPIs are then presented in the results.

Communication links, as aforementioned, are critical elements in centralized methodologies, since transmission delays, packet losses and other issues impact in system stability. Thus, this case shows the operation of the CBC with a lower transmission frequency than the one used so far. A longer transmission time of $50ms$ is adopted for the data to follow between the CC and EGs. The simulated results are presented in Fig. 63, following the operational condition in Table 11.

In Stage 1 the SPIs stay on stand by mode, not injecting any currents, resulting in a grid current with the same initial features as shown in Case 3. Power quality intervention then starts in Stage 2, with compensation of the in-phase and quadrature current terms of the most significant harmonic orders (3^{rd}, 5^{th}, and 7^{th}). Although PCC voltage and current are phase-shifted due to reactive circulation, a significant reduction is attained in relation to harmonics, decreasing the THD_i in more than 10%, as also emphasized on the harmonic bands of the grid current presented in Fig. 64. The DC link voltage remained stable with very small ripple values, and no significant amplification in oscillations of the DC bus occurred due to the harmonic compensation.

In Stage 3, distributed reactive compensation is conducted along with the harmonic suppression, resulting in an in-phase PCC current with low distortion, since practically only the fundamental active term is not supplied by the APFs. Considering that the reactive term injected

Table 11 – Operation Parameters for Simulation - Case 4

	Time [s]	**System Condition**	**SPI**	**Contribution**
Stage 1	1.000 - 1.033	Nominal Condition (Dist. Voltage Grid)	1 2 3	- - -
Stage 2	1.033 - 1.100	Nominal Condition (Dist. Voltage Grid)	1 2 3	3^{rd} + 5^{th} + 7^{th} 3^{rd} + 5^{th} + 7^{th} 3^{rd} + 5^{th} + 7^{th}
Stage 3	1.100 - 1.167	Nominal Condition (Dist. Voltage Grid)	1 2 3	React. + 3^{rd} + 5^{th} + 7^{th} React. + 3^{rd} + 5^{th} + 7^{th} React. + 3^{rd} + 5^{th} + 7^{th}
Stage 4	1.167 - 1.234	Nominal Condition (Dist. Voltage Grid) 100 % Load Step	1 2 3	React. + 3^{rd} + 5^{th} + 7^{th} React. + 3^{rd} + 5^{th} + 7^{th} React. + 3^{rd} + 5^{th} + 7^{th}
Stage 5	1.234 - 1.301	Nominal Condition (Dist. Voltage Grid) 100 % Load Step	1 2 3	React. + 3^{rd} + 5^{th} + 7^{th} React. + 3^{rd} + 5^{th} + 7^{th} React. + 3^{rd} + 5^{th} + 7^{th}
Stage 6	1.301 - 1.450	Nominal Condition (Dist. Voltage Grid) 100 % Load Step	1 2 3	React. + 3^{rd} + 5^{th} + 7^{th} React. + 3^{rd} + 5^{th} + 7^{th} React. + 3^{rd} + 5^{th} + 7^{th}

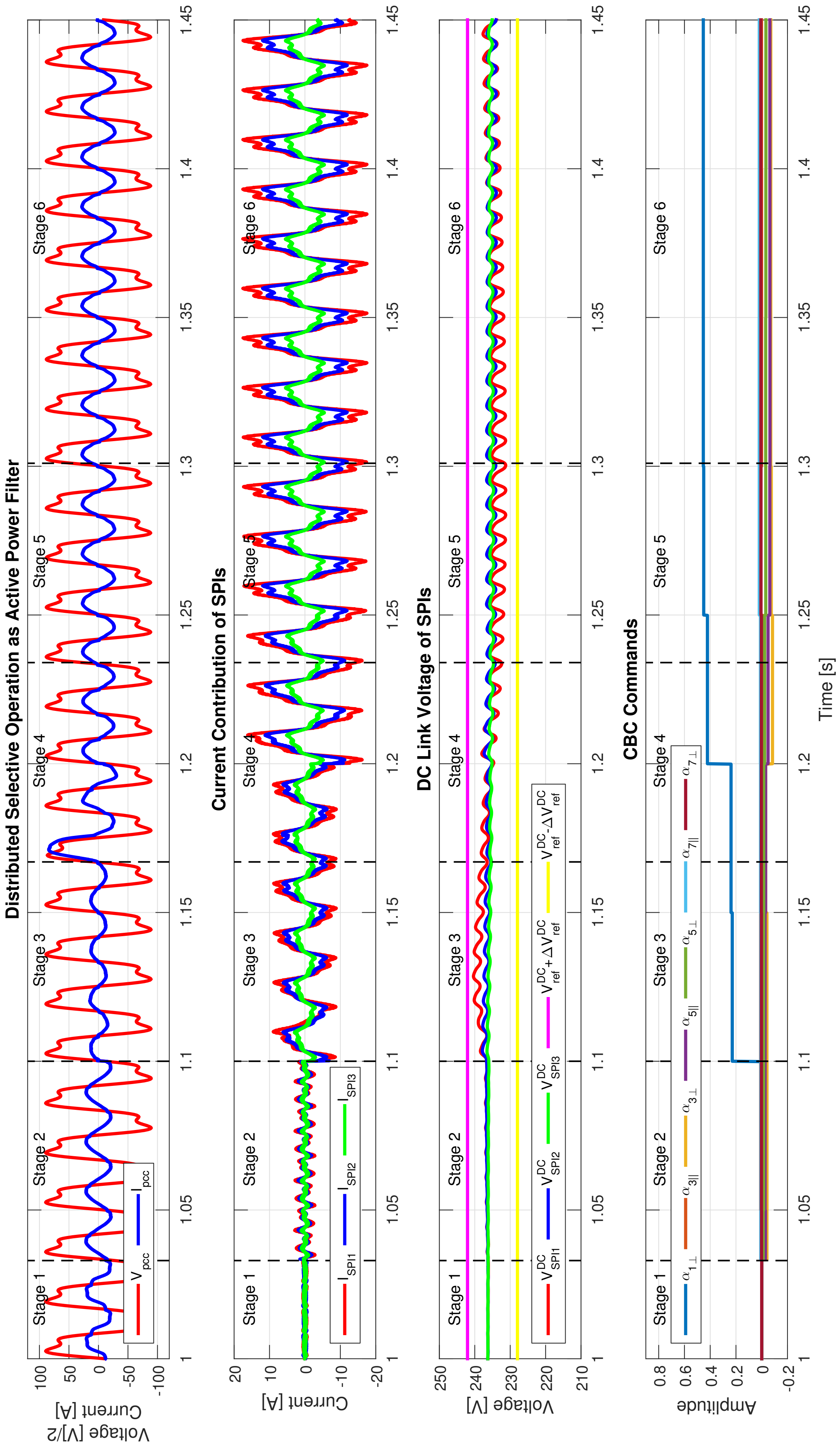


Figure 63 – CBC operation considering scenario changes.

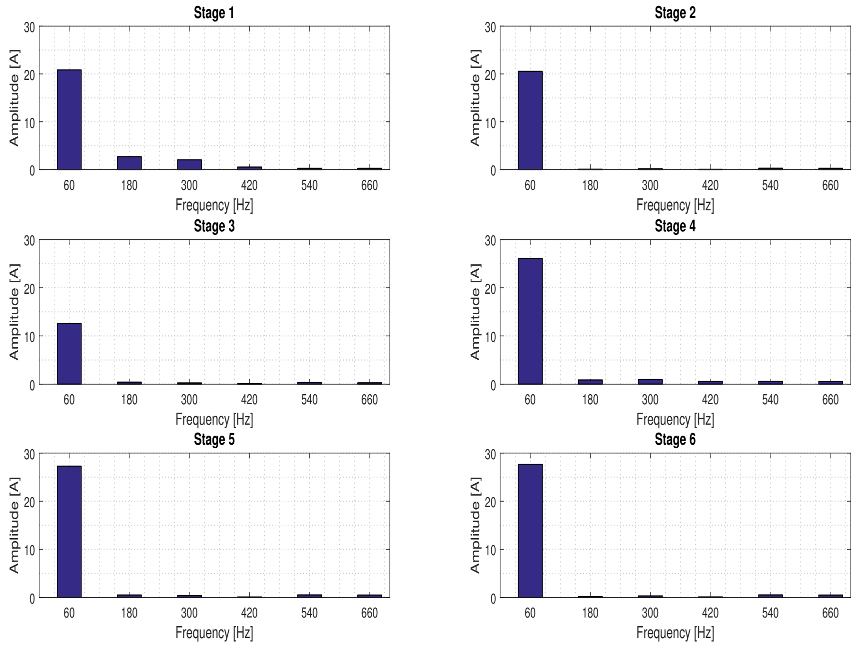


Figure 64 – Harmonic content with CBC operating

presents a more considerable amplitude, being around $10A$ higher in relation to the total peak values of the harmonic terms previously tackled, the DC link voltage suffers a more significant disturbance.

As can be noted in Fig. 63, the higher is the current injected by the respective SPI, the more significant is this voltage deviation. However, even though voltage overshoot occurs, the outer loop controllers are able to adequately respond, conducting the systems back to not variable DC link voltages. Yet, the responses still comply with the positive $(V_{ref}^{DC} + \Delta_{ref}^{DC})$ and negative $(V_{ref}^{DC} - \Delta_{ref}^{DC})$ limits of the designed voltage ripple. Another important consideration related to this matter is that, the currents injected by the SPIs slightly, or not all, deviate of their references, not impacting on the desired sharing of currents and respective intervention at the PCC.

Stage 4 brings the 100% load step, which makes the current demand to be double than the initial state. The APFs smoothly transit over this new demand, while the CBC adjusts their current references to the new peak values of the reactive and harmonic terms. As a consequence of the higher current demand, the THD_i naturally rises in relation to the previous stage, although not excessively exceeding regulatory limits, as seen in Table 12.

Stages 5 and 6 are then presented with intention of showing that, as time goes by, the DC link voltage controllers are still operating on the achievement of a steady state condition, and CBC simultaneously keeps on adjusting the control coefficients of the SPIs until final convergence is attained. It is noticeable how about $50ms$ (approximately 3 fundamental voltage cycles), the α coefficients are readjusted and the THD_i is reduced. Within these stages, it is clear that, the slower the transmission time between CC and EGs is, the slower the system will respond to disturbances and reach a steady state condition. As aforementioned, the related

Table 12 – Quantitative Analysis for Different Stages with the CBC - Case 4

	Stage 1	**Stage 2**	**Stage 3**	**Stage 4**	**Stage 5**	**Stage 6**
THD$_i$ [%]	15.55	3.02	5.31	6.73	4.40	3.94
$\boldsymbol{\lambda}$	0.6444	0.6664	0.9793	0.9679	0.9722	0.9691
$\boldsymbol{\lambda_v}$	0.2977	0.1773	0.2003	0.2437	0.2343	0.2461
$\boldsymbol{Z \cdot I^2}$: $\boldsymbol{Z_1}$ [W]	22.76	21.55	7.81	35.28	38.39	38.75
$\boldsymbol{Z \cdot I^2}$: $\boldsymbol{Z_2}$ [W]	0	0.07	1.58	5.13	5.84	5.91
$\boldsymbol{Z \cdot I^2}$: $\boldsymbol{Z_3}$ [W]	23.54	22.79	13.35	52.37	51.67	51.64

stability conditions of this matter are still to be evaluated, not being further discussed here.

The power losses over the microgrid prove that, by having the SPIs operating as APFs, active power can only by provided by the main, making Z_1 to always be different from zero. Besides, when the active control functionality is activated on the CBC, more active power is present on the main bus, resulting in more dissipation of energy. Having different and higher impedance values for Z_1, Z_2 and Z_3 also impacts on the rise of such losses.

7 Experimental Validation of Distributed Harmonic Compensation

7.1 Hardware Description and Setup Implementation

So far, many comments related to the Current-Based Control algorithm highlighted its capability to coordinate distributed SPIs in a microgrid. Nevertheless, further discussions based on some preliminary experimental work are presented in this section aiming at validating and providing a more plausible way of ensuring the real feasibility of such methodology.

The first stage of any experimental study is related to the assembly of a prototype that retrieves the environmental challenges of the real application, which in this case is a low-voltage single-phase microgrid. Within the facilities of the *Group of Automation and Integrated Systems* (GASI) at UNESP/Sorocaba, a power conditioner panel was employed as main structure for the microgrid prototype. This equipment comprises of three individual single-phase inverters in full-bridge topology, with SKM 75GB128D IGBT modules and SKHI 23/12 gate drivers, and also one three-phase four-leg inverter. LEM LV25-p and LA55-p sensors are available on the panel for, respectively, voltage and current measurements. Some electronic circuits are also present for sensor data acquisition and signal conditioning, along with power connectors and overcurrent protection equipments for the implementation of the electrical nodes of the network. The main grid is represented by a phase-neutral connection with a real network from the local utility. Some pictures of the entire prototype may be seen in Appendix C.

To support controls, one digital signal processor (DSP) module from *Texas Instrument*©, named Experimenter Kit, along with a C2000 Delfino TMS320F28335 floating-point processor controlCARD (TI, 2016) was acquired. This is a 32-bit processor with clock capability of 150MHz, respectively 256KB and 68KB flash and RAM memories, 32-bit timers and a 12-bit analog-to-digital converter (ADC) with 16 channels. A picture of this control set is shown in Fig. 65.

Due to the availability of protection elements and limitation of resources, a few adaptations had to be made in regard to the nonlinear load and microgrid's circuit topology used in

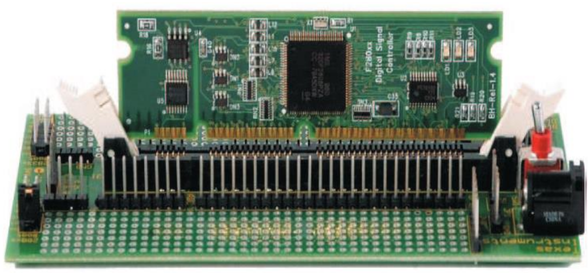


Figure 65 – DSP kit with TMS320F28335 controlCARD. Adapted from (TI, 2011).

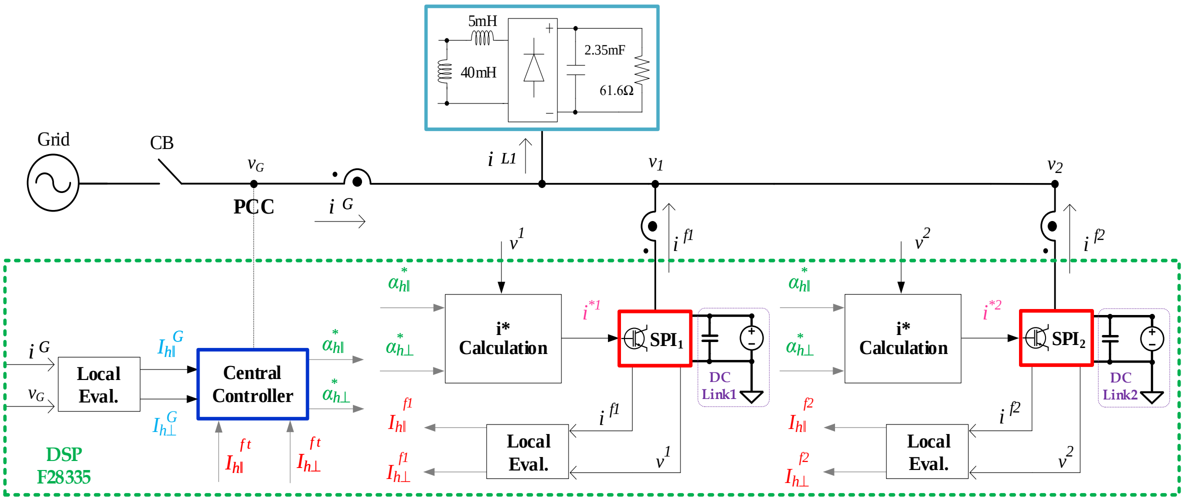


Figure 66 – Circuit assembled for experimental evaluation of the CBC.

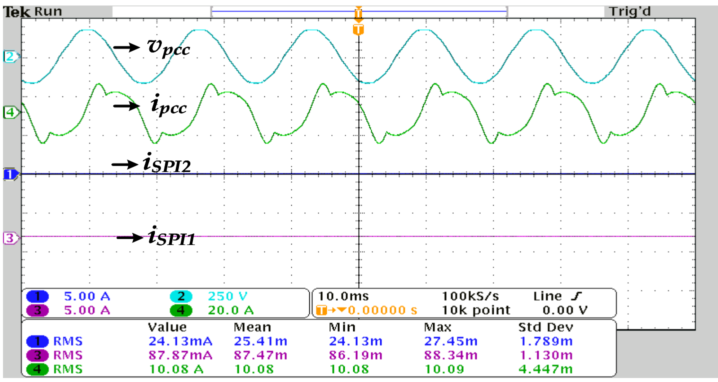


Figure 67 – Load current and grid voltage at the PCC with SPIs disabled.

simulations. The assembled microgrid used in the experimental tests is depicted in Fig. 66. First, it can be noted that the nonlinear load was slightly changed, with $R = 61.6\Omega$ on the DC side of the rectifier, to attain lower current drained, and consequently respect the limits of current fuses and circuit breakers (CB) installed. The current waveform drained by the load can be seen in Fig. 67, considering a grid with sinusoidal voltage and SPIs disabled. It presents current peak value of approximately $16A$ and rms value of $10.1A$, with apparent power $A_{load} = 1.36kVA$, power factor $PF = 0.36$ and $THD_i = 25.10\%$. As can be seen in Fig. 68, with help of a *DPO3PWR Power Analysis Module* used on a *DPO3014 Tektronix Oscilloscope*, the harmonic content of the load current shows a fundamental term with rms value of $I_1^{load} = 9.72A$, $I_3^{load} = 2.22A$ for the 3^{rd} harmonic, $I_5^{load} = 896mA$ and $I_7^{load} = 366mA$ for the 5^{th} and 7^{th} terms respectively. Other harmonic content analyzed herein follow the same approach.

For the sake of simplification, line impedances were disregarded, and only two SPIs were connected to the microgrid. In addition, since active current injection into the grid was intended to be tested as well, individual DC link voltage sources were connected in parallel to the capacitors of each SPI, allowing stable values of $V_{DC} = 235V$. Only L filters were designed for the inverters, being them based on iron core inductors.

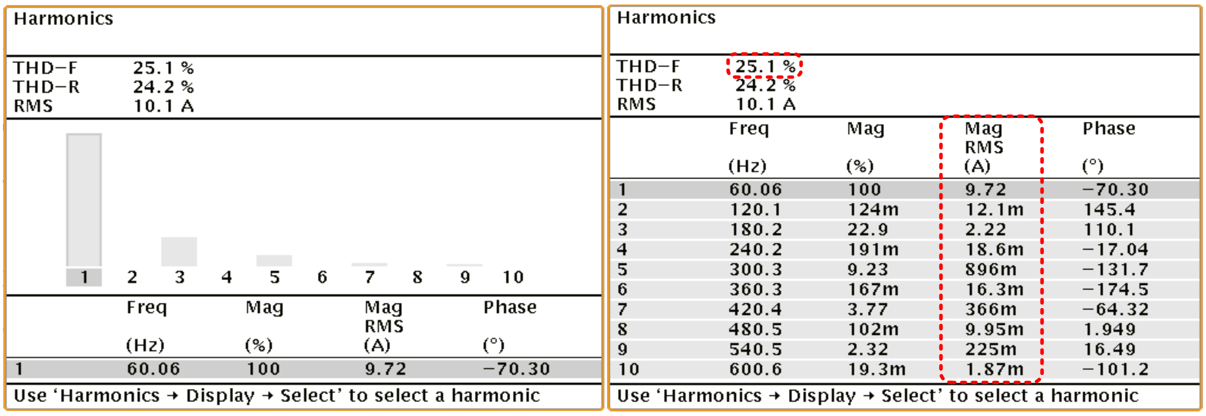


Figure 68 – Harmonic content analysis of load current at the PCC with SPIs disabled.

Concerning control implementation, PRes controllers were devised following the same methodology discussed in Chapter 4. Their respective gains are presented in Table 13, along with other features adopted for the SPIs. Note that, since processing capabilities are limited by the DSP, a single-update mode was chosen, resulting in $f_s = f_{sw}$, allowing less computational effort for further insertion of the CBC algorithm. A very important comment to highlight is that, since only one DSP was responsible for the initialization of the microgrid, the PRes current controllers of the two SPIs, and also the processing of the CBC algorithm (with activities for two local and one central controller), matters related to communications are neglected on the following results. Also, to reduce computational effort, the PRes controllers were tuned to only damp the fundamental, 3^{rd}, 5^{th}, and 7^{th} harmonic orders.

It is reinforced that, although communication matters were neglected by using only one DSP for the implementation of the entire prototype, the data transmission between CC and EGs occurs periodically, as done in the previous simulations of Chapter 6. In a more realistic case, having independent controllers (in different processors) for each EG communicating with the CC, under the condition of having all units synchronized with the CC, would likely bring the similar experimental results to the ones following presented. Nonetheless, mismatch in synchronization on the secondary controller at the CC, related to the receiving/sending of data from/to EGs, would likely cause sluggish accommodation times. Yet, it may even lead to improper operation of the CBC algorithm due to the lack of information about the status of the distributed units, as in any other classic centralized microgrid with networked control (SHAFIEE *et al.*, 2014; FAN *et al.*, 2017). Note that mismatch of frequency synchronization, for EGs to send and receive data packets, is not the same issue as the aforementioned loss of packets or delays in transmission times (SHAFIEE *et al.*, 2014). These other two later issues, as mentioned earlier in Chapter 5, may impact on the CBC operation in very specific conditions which need to be further evaluated.

Table 13 – Parameters adopted for experimental implementation of the distributed operation of SPIs.

Feature	**Specification**
SPI1 Nominal Peak Current (I_{SPI1}^{peak})	$10A$
SPI2 Nominal Peak Current (I_{SPI2}^{peak})	$6A$
SPI1 LC Filter Inductor (L_{SPI1}^{LC})	$2.5mH$
SPI2 LC Filter Inductor (L_{SPI2}^{LC})	$2.5mH$
DC Link Voltage (V_{DC})	$235V$
Switching frequency (f_{sw})	$12kHz$
Sampling frequency (f_s)	$12kHz$
Grid nominal voltage (V_g)	$127V$
Grid frequency (f_g)	$60Hz$
CC-EGs Transmission Time (t_{data})	$16.66ms$
PRes Controller Proportional Gain (K_{P_i})	1.60
PRes Controller Integrator Gain (K_{Ih})	2666.56

7.2 Experimental Results

7.2.1 Injection of Active and Reactive Terms

For the first experiment, it is presented a case in which the two SPIs are supposed to share the burden of active and reactive current terms demanded by the load, relieving the grid from supplying such components. In Fig. 69 this operation was tested, and it is shown the SPI currents, along with the voltage and current at the PCC of the microgrid.

By designing the SPIs considering different current peak capabilities, following that $I_{SPI1}^{peak} > I_{SPI2}^{peak}$, the proportional coordination provided by the CBC algorithm can be easily confirmed on the experimental result. The rms current values follow the desired proportion, resulting in a ratio of 0.574, which is close to the ideal case of $I_{SPI2}^{peak}/I_{SPI1}^{peak} = 0.6$. It is also

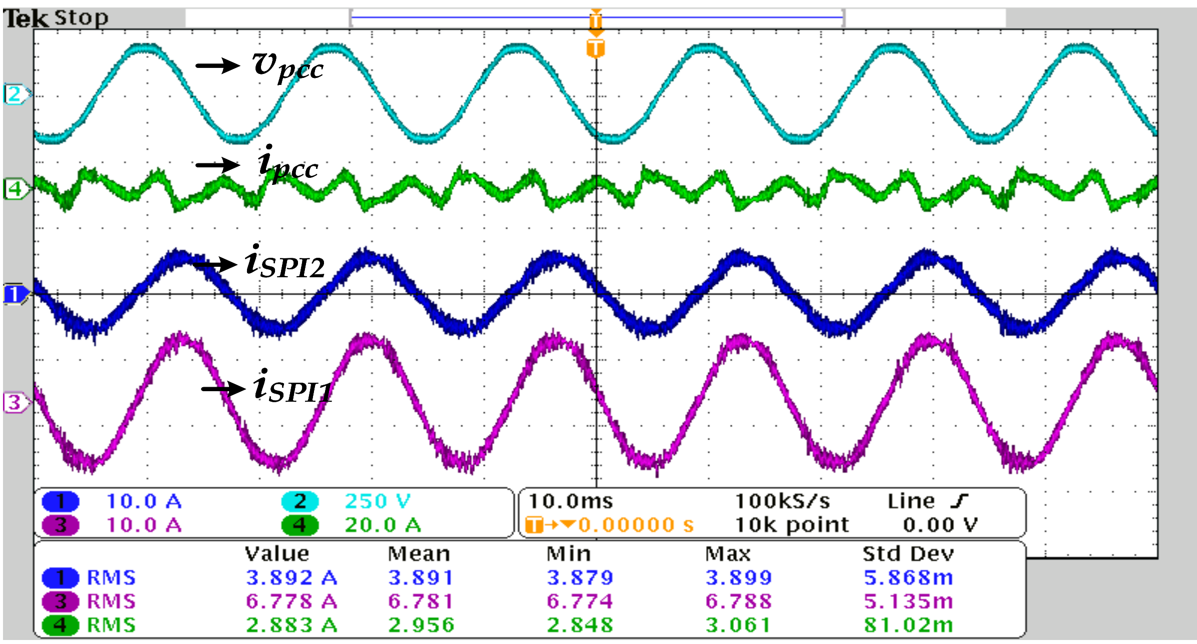


Figure 69 – SPIs cooperatively operating with the CBC injecting active and reactive terms.

noticeable that both SPI currents are in-phase with each other, being phase-shifted in relation to the grid voltage. Since reactive currents are being injected along with the active parcel, this is indeed the expected result. Furthermore, it is seen that the peak values of the currents for each SPI are respecting their maximum designed limits, reaching about $9.58A$ and $5.51A$ respectively for SPI1 and SPI2. As result of having the active and reactive terms shared by the converters, practically only harmonic content is found on the grid current.

As seen in Fig. 70-a, the resultant current at the PCC presented a THD_i of 239%, which is a tangible value considering that mostly harmonic terms are presented, impacting in very high THD values, as occurred in some earlier discussed simulated cases. Analyzing the harmonic bands of the resulting PCC current, using Fig. 68 as reference, it is inferred that the active and reactive quantities were significantly shared by the SPIs, almost fully supplying the load demand for these respective terms, decreasing from a rms value of $9.71A$ to $1.04A$. From Fig. 70-b and -c, injecting fundamental components, the SPI1 current showed THD_i of 3.52%, and the SPI2 of 4.24%. Note that the 3^{rd} and 5^{th} harmonic terms in the PCC current remained practically unchanged by having SPIs only injecting active and reactive terms. Although not being able to supply 100% of the load fundamental terms, as seen by the remaining $1.04A$ PCC rms current, this case gives an overview of the real feasibility of the CBC algorithm.

Lastly, some comments must be reinforced aiming at justifying the obtainment of such results. Since this experimental setup is still under development, only L filters were used so far, which directly impact on having unfiltered high frequency harmonic content on the synthesized currents, and consequentially, on the grid current and voltage as well. For instance, while analyzing experimental results, at all instants a $24kHz$ noise with significant amplitude was present on the frequency spectrum of the grid, SPI1 and SPI2 currents. It most likely occurs due to the inverter switching method that, even though each IGBT switches at $f_{sw} = 12kHz$, the three-level PWM modulation generates components at $2 \cdot f_{sw} = 24kHz$. This is expected but undesired current behavior, not being appropriately filtered, is even worsened by the available iron core of the inductors. It has also been seen that, the smaller the peak value of the synthesized current is, the worse the result is. By just using the LC filters and toroidal or ferrite core inductors, this issue might be diminished and the quality of the results should be increased.

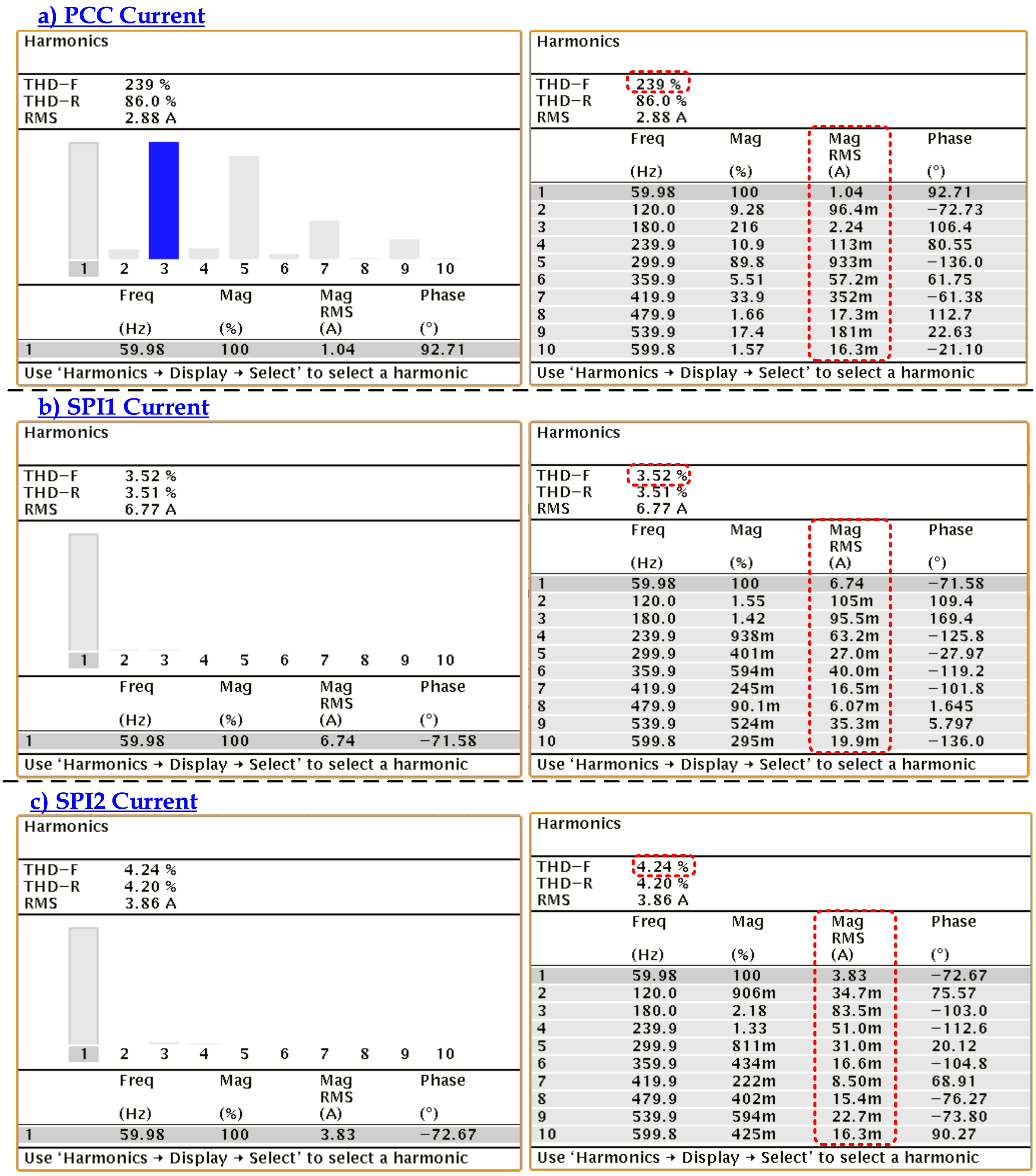


Figure 70 – Harmonic content analysis of load current at the PCC with SPIs injecting active and reactive terms.

7.2.2 Injection of Reactive Terms

Commercial inverters are already being ruled by a few regulations, requiring them to provide ancillary functionality to support the injection of the fundamental, in quadrature, current term (CPUC, 2013). Therefore, for this second case, the ability of the CBC to provide only reactive current sharing among the two SPIs was tested. The experimental result is presented in Fig. 71.

When comparing to the previous case, in which active plus reactive terms were supplied together, it is seen that the amplitudes of the synthesized currents of the SPI1 and SPI2 are

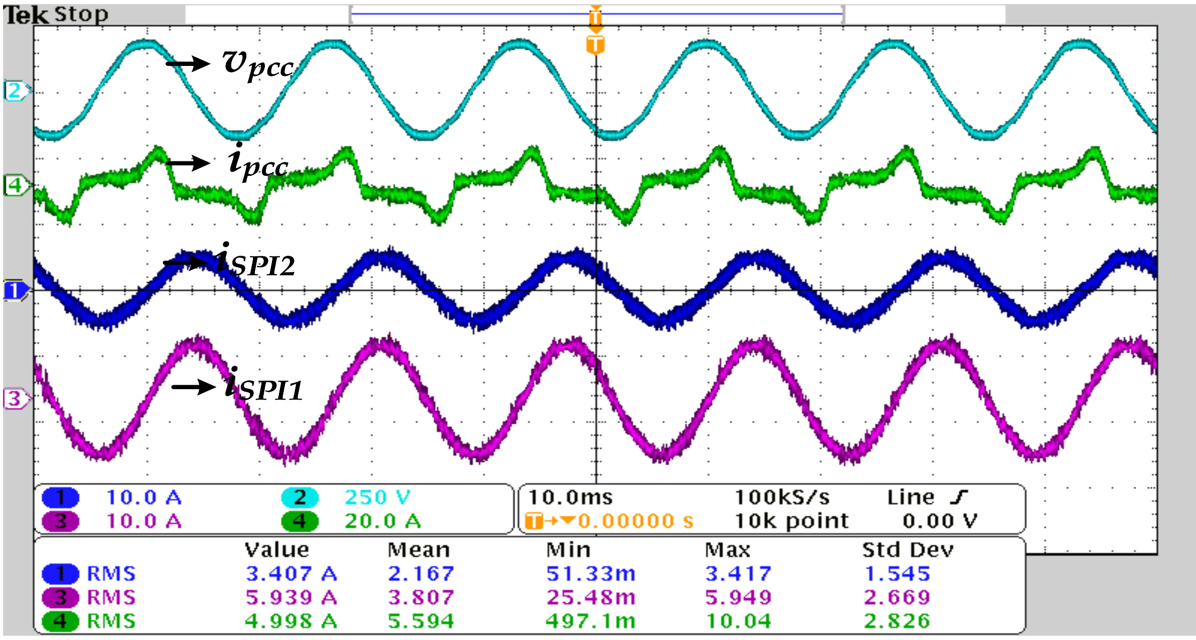


Figure 71 – SPIs cooperatively operating with the CBC injecting reactive terms.

lower, and again proportional participation is achieved, respecting the 0.6 proportion ratio. In addition, as expected for a quadrature term, such currents are in-phase with each other, but are still phase-shifted in relation to the grid voltage. The remaining PCC current, therefore, should present only active and harmonic terms, as it is seen.

By looking at Fig. 72-a, the harmonic spectrum shows that the fundamental component had its amplitude decreased in relation to the initial state, reducing from $9.71A$ to $4.71A$. Note that this remaining current presents higher rms value than the previous case considering injection of active plus reactive parcels.

Now, since only the fundamental quadrature term is being shared by the SPIs, if one pays attention to the phase of the PCC current, it proves that the remaining current is practically in-phase with the grid voltage (with $ph = 2.195°$), different from the initial state ($ph = -70.30°$) when the SPIs do not operate in Fig. 68. SPI1 and SPI2 generated currents presenting low THD_i, being respectively 3.30% and 5.00%. Again, no significant reduction is seen on other harmonic orders as expected.

For this case, the harmonic distortion of the PCC current was 58.70%, and two comments related to the mathematical definition of THD_i are highlighted. First, since in-phase fundamental current with significant amplitude is still flowing at the PCC, the denominator of eq. (4.30) is lower than on the initial case with SPIs only standing by ($THD_i = 25.10\%$), resulting in higher THD_i. Secondly, following the same ideia, in comparison to the previous case with active and reactive current injection, the THD_i at the PCC is lower as a result of a higher denominator due to the not shared active parcel.

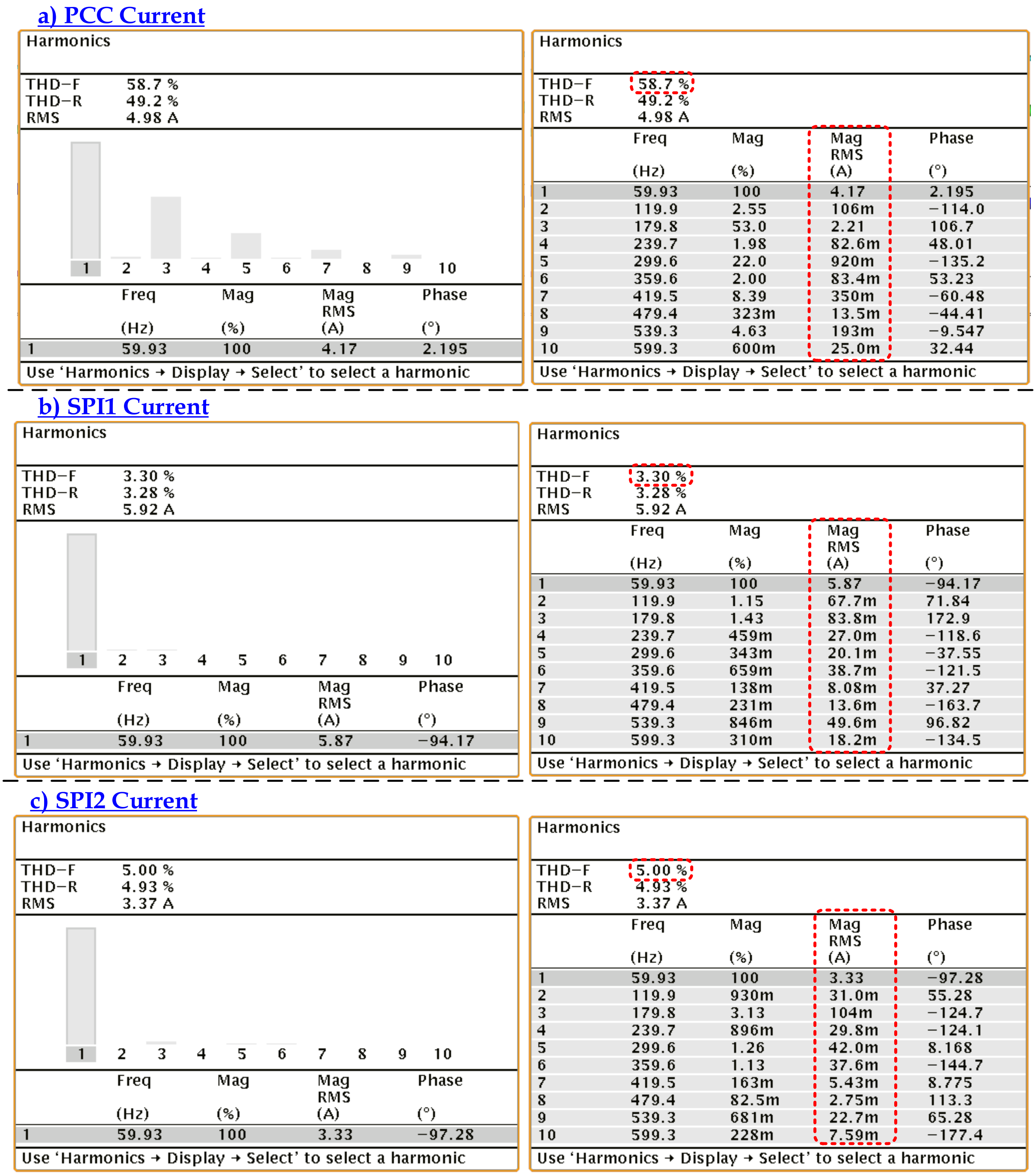


Figure 72 – Harmonic content analysis of load current at the PCC with SPIs injecting reactive terms.

7.2.3 Injection of Reactive and Third Harmonic Terms

In this case, an additional functionality is considered for the SPIs, aiming at reducing the 3^{rd} harmonic content at the PCC current. Fig. 73 presents the previous reactive current injection, being complemented by the SPIs sharing the demand for the in-phase and quadrature terms of the 3^{rd} harmonic order as well. It can be seen that the proportion between the peak values of the SPI currents still follow expected 0.6 ratio, also not exceeding the imposed inverter maximum currents.

As earlier analyzed, Fig. 74 is used as reference to demonstrate the current sharing

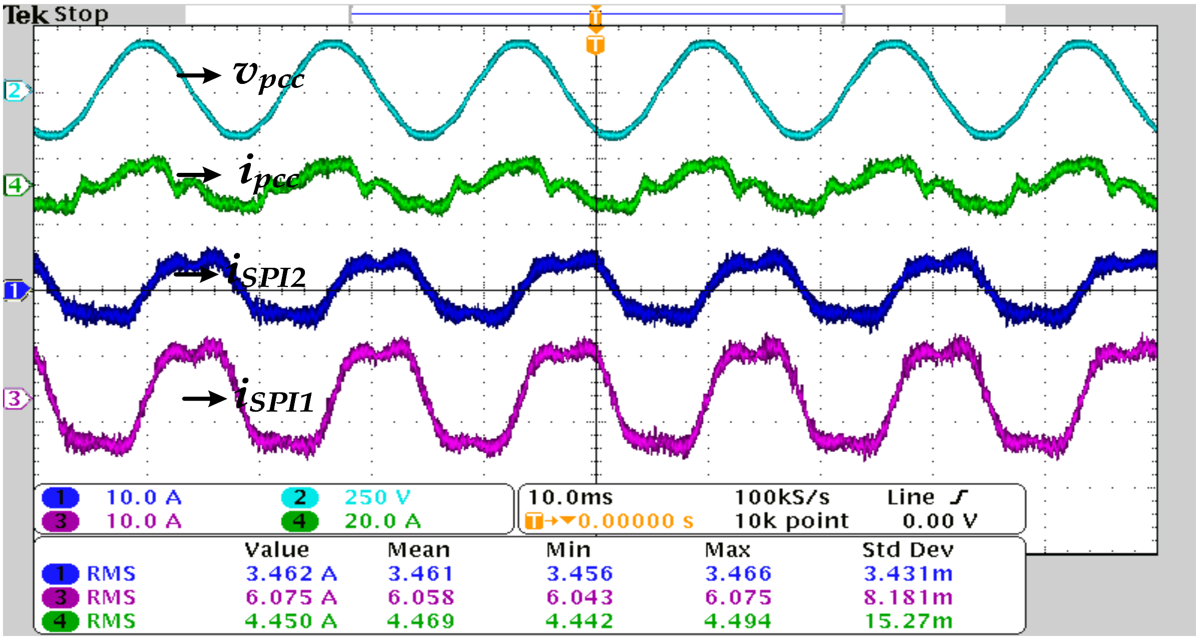
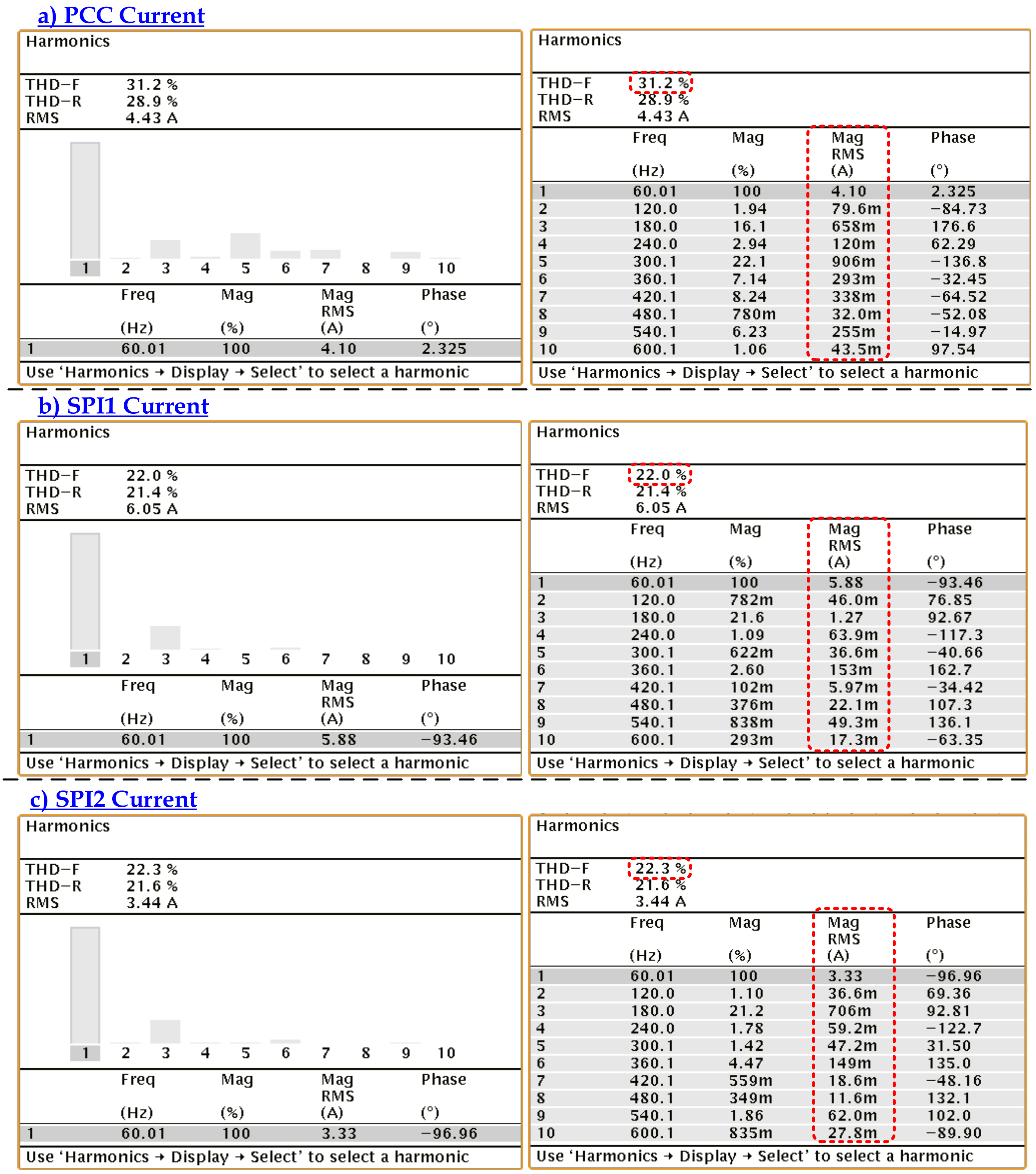


Figure 73 – SPIs cooperatively operating with the CBC injecting reactive and 3^{rd} harmonic terms.

results. Firstly, as expected by the injection of fundamental reactive currents, the PCC current is again in phase ($ph = 2.325°$) with the grid voltage, and presents practically the same rms value of $4.10A$ for the fundamental component. Secondly, in relation to the 3^{rd} harmonic component, it is then seen that the CBC provided adequate sharing of such terms between the SPIs, reducing the PCC current from $2.21A$ to a rms value of $0.658A$, while not affecting other harmonic orders. As a consequence, the THD_i decreased from 58.70% of the previous case with only reactive injection, to a condition of 31.20%. By injecting harmonic terms, as expected, the SPI currents are more distorted. SPI1 presented $THD_i = 22.0\%$ and SPI2 a $THD_i = 22.30\%$, and it is seen that the former also supplies higher magnitude of distorted current than the later.

It is reinforced that for this experiment, although the distortion factor could not attend codes as analyzed in some simulated cases, the 3^{rd} harmonic order current could not be completely diminished, other harmonic components are also present in the PCC current, and the magnitude of the active current ($4.10A$) in relation to the harmonic terms is low. All of those conditions contribute to the result of a high THD_i.



a) PCC Current

	Freq (Hz)	Mag (%)	Mag RMS (A)	Phase (°)
1	60.01	100	4.10	2.325
2	120.0	1.94	79.6m	−84.73
3	180.0	16.1	658m	176.6
4	240.0	2.94	120m	62.29
5	300.1	22.1	906m	−136.8
6	360.1	7.14	293m	−32.45
7	420.1	8.24	338m	−64.52
8	480.1	780m	32.0m	−52.08
9	540.1	6.23	255m	−14.97
10	600.1	1.06	43.5m	97.54

b) SPI1 Current

	Freq (Hz)	Mag (%)	Mag RMS (A)	Phase (°)
1	60.01	100	5.88	−93.46
2	120.0	782m	46.0m	76.85
3	180.0	21.6	1.27	92.67
4	240.0	1.09	63.9m	−117.3
5	300.1	622m	36.6m	−40.66
6	360.1	2.60	153m	162.7
7	420.1	102m	5.97m	−34.42
8	480.1	376m	22.1m	107.3
9	540.1	838m	49.3m	136.1
10	600.1	293m	17.3m	−63.35

c) SPI2 Current

	Freq (Hz)	Mag (%)	Mag RMS (A)	Phase (°)
1	60.01	100	3.33	−96.96
2	120.0	1.10	36.6m	69.36
3	180.0	21.2	706m	92.81
4	240.0	1.78	59.2m	−122.7
5	300.1	1.42	47.2m	31.50
6	360.1	4.47	149m	135.0
7	420.1	559m	18.6m	−48.16
8	480.1	349m	11.6m	132.1
9	540.1	1.86	62.0m	102.0
10	600.1	835m	27.8m	−89.90

Figure 74 – Harmonic content analysis of load current at the PCC with SPIs injecting reactive and 3^{rd} harmonic terms.

7.2.4 Injection of Third Harmonic Terms

A final case is here presented aiming at showing the distributed harmonic sharing provided by the CBC. In this experiment, the SPIs were commanded to inject only the third harmonic in-phase and quadrature terms. The results of this test are shown in Fig. 75.

Promptly, it can be noted how the SPI currents oscillates with a frequency three times higher ($3 \cdot 60Hz$) than the grid voltage and current. Since this component presents the most significant amplitude ($2.24A$) among the lower harmonic orders, once the SPIs share such component, it is expected a less distorted condition to appear at the PCC current. On the experi-

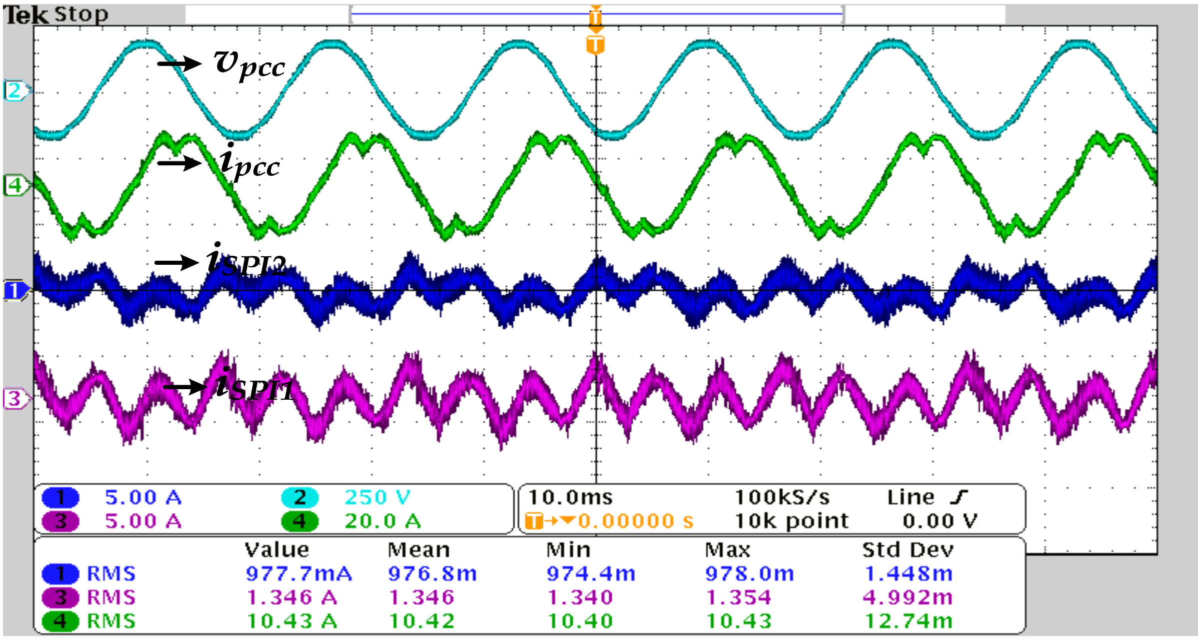


Figure 75 – SPIs cooperatively operating with the CBC injecting third harmonic terms.

mental result, this condition is verified as well, noting that initial distorted PCC current of Fig. 67 presented a more irregular shape than the one after the CBC operation. Since the reactive parcel is not supplied, the remaining current is phase-shifted in relation to the grid voltage ($ph = 153.90°$). As desired, it is noted again that the current of the SPI1 presents higher amplitude than the one from SPI2.

In regard of merit factors seen in Fig. 76, the THD_i of the grid current presented a value of 11.60%, which is the most considerable result achieved between these four experimental cases. With no injection of active and reactive terms, the fundamental harmonic band seems practically unchanged. The amplitudes around the third order frequency showed a expressive reduction from $2.24A$ to $0.605A$, even though not being totally diminished. As a result of injecting only harmonic terms, high THD_i values for the synthesized currents were attained, being 333% and 148% respectively for SPI1 and SPI2. Yet, it is noted that they could proportionally share the current demand, with respectively $1.15A$ and $0.630A$ for this term, practically following the expected 0.6 ratio.

However, due to some physical limitations aforementioned, as can be clearly seen on the results, it should be restated that the total SPI rms currents presented some imprecision, deviating approximately 20% from the expected ratio. Particularly for this case, it is known that CBC algorithm first generates the compensation references based on phasor sums of the third harmonic in-phase and quadrature terms, and after scales it (dividing onto smaller parcels) following the available SPI capabilities. Therefore, as the control reference current of each SPI presents small amplitude, the signal-noise ratio outcome, in relation to the sensed current, becomes more significant, making it more difficult for the inner loop controllers to reach a steady condition. This noise relation is a direct operational consequence of the improper filtering from the output L inductor, and also the high frequency switching distortion, making the task

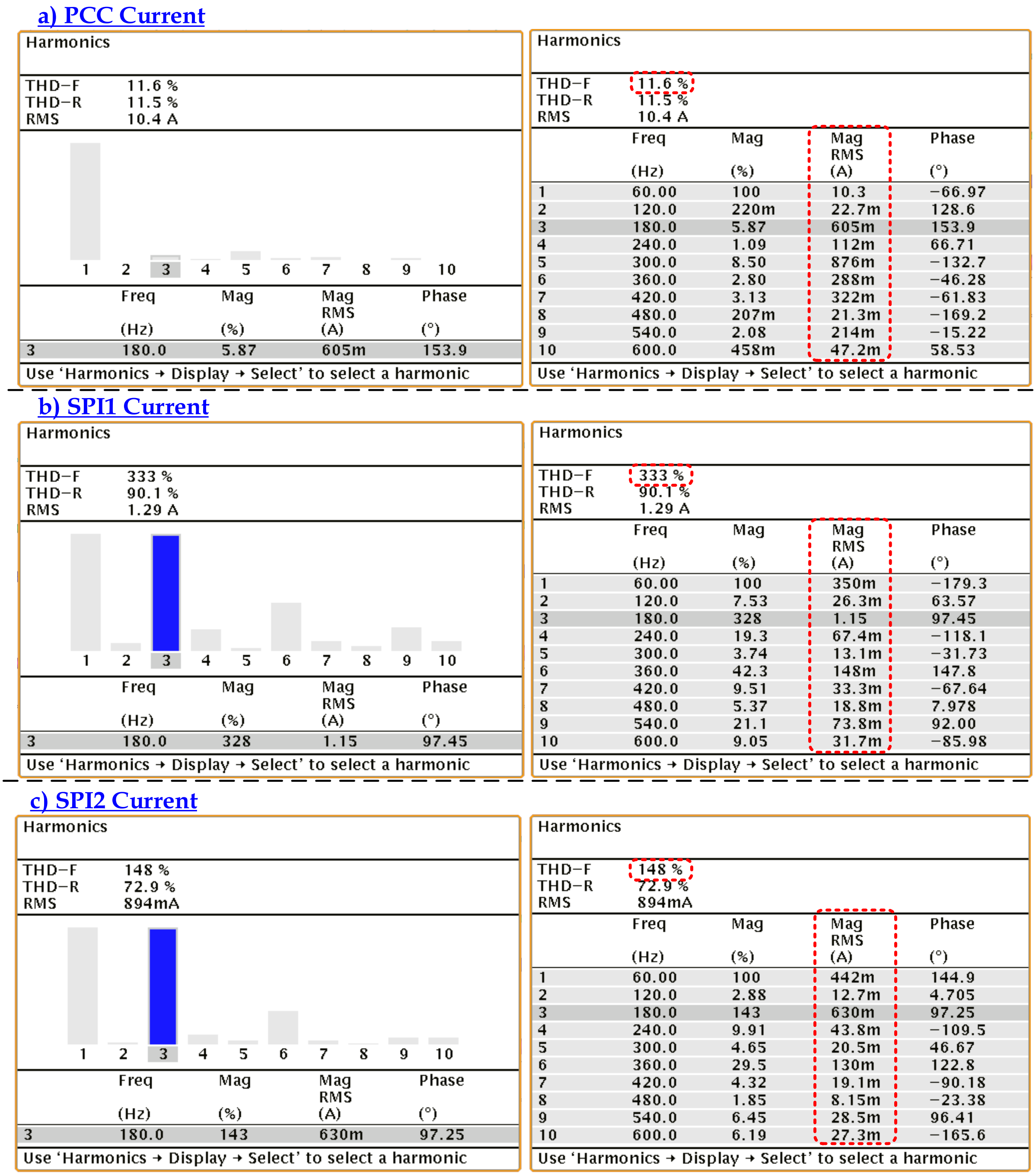


Figure 76 – Harmonic content analysis of load current at the PCC with SPIs injecting 3^{rd} harmonic terms.

of synthesizing small amplitude currents more difficult.

Nonetheless, these limitations are about to be overcome within the next and future development stages of this work, and results with better quality are expected to be obtained and expanded. In brief, from these four experiments discussed, it can be concluded that the CBC in fact shows an interesting approach to distributively coordinate the sharing of active, reactive, and in special, harmonic terms in a single-phase low-voltage microgrid under a master/slave architecture.

8 Final Conclusions

Distributed harmonic compensation obtained by means of multifunctional DGs, with accurate current sharing, is a prevailing and real challenging research topic, mainly due to the interactions among phases, nodes, line impedances and passive loads, as well as due to voltage deviations along the feeders. Furthermore, as the trend for more intelligent, robust and autonomous microgrid scenarios (OLIVARES *et al.*, 2014) are consolidated in modern energy systems, alternatives such as the Current-Based Control algorithm will be impulsed to be developed to give support to a more effective use of DGs. Having that in mind, this dissertation brought an alternative to provide a hierarchically coordinated operation of dispersed SPIs over a single-phase low-voltage microgrid, discussing not only this control methodology and its applications, but also presenting how such systems might be designed from the lower hardware level.

Chapter 2 tried to give an overview about how distributed energy systems with capability to employ compensation duties have been evolving and being applied for power quality enhancement. From the initial use of local passive filters, up to the future scenario of having many kinds of power conditioners dispersed, several consolidated methodologies were briefly discussed in a chronological sequence.

In Chapter 3, some of the most basic and general knowledge related to the architecture, modulation of PWM inverters was explained, intending to clarify how such systems operate. Along with that, comments were made on how SPIs can be modeled and may interact in grid-connected mode.

Some of the most employed current controllers were illustrated in Chapter 4, showing that many control approaches may be implemented, with each of them providing pros and cons under different perspectives. An evaluation was also presented aiming at justifying the use of PRes current controllers in simulations and experimental cases.

The foundation of the CBC algorithm was then broken down into three stages Chapter 5. Its active, reactive and harmonic current sharing methodology was discussed, intending to explain how it provides the interaction between a central controller and each of the active energy gateways. Besides, some brief comments on its, still under-development, advancements and constraints were made to explicit that several aspects need to be further evaluated.

Considering different realistic microgrid scenarios, in Chapter 6 the main contribution of this dissertation was presented, showing several simulation cases with focus on distributed harmonic compensation. It has been proved not only the effectiveness of the harmonic current sharing proposed by the CBC, but also the ability and flexibility to adequately to handle active and reactive terms. The simulations evaluated prospective conditions that will likely be, and already are, faced in single-phase low-voltage grids with high penetration level of DERs.

Although simulations are interesting tools for evaluating the performance of systems, complementary physically experimented results, as the one presented in Chapter 7, are able to solidify such statements. Therefore, the last part of this work first targeted the experimental implementation of a single-phase low voltage microgrid, comprising two full-bridge SPIs, with nonlinear load, being able to operate in grid-connected mode. Secondly, the operational capability of the CBC was preliminarily tested considering different operational goals for the grid current at the PCC. It was demonstrated that this methodology can be implemented for real applications, providing active, reactive, and harmonic sharing among distributed SPIs.

As final conclusion, it can be lastly said that the CBC was presented as a new and interesting alternative to provide coordination of DGs, power conditioners, and any other active elements that could interconnect with AC single-phase low-voltage microgrids. Active, reactive and harmonic sharing is achievable through this methodology, in way of that the power capabilities of the EGs are always respected, also allowing a balanced and proportional participation of all agents. The CBC can be, therefore, considered for playing a key role on the forthcoming small-scale distributed energy paradigm.

8.1 Future Works

Although several cases and scenarios were approached in this work, there still remains many questions that should be further evaluated for the consolidation of the Current-Based Control algorithm, and also its proposed methodology for sharing active, reactive and harmonics terms. Therefore, some of the following suggestions are left for development in future work:

1. Extension of the CBC methodology to be applied on current sharing among SPIs in three-phase three- or four-wire systems;

2. Further study the feasibility of the CBC operation considering different microgrid topologies, i.e. meshed and ring shaped, and also with more diversified technologies of DGs and power conditioners;

3. Integrate more intelligence to the reactive and harmonic compensation of the CBC by detecting the most critical terms to be mitigated and adaptively reorganizing the allocation of current capabilities;

4. Build a dense study on the stability matter of the distributed control provided by the CBC;

5. Analyze the impacts, issues and benefits of the CBC methodology under data transmission perspective, focusing on packet losses, intermittent transmission and delays in delivery windows;

6. Compare the effectiveness of the CBC in relation to other hierarchical and decentralized control methodologies, such as the PBC algorithm, and also droop-based approaches;

7. Study how the CBC and the Conservative Power Theory could be integrated to provide current sharing focusing on resistive load synthesis instead of sinusoidal current synthesis.

8. Evaluate if it would be possible to coordinate, based on the CBC, dispersed single-phase SPIs arbitrary connected in different phases of three-phase networks;

9. Expand the actual prototype developed to insert more SPIs, loads and line impedances for evaluation of more complex microgrid scenarios;

10. Implementation of a three-phase laboratory-scale prototype for evaluating the CBC and other distributed control methodologies;

11. Provide a more detailed and specific study on the impacts caused by the CBC operation in other nodes than the PCC, in regard to power quality conditions power losses;

12. Evaluate how the CBC could be enhanced in order to extend its operation to a multi-objective approach, not only aiming a global goal at the PCC, but also respecting local conditions in other specific nodes.

8.2 Correlated Publications

As part of the development of this work, and also throughout the studies directly and indirectly discussed on this master's dissertation, the following correlated publications occurred.

1. BRANDAO, D. I.; ALONSO, A. M. S.; MARAFAO, F. P.; MATTAVELLI., P.; CALDOGNETTO, T. Current-based hierarchical control for active, reactive and selective harmonic current sharing in smart microgrids. *IEEE Transactions on Power Electronics*, 2018. **SUBMITTED**

2. ALONSO, A. M. S.; BRANDAO, D. I.; MARAFAO, F. P. Controle coordenado de inversores multifuncionais para compensação distribuída de harmônicos em microrredes monofásicas de baixa tensão. In: *XXII Congresso Brasileiro de Automatica (CBA)*. [S.l.: s.n.], 2018. **SUBMITTED**

3. SAVOI, L.; ALONSO, A. M. S.; FERREIRA, W. M.; COUTO, H.; BRANDAO, D. I.; MARAFAO, F. P. Estratégia de controle para coordenação de conversores monofásicos e trisáficos distribuídos em microrredes. In: *XXII Congresso Brasileiro de Automatica (CBA)*. [S.l.: s.n.], 2018. **SUBMITTED**

4. FERREIRA, W. M.; BRANDAO, D. I.; SILVA, S. M.; ALONSO, A. M. S.; MARAFAO, F. P. Otimização multiobjetivo aplicado ao controle centralizado de uma microrrede de

baixa tensão: Controle de fluxo de potência e compensação de desbalanço. In: *XXII Congresso Brasileiro de Automatica (CBA)*. [S.l.: s.n.], 2018. **SUBMITTED**

5. MARAFAO, F. P.; ALONSO, A. M. S.; GONCALVES, F. A. S.; BRANDAO, D. I.; MARTINS, A. C. G.; PAREDES, H. K. M. Trends and constraints on brazilian photovoltaic industry: Energy policies, interconnection codes and equipment certification. *IEEE Transactions on Industry Applications*, 2018. **ACCEPTED**

6. BRANDAO, D. I.; POMILIO, J. A.; MARAFAO, F. P.; ALONSO, A. M. S. Validação experimental de uma arquitetura de microrrede completamente despáchavel. *(SOBRAEP) Revista Eletrônica de Potência*, 2017. **ACCEPTED**

7. LIBERADO, E. V.; POMILIO, J. A.; MARAFAO, F. P.; TEDESCHI, E.; ALONSO, A. M. S. Three/four-leg inverter current control based on generalized symmetrical components. In: *19^{th} IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*. Padova, Italy: [s.n.], 2018. **ACCEPTED**

8. ALONSO, A. M. S.; MARAFAO, F. P.; BRANDAO, D. I.; TEDESCHI, E.; GUERREIRO, J. F. A guideline for employing psim on power converter applications: Prototyping and educational tool. In: *Brazilian Power Electronics Conference (COBEP 2017)*. Juiz de Fora, MG - Brazil: [s.n.], 2017. Disponível em: <http://ieeexplore.ieee.org/document/8257284/>.

9. ALONSO, A. M. S.; MARAFAO, F. P.; GONCALVES, F. A. S.; PAREDES, H. K. M.; MARTINS, A. C. G.; BRANDAO, D. I. Pv microgeneration perspective in brazil: Approaching interconnection procedures and equipment certification. *9th Annual IEEE Green Technologies Conference*, 2017.

10. ALONSO, A. M. S.; MARAFAO, F. P.; GONCALVES, F. A. S.; PAREDES, H. K. M.; MARTINS, A. C. G. Consideracoes sobre a regulamentacao de microgeracao e certificacao de inversores no brasil. *12th IEEE/IAS International Conference on Industry Applications - INDUSCON 2016*, 2016.

11. MARTINS, A. S.; ALONSO, A. M. S.; MARAFAO, F. P.; GONCALVES, F. A. S.; PAREDES, H. K. M. Inversor trans-quase-fonte-z utilizando a modulacao constant boost control. *12th IEEE/IAS International Conference on Industry Applications - INDUSCON 2016*, 2016.

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Appendix

APPENDIX A – Auxiliar Pseudocode Algorithms

Pseudocode 3 Saturation Pseudocode

Input: Variable to be saturated
Output: Saturated variable

function SATURATION($Input$,$UpperLimit$,$LowerLimit$)
    if $Input > UpperLimit$ **then**
        $Aux \leftarrow UpperLimit$ ▷ "Aux" is an auxiliar variable
    else if $Input < LowerLimit$ **then**
        $Aux \leftarrow LowerLimit$
    else if $LowerLimit \leq Input \leq UpperLimit$ **then**
        $Aux \leftarrow Input$
    end if
    return (Aux)
end function

Pseudocode 4 Read Data Package

function READEGSDATAPACKAGE( )
    for $n \leftarrow 1$ to N **do** ▷ Loop for all EGs
        $I_{nom}^{fn} \leftarrow EG_n{:}Data_1$ ▷ $Data_x$ is any transmitted variable of **??**
        $I_{max}^{fn} \leftarrow EG_n{:}Data_2$
        for $h \leftarrow 1$ to H **do** ▷ Loop for all desired harmonic orders
            $I_{h_{||}} \leftarrow EG_n{:}Data_{h+2}$
            $I_{h_{\perp}} \leftarrow EG_n{:}Data_{h+3}$
        end for
        $I_{nom}^{ft} \leftarrow I_{nom}^{ft} + I_{nom}^{fn}$
        $I_{max}^{ft} \leftarrow I_{max}^{ft} + I_{max}^{fn}$
    end for
end function

Pseudocode 5 Gather Control Data from CC Pseudocode

Input: $\alpha_{||}$ and $\alpha_{\perp}$ commands calculated for each harm. order
Output: A data vector with all the scaling commands of the current CBC cycle

function CONTROLDATAPACKAGE($Coef_{h_{||}}$,$Coef_{h_{\perp}}$) ▷ $Coef_{h_{||}}$ and $Coef_{h_{\perp}}$ are auxiliar variables
    $CtrlPackage[j] = Coef_{h_{||}}$
    $CtrlPackage[j+1] = Coef_{h_{\perp}}$
    $j \leftarrow j + 1$
    if $(j+1) == H$ **then**
        $j \leftarrow 0$
    end if
end function

Pseudocode 6 Send α Commands to EGs Pseudocode

Output: Data package with all control commands sent to all the SPIs

preload: $CtrlPackage[n]$ ▷ Processed in *ControlDataPackage()* - "n" is the size of the vector
function DISPATCHCONTROLDATAPACKAGE( )
    Enable data transmission links with all SPIs
    Send $CtrlPackage[n]$ **to all SPIs**
end function

APPENDIX B – Conservative Power Theory - Merit Factors

The Conservative Power Theory (CPT) is a time-domain proposed power theory (TENTI *et al.*, 2011; PAREDES, 2011), which can be applied to single- or poly-phase circuits with periodic quantities, regardless if it is under sinusoidal, asymmetrical or distorted voltage conditions. Electrical current and power components may be decoupled by the CPT, following physical representations defined upon conservative terms, which are the related to the average active power (P), reactive energy (W), distortion peculiarities (D) and load unbalance features (N). Since the work in this dissertation only targets single-phase systems, the load unbalance components have no meaning here, therefore being unconsidered. In regard to the other terms, following the same respective order presented, the following corresponding subscripts are used: "a", "r", "v".

In a simplified way, the decomposition of an instantaneous current "i" can then be resumed by the definitions of the CPT as given by eq. (B.1).

$$i = i_a + i_r + i_v \tag{B.1}$$

Given a single-phase system with equivalent conductance "G", the active current of the system is defined by eq. (B.2), where "V" stands for the RMS value and "v" for the instantaneous waveform of the circuit voltage.

$$i_a = \frac{P}{V^2} \cdot v = G \cdot v \tag{B.2}$$

Following the same ideia of P, for a period "T", the reactive energy (W) is calculated by eq. (B.3), where "$\widehat{v}$" is defined as the unbiased integral of the v, given by eq. (B.4).

$$W = \frac{1}{T} \cdot \int_0^T \widehat{v} \cdot i \cdot dt \tag{B.3}$$

$$\widehat{v} = \int_0^t \widehat{v(\tau)} \cdot d\tau - \int_0^T \widehat{v}(t) \cdot dt \tag{B.4}$$

Consequently, the CPT‘s reactive current is defined as in eq. (B.5), knowing that "B" stands for the equivalent susceptance of the circuit.

$$i_r = \frac{W}{\widehat{V}^2} \cdot \widehat{v} = B \cdot \widehat{v} \tag{B.5}$$

The last current parcel, named as void term, is given by the remaining current on the circuit as in eq. (B.6), which is responsible for the possible harmonic distortion effects.

$$i_v = i - i_a - i_r \tag{B.6}$$

Having these decomposed currents, from the calculation of their individual RMS values (I_x), the CPT finally defines its respective apparent (A), active (P), reactive (Q) and distortion (D) powers by eq. (B.7).

$$\begin{aligned} A^2 &= V^2 \cdot I_a^2 + V^2 \cdot I_r^2 + V^2 \cdot I_v^2 \\ A^2 &= P^2 + Q^2 + D^2 \end{aligned} \tag{B.7}$$

With the basics of the CPT definitions defined, the intended merit factors of a circuit can be briefly discussed. The three most important are: the power factor (λ), the reactivity factor (λ_Q), and the distortion factor (λ_D).

Following the most general definition of power factor, the (λ) term is formulated by eq. (B.8). However, since the apparent power A considers also the distortion power, it presents a more adequate representation of the active current circulation on the circuit, even is non-sinusoidal voltage conditions occur. Also due to its definition, this factor can then be affected by the presence of reactive and void current terms present on the circuit, being unitary if only active current exists.

$$\lambda = \frac{P}{A} \tag{B.8}$$

The reactivity factor (λ_Q) is related to the presence of electrical components with phase-shifting features on the circuit, such as inductors, capacitors and thyristor rectifiers, impacting on the circulation of reactive currents. For a single-phase system, it is defined as in eq. (B.9).

$$\lambda_Q = \frac{Q}{\sqrt{P^2 + Q^2}} \tag{B.9}$$

Finally, the distortion factor may be used as a parameter for evaluating the presence of nonlinear behaviors of loads, caused by distorted currents. (λ_v) is calculated by eq. (B.10), and should be zero if no distortion is present on the circulating currents, which has an equivalence with a null THD_i.

$$\lambda_v = \frac{D}{A} \tag{B.10}$$

APPENDIX C – Pictures of the Experimental Prototype

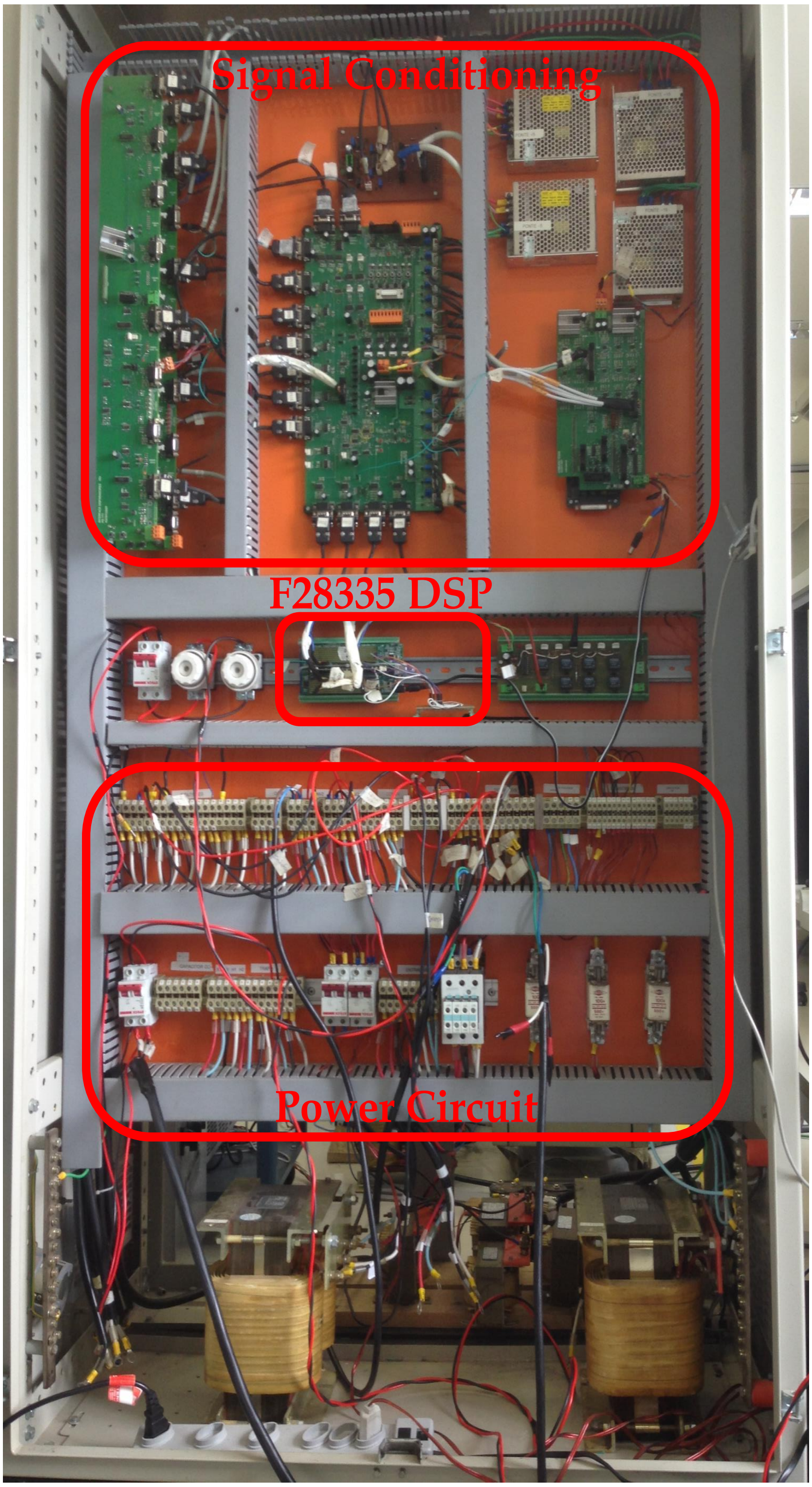

Figure 77 – Front of the power conditioner cabinet.

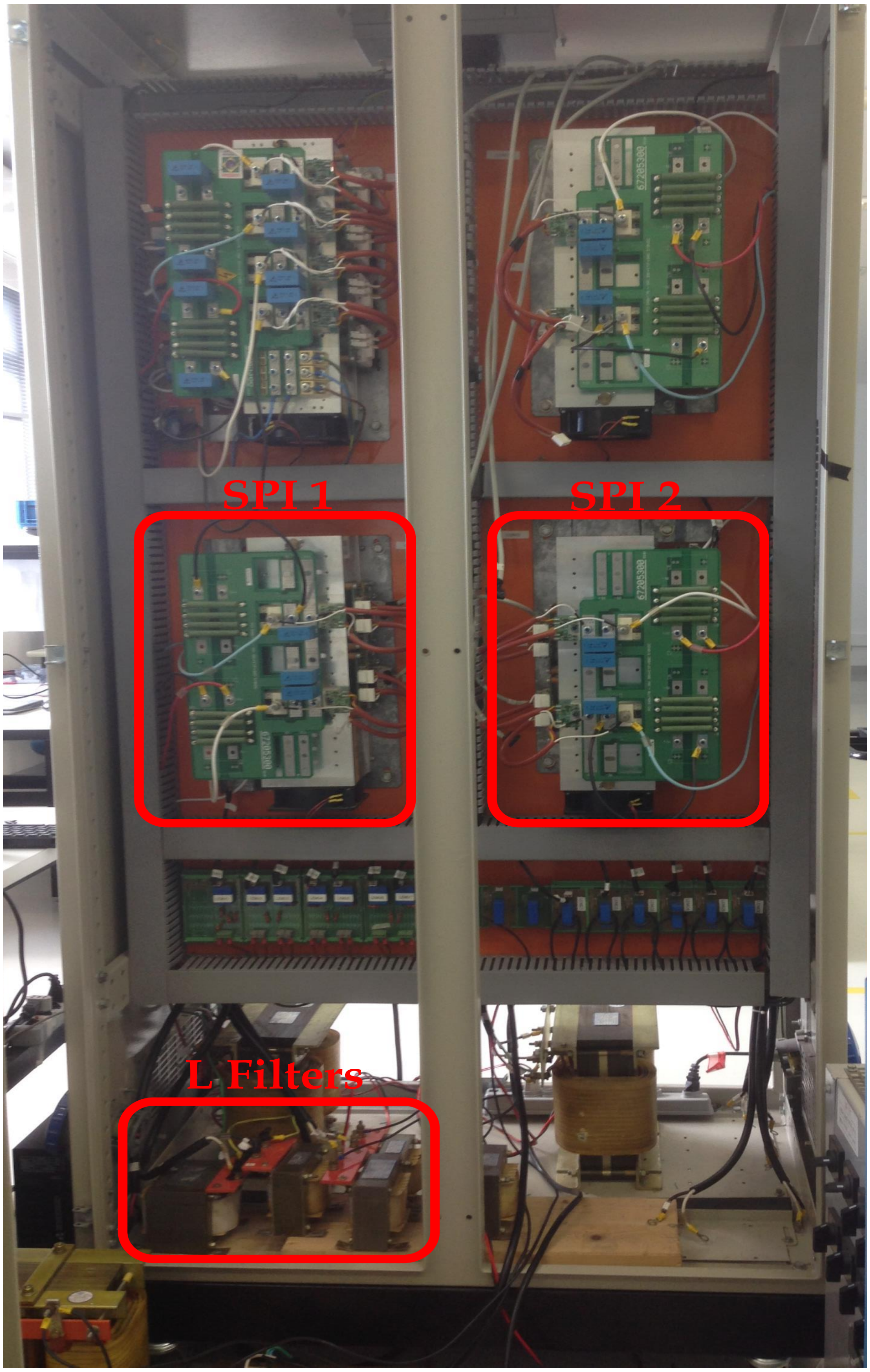

Figure 78 – Back of the power conditioner cabinet.

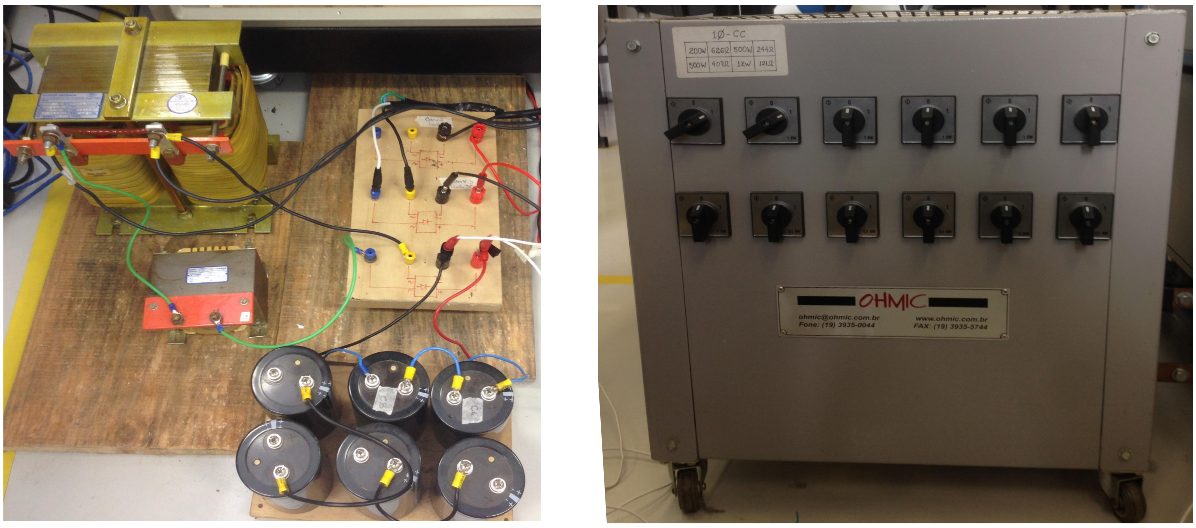

Figure 79 – Nonlinear load assembled.

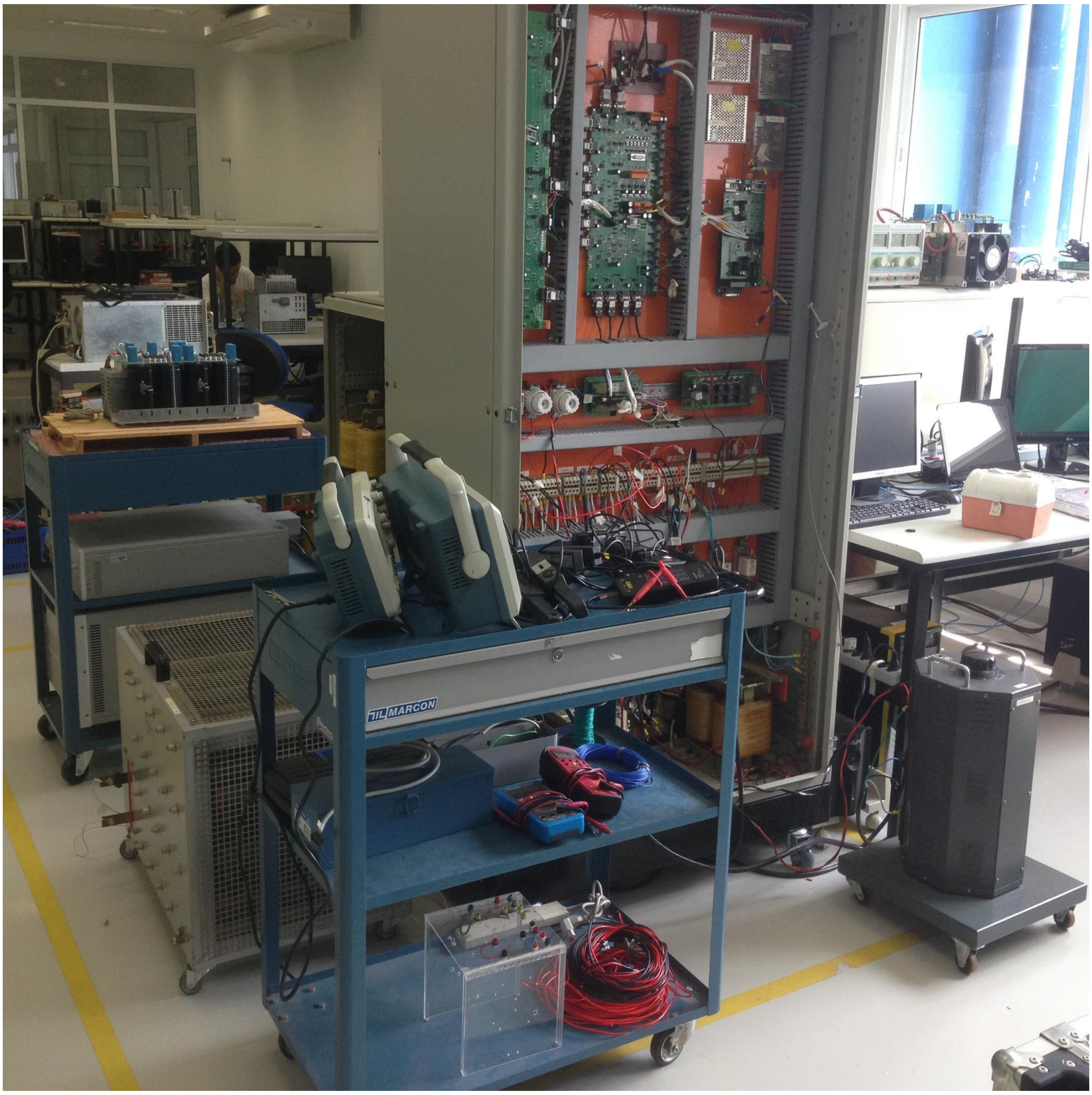
Figure 80 – Frontal perspective of the entire prototype.

APPENDIX D – Primary and Secondary Level Controllers Algorithms

```
static double Tsh = 0.000083333;

//P+Resonant
static double KPI = 1.60;
static double pia, limit_ia;
static double errora0, errora1, errora2;
static double presa1;
static double presa[4] = {0,0,0,0};
static double pres_1a[4] = {0,0,0,0};
static double pres_2a[4] = {0,0,0,0};
static double a[4] = {0.0054986433,0.0054878134,0.0054662813,0.0054342979};
static double b[4] = {1.9990132830,1.9911370377,1.9754772576,1.9522166518};
static double pres_ia;
static double pib, limit_ib;
static double errorb0, errorb1, errorb2;
static double presb1;
static double presb[4] = {0,0,0,0};
static double pres_1b[4] = {0,0,0,0};
static double pres_2b[4] = {0,0,0,0};
static double pres_ib;
static int i;

//Relay_Control (Initializes_PWM_modulation_for_SPIs)
static int relay = 0, init = 0;
static unsigned long count = 0;

//SPIs_Control
static double inva, errora, refi;
static double invb, errorb;
static double Kramp=0.0;
static double taa=0.0, tbb=0.0;

// ////////////PLL_pcc
//PLL_Fund.
static double pii=3.141592653589793;
static double Vrede, w, teta; //(q-p) Quadrature and In-phase components
static double pll_q=0.0, pll_p=0.0;
static int samples=0, first_done=0;
static double dp=0.0, mean_dp=0.0, sum_dp=0.0, maf_dp[200];
//PLL PI Controller
static double PLL_kp=200, PLL_ki=4000; //Canonical Method - 2nd Order
static double PI_PLL, error_pll, PI_limit;
static double PI_kp = 0.0;
static double PI_ki = 0.0;
//PLL_Harms.
static double tet3a; //3rd_harm
static double pll_3q=0.0, pll_3p=0.0;
static double tet5a; //5th_harm
static double pll_5q=0.0, pll_5p=0.0;

//##################PLL_NODE2
//PLL_Fund.
```

```
static double V2n, w2n, teta2n; //(q-p) Quadrature and In-phase components
static double pll2n_q=0.0, pll2n_p=0.0;
static double dp2n=0.0, mean2n_dp=0.0, sum2n_dp=0.0, maf2n_dp[200];
//PLL PI Controller
static double PI2n_PLL, error2n_pll, PI2n_limit;
static double PI2n_kp = 0.0;
static double PI2n_ki = 0.0;
//PLL_Harms.
static double tet3a2n;//3rd_harm
static double pll2n_3q=0.0, pll2n_3p=0.0;
static double tet5a2n;//5th_harm
static double pll2n_5q=0.0, pll2n_5p=0.0;

//##################PLL_NODE1
//PLL_Fund.
static double V1n, w1n, teta1n; //(q-p) Quadrature and In-phase components
static double pll1n_q=0.0, pll1n_p=0.0;
static double dp1n=0.0, mean1n_dp=0.0, sum1n_dp=0.0, maf1n_dp[200];
//PLL PI Controller
static double PI1n_PLL, error1n_pll, PI1n_limit;
static double PI1n_kp = 0.0;
static double PI1n_ki = 0.0;
//PLL_Harms.
static double tet3a1n;//3rd_harm
static double pll1n_3q=0.0, pll1n_3p=0.0;
static double tet5a1n;//5th_harm
static double pll1n_5q=0.0, pll1n_5p=0.0;

//PWM_Trip
static unsigned long count2=0;
static int trip_cmd=1;

//Filter_SPI_current (for PWM trip)
static double inva_filter=0.0;
static double invb_filter=0.0;

//Current_Control_Reference
static double i_ctrl=0.0;

static double i_pcc=0.0;

//Peak_Detection_PCC
static double maf_1p[200], sum_1p, peak_1p;
static double maf_1q[200], sum_1q, peak_1q;
static double maf_3p[200], sum_3p, peak_3p;
static double maf_3q[200], sum_3q, peak_3q;
static double maf_5p[200], sum_5p, peak_5p;
static double maf_5q[200], sum_5q, peak_5q;

//Peak_Detection_EG1=EGa
static double maf_1pEGa[200], sum_1pEGa, peak_1pEGa;
static double maf_1qEGa[200], sum_1qEGa, peak_1qEGa;
static double maf_3pEGa[200], sum_3pEGa, peak_3pEGa;
static double maf_3qEGa[200], sum_3qEGa, peak_3qEGa;
static double maf_5pEGa[200], sum_5pEGa, peak_5pEGa;
static double maf_5qEGa[200], sum_5qEGa, peak_5qEGa;
static double itotal_EGa=0.0;
```

```
//Peak_Detection_EG2=EGb
static double maf_1pEGb[200], sum_1pEGb, peak_1pEGb;
static double maf_1qEGb[200], sum_1qEGb, peak_1qEGb;
static double maf_3pEGb[200], sum_3pEGb, peak_3pEGb;
static double maf_3qEGb[200], sum_3qEGb, peak_3qEGb;
static double maf_5pEGb[200], sum_5pEGb, peak_5pEGb;
static double maf_5qEGb[200], sum_5qEGb, peak_5qEGb;
static double itotal_EGb=0.0;

//Current_Based_Control
//PCC+EGa+EGb
static double Imaxa, Imaxb, Imax, I2max; //Max._Current_Capab.=Max_Generation(DER)
static double DI, DIa, DIb, Io; //DeltaI:ActualCapability//Io:ActiveCurrentCtrlRef
static double a1p, a1q; //alphas_fundamental
static double a3p, a3q;
static double a5p, a5q;
static double P1EGt, Q1EGt; //total_current_EGs
static double P3EGt, Q3EGt;
static double P5EGt, Q5EGt;
static double iP1EGa, iQ1EGa; //final_CBC_current_ref
static double iP1EGb, iQ1EGb;
static double iP3EGa, iQ3EGa;
static double iP3EGb, iQ3EGb;
static double iP5EGa, iQ5EGa;
static double iP5EGb, iQ5EGb;
static double disp_a1p, disp_a1q, disp_a3p, disp_a3q, disp_a5p, disp_a5q;
static int dispatch=0;

static double disp_P1EGt, disp_Q1EGt; //total_EGs
static double disp_P3EGt, disp_Q3EGt; //total_EGs
static double disp_P5EGt, disp_Q5EGt; //total_EGs
static int counter=0;

//INPUTS
inva = x1;
inva_filter = x2; //filter is outside C block
invb = x3;
invb_filter = x4;
Vrede = x5;
i_pcc = x6;
V2n = x7;
V1n = x8;

//#######################
//Current_Ratings

Imaxa = (6.0/20); //p.u.
Imaxb = (4.0/20);

Imax = Imaxa + Imaxb;
I2max = (Imax)*(Imax);
//Io = (0.00/20);

Io = (0.0/20); //$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

//#######################
```

```
//######################_START PLL
//Dot Product
dp = Vrede*pll_q;
  //###Node2
  dp2n = V2n*pll2n_q;
  //###Node1
  dp1n = V1n*pll1n_q;

if(samples>=200)
{
  samples = 0;
  first_done = 1;
}
//MAF
if(first_done==0)//1st Cycle
{
  //Fund.
  pll_p = 0.0;
  pll_q = 0.0;
  w = 0.0;
  teta = 0.0;
  maf_dp[samples] = 0.0;
  sum_dp += dp;
  mean_dp = sum_dp/200;
  //Harms.
  pll_3p = 0.0;
  pll_3q = 0.0;
  tet3a = 0.0;
  pll_5p = 0.0;
  pll_5q = 0.0;
  tet5a = 0.0;

    //###Node2
    //Fund.
    pll2n_p = 0.0;
    pll2n_q = 0.0;
    w2n = 0.0;
    teta2n = 0.0;
    maf2n_dp[samples] = 0.0;
    sum2n_dp += dp2n;
    mean2n_dp = sum2n_dp/200;
    //Harms.
    pll2n_3p = 0.0;
    pll2n_3q = 0.0;
    tet3a2n = 0.0;
    pll2n_5p = 0.0;
    pll2n_5q = 0.0;
    tet5a2n = 0.0;

    //###Node1
    //Fund.
    pll1n_p = 0.0;
    pll1n_q = 0.0;
    w1n = 0.0;
    teta1n = 0.0;
    maf1n_dp[samples] = 0.0;
```

```
    sum1n_dp += dp1n;
    mean1n_dp = sum1n_dp/200;
    //Harms.
    pll1n_3p = 0.0;
    pll1n_3q = 0.0;
    tet3a1n = 0.0;
    pll1n_5p = 0.0;
    pll1n_5q = 0.0;
    tet5a1n = 0.0;
}
else if (first_done==1)//After 1st Cycle
{
  sum_dp += dp - maf_dp[samples];
  maf_dp[samples] = dp;
  mean_dp = sum_dp/200;

    //###Node2
    sum2n_dp += dp2n - maf2n_dp[samples];
    maf2n_dp[samples] = dp2n;
    mean2n_dp = sum2n_dp/200;

    //###Node1
    sum1n_dp += dp1n - maf1n_dp[samples];
    maf1n_dp[samples] = dp1n;
    mean1n_dp = sum1n_dp/200;
}

//PLL_PI_Controller
error_pll = 0.00 - mean_dp; //ref - dp = 0 - dp;
PI_kp = error_pll*PLL_kp; //proportional
PI_ki += error_pll*PLL_ki*Tsh; //integral
PI_PLL = PI_kp + PI_ki; //PI

  //###Node2
  error2n_pll = 0.00 - mean2n_dp;
  PI2n_kp = error2n_pll*PLL_kp;
  PI2n_ki += error2n_pll*PLL_ki*Tsh;
  PI2n_PLL = PI2n_kp + PI2n_ki;

  //###Node1
  error1n_pll = 0.00 - mean1n_dp;
  PI1n_kp = error1n_pll*PLL_kp;
  PI1n_ki += error1n_pll*PLL_ki*Tsh;
  PI1n_PLL = PI1n_kp + PI1n_ki;

//Fund.
w = PI_PLL + 376.9911184307; //w0 = 2*pi*60
teta += w*Tsh;
//Saturation
if(teta >= 2*pii)
{
  teta = teta - (2*pii);
}
//In-quadrature
pll_q = sin(teta);
//pll_p = sin(teta + pii/2);
//In-phase
```

```
pll_p = cos(teta);

  //###Node2
  w2n = PI2n_PLL + 376.9911184307; //w0 = 2*pi*60
  teta2n += w2n*Tsh;
  //Saturation
  if(teta2n >= 2*pii)
  {
    teta2n = teta2n - (2*pii);
  }
  //In-quadrature
  pll2n_q = sin(teta2n);
  //pll_p = sin(teta + pii/2);
  //In-phase
  pll2n_p = cos(teta2n);

  //###Node1
  w1n = PI1n_PLL + 376.9911184307; //w0 = 2*pi*60
  teta1n += w1n*Tsh;
  //Saturation
  if(teta1n >= 2*pii)
  {
    teta1n = teta1n - (2*pii);
  }
  //In-quadrature
  pll1n_q = sin(teta1n);
  //pll_p = sin(teta + pii/2);
  //In-phase
  pll1n_p = cos(teta1n);

//Harms.
//3rd
tet3a += 3.0*w*Tsh;
if(tet3a >= 2*pii)
{
  tet3a = tet3a - (2*pii);
}
pll_3q = sin(tet3a);
pll_3p = cos(tet3a);
//5th
tet5a += 5.0*w*Tsh;
if(tet5a >= 2*pii)
{
  tet5a = tet5a - (2*pii);
}
pll_5q = sin(tet5a);
pll_5p = cos(tet5a);

  //###Node2
  //Harms.
  //3rd
  tet3a2n += 3.0*w2n*Tsh;
  if(tet3a2n >= 2*pii)
  {
    tet3a2n = tet3a2n - (2*pii);
  }
  pll2n_3q = sin(tet3a2n);
```

```
  pll2n_3p = cos(tet3a2n);
  //5th
  tet5a2n += 5.0*w2n*Tsh;
  if(tet5a2n >= 2*pii)
  {
    tet5a2n = tet5a2n - (2*pii);
  }
  pll2n_5q = sin(tet5a2n);
  pll2n_5p = cos(tet5a2n);

  //###Node1
  //Harms.
  //3rd
  tet3a1n += 3.0*w1n*Tsh;
  if(tet3a1n >= 2*pii)
  {
    tet3a1n = tet3a1n - (2*pii);
  }
  pll1n_3q = sin(tet3a1n);
  pll1n_3p = cos(tet3a1n);
  //5th
  tet5a1n += 5.0*w1n*Tsh;
  if(tet5a1n >= 2*pii)
  {
    tet5a1n = tet5a1n - (2*pii);
  }
  pll1n_5q = sin(tet5a1n);
  pll1n_5p = cos(tet5a1n);
//#######################_END_PLL

//#######################_Peak_Detection
if(first_done==0) //1stCycle
{
  //PCC
  maf_1p[samples] = 0.0;
  peak_1p = 0.0;
  sum_1p = 0.0;
  maf_1q[samples] = 0.0;
  peak_1q = 0.0;
  sum_1q = 0.0;
  maf_3p[samples] = 0.0;
  peak_3p = 0.0;
  sum_3p = 0.0;
  maf_3q[samples] = 0.0;
  peak_3q = 0.0;
  sum_3q = 0.0;
  maf_5p[samples] = 0.0;
  peak_5p = 0.0;
  sum_5p = 0.0;
  maf_5q[samples] = 0.0;
  peak_5q = 0.0;
  sum_5q = 0.0;

  //EG1=EGa
  //h=1
  maf_1pEGa[samples] = 0.0;
  peak_1pEGa = 0.0;
```

```
  sum_1pEGa = 0.0;
  maf_1qEGa[samples] = 0.0;
  peak_1qEGa = 0.0;
  sum_1qEGa = 0.0;
  //h=3
  maf_3pEGa[samples] = 0.0;
  peak_3pEGa = 0.0;
  sum_3pEGa = 0.0;
  maf_3qEGa[samples] = 0.0;
  peak_3qEGa = 0.0;
  sum_3qEGa = 0.0;
  //h=5
  maf_5pEGa[samples] = 0.0;
  peak_5pEGa = 0.0;
  sum_5pEGa = 0.0;
  maf_5qEGa[samples] = 0.0;
  peak_5qEGa = 0.0;
  sum_5qEGa = 0.0;

  //EG2=EGb
  //h=1
  maf_1pEGb[samples] = 0.0;
  peak_1pEGb = 0.0;
  sum_1pEGb = 0.0;
  maf_1qEGb[samples] = 0.0;
  peak_1qEGb = 0.0;
  sum_1qEGb = 0.0;
  //h=3
  maf_3pEGb[samples] = 0.0;
  peak_3pEGb = 0.0;
  sum_3pEGb = 0.0;
  maf_3qEGb[samples] = 0.0;
  peak_3qEGb = 0.0;
  sum_3qEGb = 0.0;
  //h=5
  maf_5pEGb[samples] = 0.0;
  peak_5pEGb = 0.0;
  sum_5pEGb = 0.0;
  maf_5qEGb[samples] = 0.0;
  peak_5qEGb = 0.0;
  sum_5qEGb = 0.0;

  P1EGt = 0.00;
  Q1EGt = 0.00;
  P3EGt = 0.00;
  Q3EGt = 0.00;
  P5EGt = 0.00;
  Q5EGt = 0.00;
}
else if(first_done==1)//After1st
{
  //PCC
    //h=1
    sum_1p += 2*i_pcc*pll_p - maf_1p[samples];
    maf_1p[samples] = 2*i_pcc*pll_p;
      peak_1p = (sum_1p)/200; //peak_value
    sum_1q += 2*i_pcc*pll_q - maf_1q[samples];
```

```
    maf_1q[samples] = 2*i_pcc*pll_q;
      peak_1q = (sum_1q)/200; //peak_value
    //h=3
    sum_3p  += 2*i_pcc*(pll_3p) - maf_3p[samples];
    maf_3p[samples] = 2*i_pcc*(pll_3p);
      peak_3p = (sum_3p)/200;
    sum_3q += 2*i_pcc*(pll_3q) - maf_3q[samples];
    maf_3q[samples] = 2*i_pcc*(pll_3q);
      peak_3q = (sum_3q)/200;
    //h=5
    sum_5p += 2*i_pcc*pll_5p - maf_5p[samples];
    maf_5p[samples] = 2*i_pcc*pll_5p;
      peak_5p = (sum_5p)/200;
    sum_5q += 2*i_pcc*pll_5q - maf_5q[samples];
    maf_5q[samples] = 2*i_pcc*pll_5q;
      peak_5q = (sum_5q)/200;

  //EG1=EGa
    //h=1
    sum_1pEGa += 2*inva*pll2n_p - maf_1pEGa[samples];
    maf_1pEGa[samples] = 2*inva*pll2n_p;
      peak_1pEGa = (sum_1pEGa)/200; //peak_value
    sum_1qEGa += 2*inva*pll2n_q - maf_1qEGa[samples];
    maf_1qEGa[samples] = 2*inva*pll2n_q;
      peak_1qEGa = (sum_1qEGa)/200; //peak_value
    //h=3
    sum_3pEGa += 2*inva*pll2n_3p - maf_3pEGa[samples];
    maf_3pEGa[samples] = 2*inva*pll2n_3p;
      peak_3pEGa = (sum_3pEGa)/200; //peak_value
    sum_3qEGa += 2*inva*pll2n_3q - maf_3qEGa[samples];
    maf_3qEGa[samples] = 2*inva*pll2n_3q;
      peak_3qEGa = (sum_3qEGa)/200; //peak_value
    //h=5
    sum_5pEGa += 2*inva*pll2n_5p - maf_5pEGa[samples];
    maf_5pEGa[samples] = 2*inva*pll2n_5p;
      peak_5pEGa = (sum_5pEGa)/200; //peak_value
    sum_5qEGa += 2*inva*pll2n_5q - maf_5qEGa[samples];
    maf_5qEGa[samples] = 2*inva*pll2n_5q;
      peak_5qEGa = (sum_5qEGa)/200; //peak_value

  //EG1=EGb
    //h=1
    sum_1pEGb += 2*invb*pll1n_p - maf_1pEGb[samples];
    maf_1pEGb[samples] = 2*invb*pll1n_p;
      peak_1pEGb = (sum_1pEGb)/200; //peak_value
    sum_1qEGb += 2*invb*pll1n_q - maf_1qEGb[samples];
    maf_1qEGb[samples] = 2*invb*pll1n_q;
      peak_1qEGb = (sum_1qEGb)/200; //peak_value
    //h=3
    sum_3pEGb += 2*invb*pll1n_3p - maf_3pEGb[samples];
    maf_3pEGb[samples] = 2*invb*pll1n_3p;
      peak_3pEGb = (sum_3pEGb)/200; //peak_value
    sum_3qEGb += 2*invb*pll1n_3q - maf_3qEGb[samples];
    maf_3qEGb[samples] = 2*invb*pll1n_3q;
      peak_3qEGb = (sum_3qEGb)/200; //peak_value
    //h=5
    sum_5pEGb += 2*invb*pll1n_5p - maf_5pEGb[samples];
```

```
    maf_5pEGb[samples] = 2*invb*pll1n_5p;
      peak_5pEGb = (sum_5pEGb)/200; //peak_value
    sum_5qEGb += 2*invb*pll1n_5q - maf_5qEGb[samples];
    maf_5qEGb[samples] = 2*invb*pll1n_5q;
      peak_5qEGb = (sum_5qEGb)/200; //peak_value

  //Injected_PeakCurrents_@_Cycle_k
  disp_P1EGt = peak_1pEGa + peak_1pEGb;
  disp_Q1EGt = peak_1qEGa + peak_1qEGb;
  disp_P3EGt = peak_3pEGa + peak_3pEGb;
  disp_Q3EGt = peak_3qEGa + peak_3qEGb;
  disp_P5EGt = peak_5pEGa + peak_5pEGb;
  disp_Q5EGt = peak_5qEGa + peak_5qEGb;

  counter = counter + 1;
  if(counter==200) //transmission 1x cycle
  {
    P1EGt  = disp_P1EGt;
    Q1EGt  = disp_Q1EGt;
    P3EGt  = disp_P3EGt;
    Q3EGt  = disp_Q3EGt;
    P5EGt  = disp_P5EGt;
    Q5EGt  = disp_Q5EGt;

    counter = 0;
  }
}

//#######################_END_Peak_Detection

samples++; //var_2_sweep_arrays

//#######################_Central_Controller
//Fundamental_In-Phase
DI = Imax;
a1p = (peak_1p + P1EGt - Io)/(DI); //Eq. 5.16 & 5.18 (dissertation): Io->
    active_current_ctrl
  if(a1p>=1)
  {
    a1p = 1;
  }
  else if(a1p<=(-1))
  {
    a1p = -1;
  }
//Fundamental_In-Quadrature
DI = I2max - (P1EGt)*(P1EGt);
if(DI>0.00)
{
  a1q = (peak_1q + Q1EGt)/sqrt(DI); //Eq. 5.17 & 5.19 (dissertation): grid + EGs + 0
     = I*
}
else
{
  a1q = 0.00;
}
  if(a1q>=1)
```

```
  {
    a1q = 1;
  }
  else if(a1q<=(-1))
  {
    a1q = -1;
  }
//3rd_In-Phase
DI = I2max - (P1EGt)*(P1EGt) - (Q1EGt)*(Q1EGt);
if(DI>0.00)
{
  a3p = (peak_3p + P3EGt)/sqrt(DI);
}
else
{
  a3p = 0.00;
}
  if(a3p>=1)
  {
    a3p = 1;
  }
  else if(a3p<=(-1))
  {
    a3p = -1;
  }
//3rd_In-Quadrature
DI = I2max - (P1EGt)*(P1EGt) - (Q1EGt)*(Q1EGt) - (P3EGt)*(P3EGt);
if(DI>0.00)
{
  a3q = (peak_3q + Q3EGt)/sqrt(DI);
}
else
{
  a3q = 0.00;
}
  if(a3q>=1)
  {
    a3q = 1;
  }
  else if(a3q<=(-1))
  {
    a3q = -1;
  }
//5th_In-Phase
DI = I2max - (P1EGt)*(P1EGt) - (Q1EGt)*(Q1EGt) - (P3EGt)*(P3EGt) - (Q3EGt)*(Q3EGt);
if(DI>0.00)
{
  a5p = (peak_5p + P5EGt)/sqrt(DI);
}
else
{
  a5p = 0.00;
}
  if(a5p>=1)
  {
    a5p = 1;
  }
```

```
  else if(a5p<=(-1))
  {
    a5p = -1;
  }
//5th_In-Quadrature
DI = I2max - (P1EGt)*(P1EGt) - (Q1EGt)*(Q1EGt) - (P3EGt)*(P3EGt) - (Q3EGt)*(Q3EGt) -
     (P5EGt)*(P5EGt);
if(DI>0.00)
{
  a5q = (peak_5q + Q5EGt)/sqrt(DI);
}
else
{
  a5q = 0.00;
}
  if(a5q>=1)
  {
    a5q = 1;
  }
  else if(a5q<=(-1))
  {
    a5q = -1;
  }

if(a1p>=1 || a1p<=-1)
{
  a1q = 0.00;
  a3p = 0.00;
  a3q = 0.00;
  a5p = 0.00;
  a5q = 0.00;
}

//Dispatch_Frequency
dispatch = dispatch + 1;
if(dispatch==200) //transmission 1x cycle
{
  disp_a1p = a1p;
  disp_a1q = a1q;
  disp_a3p = a3p;
  disp_a3q = a3q;
  disp_a5p = a5p;
  disp_a5q = a5q;

  dispatch = 0;
}
//#######################_END_Central_Controller

//#######################_EGs
//##########_EGa
//Fundamental In-Phase
DIa = Imaxa;
iP1EGa = (disp_a1p)*(DIa)*(pll2n_p);
//Fundamental_In-Quadrature
DIa = (Imaxa)*(Imaxa) - (peak_1pEGa)*(peak_1pEGa);
if(DIa>0.00)
{
```

```
  iQ1EGa = (disp_a1q)*(sqrt(DIa))*(pll2n_q);
}
else
{
  iQ1EGa = 0.00;
}
//3rd_In-Phase
DIa = (Imaxa)*(Imaxa) - (peak_1pEGa)*(peak_1pEGa) - (peak_1qEGa)*(peak_1qEGa);
if(DIa>0.00)
{
  iP3EGa = (disp_a3p)*(sqrt(DIa))*(pll2n_3p);
}
else
{
  iP3EGa = 0.00;
}
//3rd_In-Quadrature
DIa = (Imaxa)*(Imaxa) - (peak_1pEGa)*(peak_1pEGa) - (peak_1qEGa)*(peak_1qEGa) - (
    peak_3pEGa)*(peak_3pEGa);
if(DIa>0.00)
{
  iQ3EGa = (disp_a3q)*(sqrt(DIa))*(pll2n_3q);
}
else
{
  iQ3EGa = 0.00;
}
//5th_In-Phase
DIa = (Imaxa)*(Imaxa) - (peak_1pEGa)*(peak_1pEGa) - (peak_1qEGa)*(peak_1qEGa) - (
    peak_3pEGa)*(peak_3pEGa) - (peak_3qEGa)*(peak_3qEGa);
if(DIa>0.00)
{
  iP5EGa = (disp_a5p)*(sqrt(DIa))*(pll2n_5p);
}
else
{
  iP5EGa = 0.00;
}
//5th_In-Quadrature
DIa = (Imaxa)*(Imaxa) - (peak_1pEGa)*(peak_1pEGa) - (peak_1qEGa)*(peak_1qEGa) - (
    peak_3pEGa)*(peak_3pEGa) - (peak_3qEGa)*(peak_3qEGa) - (peak_5pEGa)*(peak_5pEGa)
    ;
if(DIa>0.00)
{
  iQ5EGa = (disp_a5q)*(sqrt(DIa))*(pll2n_5q);
}
else
{
  iQ5EGa = 0.00;
}

//##########_EGb
//Fundamental In-Phase
DIb = Imaxb;
iP1EGb = (disp_a1p)*(DIb)*(pll1n_p);
//Fundamental_In-Quadrature
DIb = (Imaxb)*(Imaxb) - (peak_1pEGb)*(peak_1pEGb);
```

```
if(DIb>0.00)
{
  iQ1EGb = (disp_a1q)*(sqrt(DIb))*(pll1n_q);
}
else
{
  iQ1EGb = 0.00;
}
//3rd_In-Phase
DIb = (Imaxb)*(Imaxb) - (peak_1pEGb)*(peak_1pEGb) - (peak_1qEGb)*(peak_1qEGb);
if(DIb>0.00)
{
  iP3EGb = (disp_a3p)*(sqrt(DIb))*(pll1n_3p);
}
else
{
  iP3EGb = 0.00;
}
//3rd_In-Quadrature
DIb = (Imaxb)*(Imaxb) - (peak_1pEGb)*(peak_1pEGb) - (peak_1qEGb)*(peak_1qEGb) - (
    peak_3pEGb)*(peak_3pEGb);
if(DIb>0.00)
{
  iQ3EGb = (disp_a3q)*(sqrt(DIb))*(pll1n_3q);
}
else
{
  iQ3EGb = 0.00;
}
//5th_In-Phase
DIb = (Imaxb)*(Imaxb) - (peak_1pEGb)*(peak_1pEGb) - (peak_1qEGb)*(peak_1qEGb) - (
    peak_3pEGb)*(peak_3pEGb) - (peak_3qEGb)*(peak_3qEGb);
if(DIb>0.00)
{
  iP5EGb = (disp_a5p)*(sqrt(DIb))*(pll1n_5p);
}
else
{
  iP5EGb = 0.00;
}
//5th_In-Quadrature
DIb = (Imaxb)*(Imaxb) - (peak_1pEGb)*(peak_1pEGb) - (peak_1qEGb)*(peak_1qEGb) - (
    peak_3pEGb)*(peak_3pEGb) - (peak_3qEGb)*(peak_3qEGb) - (peak_5pEGb)*(peak_5pEGb)
    ;
if(DIb>0.00)
{
  iQ5EGb = (disp_a5q)*(sqrt(DIb))*(pll1n_5q);
}
else
{
  iQ5EGb = 0.00;
}
//######################_END_EGs

//######################_InnerCurrentLoop
//if(count > 2400) //-> Simulation
if(count > 120000) //10 Secs to start relay -> DSP
```

```
{
  relay = 1;
  init  = 1;
  count = 120002;

  trip_cmd = 1;//trip OFF
}

if(init == 0)
{
  relay = 0;
  count = count + 1;
  Kramp = 0;
  trip_cmd = 0;//trip ON
}

if(relay == 1)
{
  //CBC Final Local Current References:
  //itotal_EGa = iP1EGa + iQ1EGa + iP3EGa + iQ3EGa + iP5EGa + iQ5EGa;
  //itotal_EGb = iP1EGb + iQ1EGb + iP3EGb + iQ3EGb + iP5EGb + iQ5EGb;
  //itotal_EGa = iP1EGa + iQ1EGa;
  //itotal_EGb = iP1EGb + iQ1EGb;
  itotal_EGa = iP1EGa + iQ1EGa + iP3EGa + iQ3EGa + iP5EGa + iQ5EGa;
  itotal_EGb = iP1EGb + iQ1EGb + iP3EGb + iQ3EGb + iP5EGb + iQ5EGb;

  //Ramp for current reference
  Kramp = Kramp + 2*0.000010416; //+- 4 sec ramp -> DSP
  //Kramp = Kramp + 0.00062500; //-> Simulation (4 cycles)
  if(Kramp>=1)
  {
    Kramp = 1;
  }

  errora = Kramp*itotal_EGa - inva;
  errorb = Kramp*itotal_EGb - invb;

  //Proportional Part - SPI1
  pia = errora*KPI;
  if (pia > 1)
    pia = 1;
  else if (pia < -1)
    pia = -1;
  if (pia > 0)
    limit_ia = 1 - pia;
  else
    limit_ia = 1 + pia;

  //Proportional Part - SPI2
  pib = errorb*KPI;
  if (pib > 1)
    pib = 1;
  else if (pib < -1)
    pib = -1;
  if (pib > 0)
    limit_ib = 1 - pib;
  else
```

```
  limit_ib = 1 + pib;

//Ressonant Part - SPI1
errora2 = errora1;
errora1 = errora0;
errora0 = errora;

//Ressonant Part - SPI2
errorb2 = errorb1;
errorb1 = errorb0;
errorb0 = errorb;

for(i=0; i<4; i++)
{
  //Ressonant Part - SPI1
  pres_2a[i] = pres_1a[i];
  pres_1a[i] = presa[i];
  presa[i] = a[i]*errora -a[i]*errora2 + b[i]*pres_1a[i] - pres_2a[i];

  if(presa[i] > limit_ia)
    presa[i] = limit_ia;
  else if (presa[i] < -limit_ia)
  presa[i] = -limit_ia;

  //Ressonant Part - SPI2
  pres_2b[i] = pres_1b[i];
  pres_1b[i] = presb[i];
  presb[i] = a[i]*errorb -a[i]*errorb2 + b[i]*pres_1b[i] - pres_2b[i];

  if(presb[i] > limit_ib)
    presb[i] = limit_ib;
  else if (presb[i] < -limit_ib)
  presb[i] = -limit_ib;
}
pres_ia = pia;
pres_ib = pib;

//P+Resonant Result
for(i=0; i<4; i++)
{
  pres_ia = pres_ia + presa[i];
  pres_ib = pres_ib + presb[i];
}

//PWM Ctrl - SPI1
taa = pres_ia; //modulation_2_PWM
if (taa > 1)
{
  taa = 1;
}
else if (taa < -1)
{
  taa = -1;
}

//PWM Ctrl - SPI2
tbb = pres_ib;
```

```
  if (tbb > 1)
  {
    tbb = 1;
  }
  else if (tbb < -1)
  {
    tbb = -1;
  }
}

if(inva_filter >=1 || inva_filter <=-1 || invb_filter >=1 || invb_filter <=-1)
{
  trip_cmd = 0;//trip ON
  relay = 0;
}
//########################_END_InnerCurrentLoop

//_______________OUTPUTS
y1 = relay;
y2 = trip_cmd;
y3 = taa;
y4 = tbb;
```