Low-Frequency Noise Assessment of Different Ge pFinFET STI Processes

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***Abstract*— An experimental low-frequency noise (LFN) assessment of long channel Ge pFinFET devices fabricated in different shallow trench isolation (STI) processes is presented, taking into consideration devices with fin widths from 100 nm (planar-like) down to 20 nm. In addition, the correlation among LFN parameters, hole mobility and threshold voltage, is also evaluated. The carrier number fluctuation (ΔN) model is confirmed as dominant mechanism for all studied Ge pFinFETs and there is no correlation with the used STI process. From the LFN, it is evidenced that the Coulomb scattering mobility mechanism plays an important role for STI-first process, resulting in a mobility degradation.**

***Index Terms*— Ge pFinFET, low-frequency noise (LFN), shallow trench isolation (STI) first, STI last.**

I. Introduction

THE combination of germanium as a channel material, because of its superior hole mobility compared with silicon [1], and multiple gate structures, such as FinFETs, which present greater electrostatic coupling and better short channel effects compared with planar devices [2], [3], has been pointed out as a promising device approach for high performance applications.

The high mobility materials, such as Ge and III–V [4], have been extensively investigated, motivated by the mobility degradation when high-κ dielectrics compose the gate-stack [5]. However, in order to enable industrial manufacturing, the Si-platform integration must be taken into consideration for future devices. However, heteroepitaxy on a Si substrate may be prone to extensive defect generation, mainly misfit dislocation and threading dislocation (TD) [6], since there is a mismatch in lattice parameter and coefficient of thermal expansion between Si and Ge [7]. Moreover, the TD density is a key parameter to be reduced, since it strongly affects the device performance [8], [9].

In order to keep the TD density as low as possible, different techniques have been evaluated to grow a Ge layer, which can be either on top of a Si–Ge strain relaxed buffer (SRB) [10] or directly on silicon [11]. The first process fabricates SRB layers in predefined shallow trench isolation (STI) region (referred to as STI-first) [12], where the SRB layer must be thick enough, i.e., with an aspect ratio higher than 3, so that most of the TDs are trapped in the bottom part of the layer [13]. In another approach, a thick SRB layer ($\sim$1 μm) is grown on a Si wafer, followed by a thin Ge layer on the SRB, which can achieve a TD density in the SRB around 10^6 cm^{-2} [14]. Subsequently, the fin is defined by an STI process, which in this case is called STI-last. A modified option is the growth of a thick Ge layer on the Si substrate, followed by a chemical mechanical polishing. The fin is also defined by the STI-last process [11]. It is worth mentioning that the growth of a thin Ge layer on the SRB results in a compressive stress, which can have a beneficial impact on the p-channel device performance [15].

Low-frequency noise (LFN) measurement has been systematically used in this paper, which is one important, powerful and nondestructive technique that allows evaluating in detail the gate dielectric and device channel quality [16].

This paper has the following sequence: Section II starts with the device characteristics, where the main dimensions and process data are presented. Section III describes how the LFN analysis has been done. Section IV shows both LFN parameters, hole mobility and threshold voltage behaviors, as a function of the fin width. Section V concludes with the correlation among the main studied parameters from Section IV in order to evaluate and identify the parameters that contribute to the hole mobility and the threshold voltage degradations.

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TABLE I
DEVICE DIMENSIONS FOR THE DIFFERENT STI PROCESSES

	STI first strained	STI last strained using SRB/Si	STI last relaxed using Ge/Si
W_{fin} (nm)		20 to 100 (planar-like)	
L_G (nm)		330 to 1,000	
H_{fin} (nm)	20	30	30
N		4	
$Si_{1-x}Ge_x$	75	70	N.A.
Gate stack composition		Ge/Si-cap/HfO_2/TiN/W	

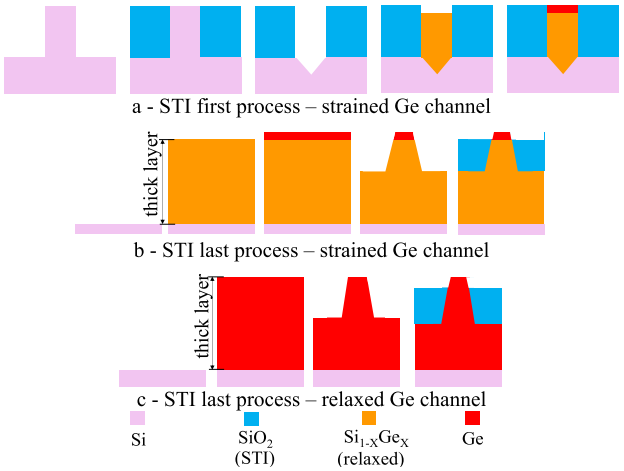

Fig. 1. Schematic of the three different processes. (a) STI first strained device. (b) and (c) STI last strained and relaxed devices.

II. DEVICE CHARACTERISTICS

The p-type Ge FinFETs for all evaluated STI processes have been fabricated at imec/Belgium on 300-mm Si (100) substrates. The device dimensions, such as fin width (W_{fin}), geometric channel length (L_G), fin height (H_{fin}), number of fins in parallel (N), gate-stack composition, and the Ge amount in the n-type *in situ* doped relaxed buffers, are presented in Table I. Moreover, the region underneath the channel has an n-type doping concentration around 5×10^{18} cm^{-3}. The processing details regarding the germanium layer growth for the three considered scenarios, i.e., STI last-strained, STI first-strained, and STI last-relaxed, can be found in [10]–[12], respectively, where Fig. 1 shows the main difference among them.

III. METHODOLOGY

This paper is based on extensive experimental data, where the LFN characterization has been performed in the linear operation regime, while the gate bias (V_{GS}) was stepped from weak to strong inversion from the hardware/software systems from ProPlusSolution. It is worth mentioning that the input-referred voltage noise spectral density (S_{VG}) was determined from the ratio of the drain current noise spectral density over the square of the transconductance (S_{ID}/gm^2). Regarding the input characteristic curves, the same operation regime has been used and obtained by an HP 4146C-Semiconductor Device Parameter Analyzer. The hole mobility and threshold voltage

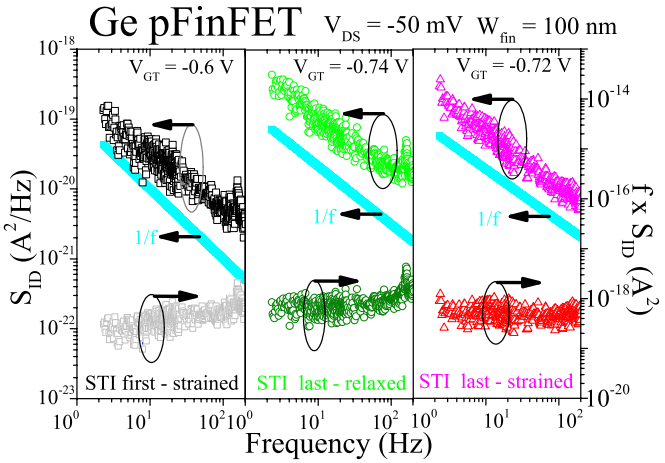

Fig. 2. LFN spectral density (S_{ID}) and $f \times S_{ID}$ as a function of frequency in linear operation corresponding with planar-like ($W_{fin} = 100$ nm) devices for different STI processes.

were extracted by the y-function [17] and second derivative peak [18] methods, respectively.

The LFN is composed of three components as in (1), i.e., white noise, $1/f^{\gamma}$ (flicker-noise), and the sum of Lorentzian components (generation–recombination: GR-noise) [19]. The first component is found in all spectra, on the other hand, it is negligible compared with other ones at frequencies below 10 kHz

$$S_{VG}(f) = B_W + \frac{K_f}{f^{\gamma}} + \sum_{i=0}^{N} \frac{A_i}{1 + \left(\frac{f}{f_{0i}}\right)^2} \tag{1}$$

where B_W is related to the white noise level, k_f/f^{γ} presents the flicker noise, and A_i and f_{0i} are the plateau value and characteristic frequency, respectively, of the different Lorentzian components.

The power spectral densities (S_{ID}) in Fig. 2 clearly show that the $1/f^{\gamma}$ component is dominant for all STI processes. On top of that, the humps presented in S_{ID} indicate the presence of a GR-noise component, which gives insights where the traps are located: either into the gate dielectric or into the channel region [20]. The GR-noise has been reported in detail in [21] taking into consideration both studied STI processes. Apart from that, the plateau behavior in the $f \times S_{ID}$ plots in Fig. 2 indicates that the γ factor is close to one for all studied processes.

The $1/f^{\gamma}$ can be influenced by two different mechanisms: carrier number fluctuation (ΔN) or mobility fluctuation ($\Delta \mu$) or a correlation of both of them [22]. The dominant mechanism can be easily identified by checking whether there is a parallelism between the normalized power spectral density (S_{ID}/I_{DS}^2) and the squared transconductance over drain current ratio $(gm/I_{DS})^2$ as a function of drain current [23]. If this is confirmed, the ΔN is strongly predominant, otherwise $\Delta\mu$ fluctuations or an additional effect determine the $1/f^{\gamma}$ noise.

Fig. 3 confirms the predominance of ΔN for the studied devices, similar as in Ge planar devices with different passivation layers [24], [25].

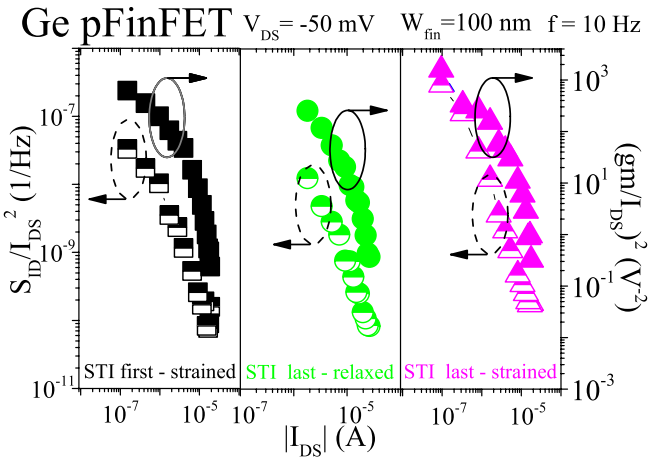

Fig. 3. Normalized drain current noise spectral density and $(\mathrm{gm}/I_{\mathrm{DS}})^2$ as a function of absolute drain current in linear operation for planar-like ($W_{\mathrm{fin}} = 100$ nm) devices and different STI processes.

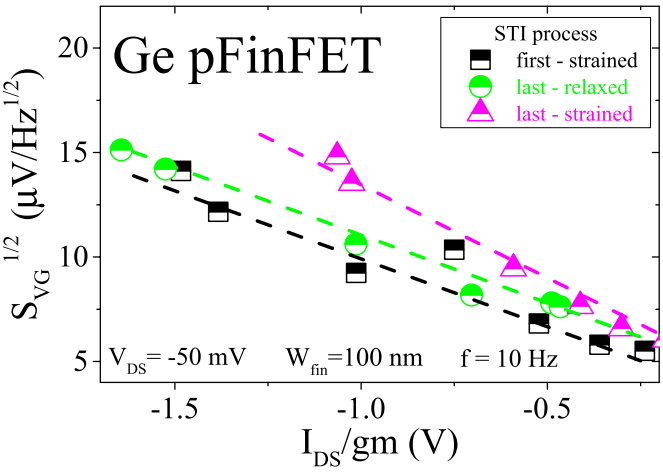

Fig. 4. Square root input-referred voltage noise spectral density in linear operation and $f = 10$ Hz as a function of drain current over transconductance ratio for planar-like ($W_{\mathrm{fin}} = 100$ nm) devices and different STI processes.

Moreover, since ΔN is dominant, it allows the extraction of important parameters, such as Coulomb scattering coefficient (α_{sc}), input-referred voltage noise at flat-band (S_{VGfb}), and oxide trap density (N_{OT}). The latter is determined by the following:

$$S_{\mathrm{VGfb}} = \frac{q^2 k_B \mathrm{T} N_{\mathrm{OT}}}{W_{\mathrm{eff}} L_G \alpha_t C_{\mathrm{OX}}^2 f} \tag{2}$$

where q is the elementary charge, $k_B T$ is the thermal energy, W_{eff} is the effective width, L_G is the geometric channel length, f is the frequency, α_t is the attenuation tunneling parameter noise taken as 1×10^8 cm^{-1}, and C_{OX} is the capacitance density.

In order to extract N_{OT}, both α_{sc} and S_{VGfb} values must be known and can be obtained from (3). By plotting this equation as done in Fig. 4, α_{sc} and S_{VGfb} are determined from the intercept and slope of the curves. By assuming an energy interval of 4 $k_B T$, N_{OT} (eV^{-1}cm^{-3}) can be converted into surface density (D_{OT}) [26], considering a thickness of the trapping–detrapping layer of 2 nm

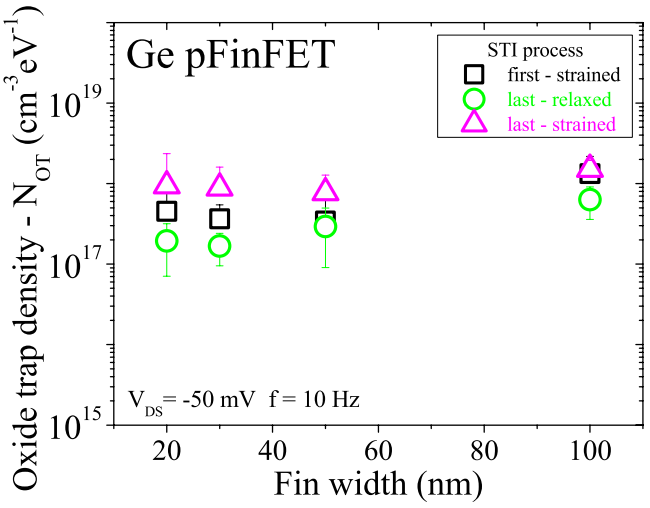

Fig. 5. Oxide trap density as a function of fin width for different STI processes.

$$S_{\mathrm{VG}} = S_{\mathrm{VGfb}} \left(1 + \alpha_{\mathrm{SC}} \mu C_{\mathrm{OX}} \frac{I_{\mathrm{DS}}}{\mathrm{gm}}\right)^2 \tag{3}$$

where S_{VG} is the input-referred voltage noise spectral density and μ is the mobility.

The Coulomb scattering (α_{SC}) can also be extracted from the linear dependence of the inverse mobility ($1/\mu$) with D_{OT}, as shown in [27]

$$\frac{1}{\mu} = \frac{1}{\mu_0} + q D_{\mathrm{OT}} \alpha_{\mathrm{SC}} \tag{4}$$

where μ_0 represents the mobility limited by other scattering mechanisms apart from the Coulomb scattering of the oxide.

IV. Results

Fig. 5 shows the oxide trap density (N_{OT}) and reveals that for Ge FinFETs, the N_{OT} level is around $10^{17} \sim 10^{18}$ cm^{-3}eV^{-1}, which is lower than for planar Ge MOSFET devices, which is around 5×10^{18} cm^{-3}eV$^{-1} \sim 3 \times 10^{19}$ cm^{-3}eV^{-1} [25], [27] and similar to values for Si FinFETs with a similar gate-stack [28]–[30].

Fig. 6 presents the hole mobility (μ_h) for different fin widths, and in STI last strained devices, no noticeable W_{fin} dependence is observed. On the other hand, the other STI processes show a hole mobility increase, when the fin width reduces, because of the strong sidewall contribution, since the low-field hole mobility of the FinFET on the top ⟨100⟩ plane is inferior over the value for ⟨110⟩ sidewalls [31]. It is also clear in Fig. 6 that for the STI first strained devices, the compressive stress has only a marginal impact on the hole mobility, while there is a clear improvement for the STI last strained counterparts. As shown in the following, this is related with a more pronounced impact of Coulomb scattering in the former case.

Fig. 7 presents the Coulomb scattering coefficient (α_{SC}) and clearly shows the one order of magnitude higher value for STI first compared with both STI last processes, which might play

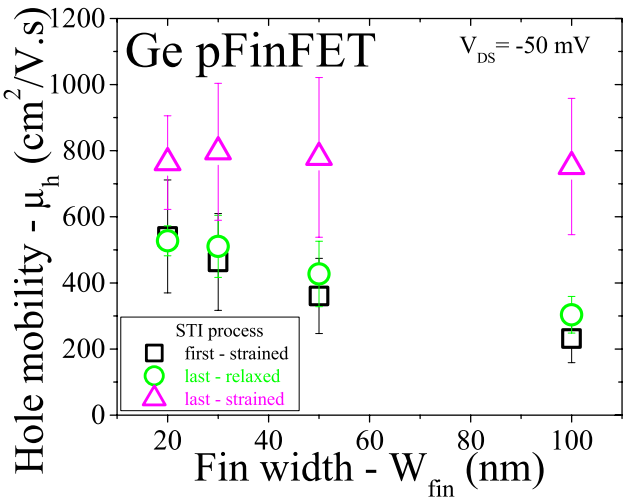

Fig. 6. Hole mobility as a function of fin width for different STI processes.

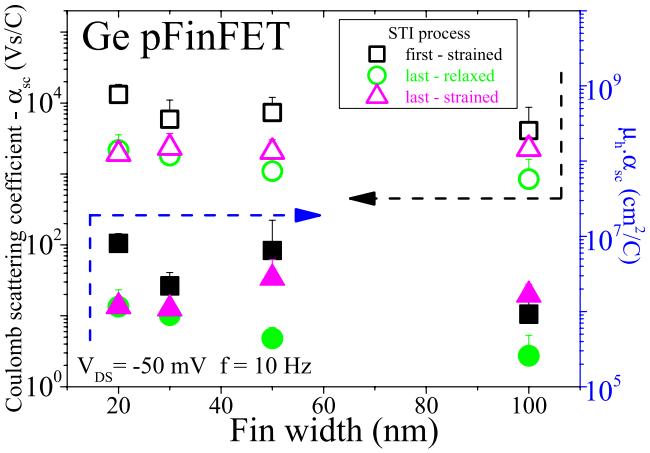

Fig. 7. Coulomb scattering coefficient as a function of fin width for different STI processes.

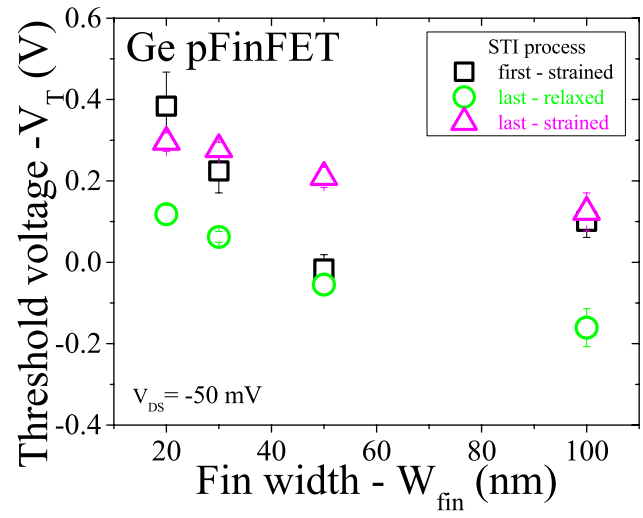

Fig. 8. Threshold voltage as a function of fin width for different STI processes.

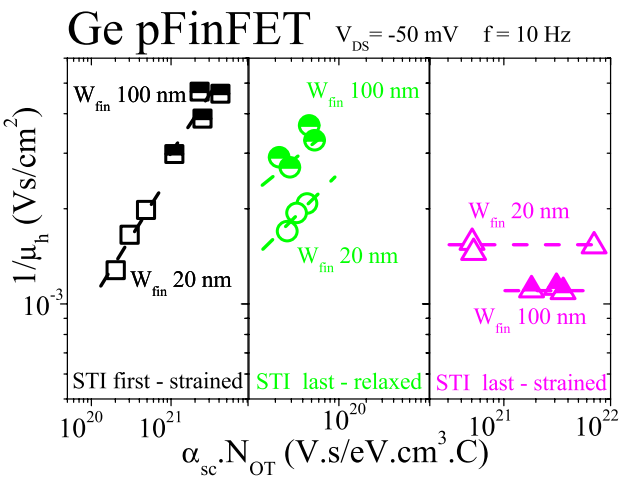

Fig. 9. Inverse hole mobility as a function of scattering coefficient times oxide trap density for different STI processes.

a role in the device performance, due to its impact on the hole mobility. The obtained values are similar to those for Ge pMOSFETs, which is between $10^3 \sim 10^4$ Vs/C [25], [27]. Moreover, a slight fin width (W_{fin}) dependence is found, except for the STI last strained process where there is no correlation between α_{SC} and W_{fin} and its α_{SC} value is around 2×10^3 Vs/C.

A higher scattering coefficient indicates more efficient scattering by charged traps, which are on the average closer to the channel. It implies that the charge centers in the STI first case are closer to the inversion layer, either in the gate-stack or perhaps, more directly in the Ge fin. From the product of μ_h and α_{SC}, which is presented in a secondary y-axis in Fig. 7, one can derive that the STI first approach experiences the strongest effect of the Coulomb scattering by charged oxide traps, probed by the 1/f noise PSD.

Fig. 8 shows the influence of fin width on the threshold voltage (V_T), where there is both a W_{fin}-dependence and strain effect. The latter results in a V_T difference between strain and relaxed devices (ΔV_T) of about 0.3 V, as a consequence of the Ge valence band (E_V) shifting when compressive strain is applied in p-channel Ge devices, i.e., there is a Ge bandgap reduction [32]. The W_{fin}-dependence might be associated with the doping concentration that can be inferior to narrow devices compared with planar-like ones.

V. Discussion

Fig. 9 uses the product of the Coulomb scattering coefficient and oxide trap density to evaluate their influence on the hole mobility (μ_h).

The more pronounced μ_h degradation is found for STI first strained narrow and planar-like devices, indicating that the Coulomb scattering mechanism might be dominant. The STI last relaxed devices also present μ_h degradation, however, less prominent than for the STI first ones. On the other hand, μ_h shows no clear correlation with α_{SC} times N_{OT} for the STI last strained process.

Fig. 10 presents the impact of the oxide trap density on the threshold voltage. There is a slight variation of the V_T value for STI last strained narrow devices, resulting in a lower V_T value compared with STI first devices, as presented in Fig. 8 (W_{fin} of 20 nm). For both STI first and last processes, strained

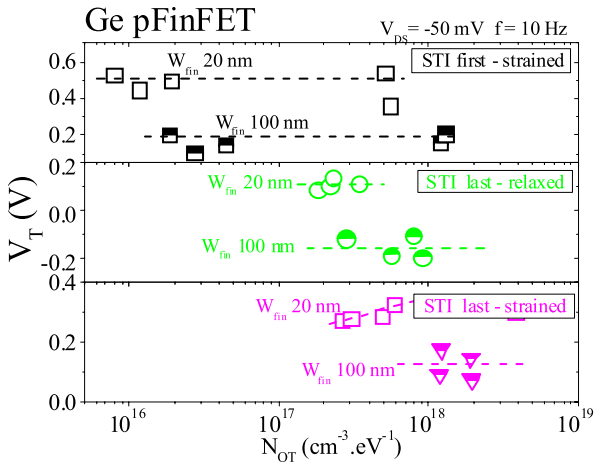

Fig. 10. Threshold voltage as a function of oxide trap density for different STI processes and two fin widths.

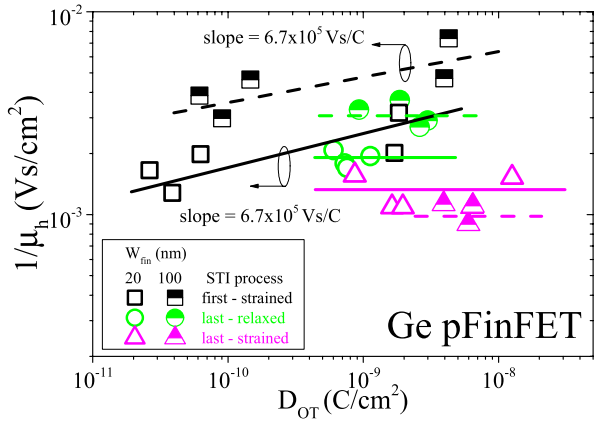

Fig. 11. Inverse hole mobility as a function of surface trap charge density for different STI processes.

and relaxed, there is no clear correlation that might affect the V_T behavior.

Fig. 11 presents the inverse hole mobility as a function of surface trap charge density. Despite the fact that the Coulomb scattering coefficient obtained from Fig. 11 (6.7×10^5 Vs/C) is about one order of magnitude higher than the ones from Fig. 7 (STI first process). It gives further support to the predominance of the Coulomb scattering mechanism independent of the fin width only for the STI first process, which has also been demonstrated by low-temperature split-CV measurements [33]. It might be associated with fixed charges into the gate-stack layer [34].

The latter presents thinner and thicker layers of SiO_2 and HfO_2, respectively, for STI first process compared with the STI last ones, indicating that thicker high-k layer might contribute to the predominance of the Coulomb scattering mechanisms. This is supported by the higher α_{SC} values in Fig. 7. A thinner interfacial SiO_2 layer brings the charged traps in the HfO_2 closer to the channel, resulting in more efficient Coulomb scattering.

VI. Conclusion

For the studied Ge pFinFETs, the dominant noise mechanism, independent of the used STI process, is number fluctuations. Furthermore, the STI last processes demonstrate to be less affected by the Coulomb scattering, at least for strained devices. In contrast, the Coulomb scattering mechanism plays an important role for STI first strained devices, resulting in a degradation of the hole mobility. The strain effect has only a pronounced impact on the threshold voltage and not on the hole mobility, indicating that there are other mechanisms playing a role. Finally, the oxide trap density can degrade the device V_T, although the STI first-strained and last-relaxed approaches show no significant correlation between these parameters.

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