The Influence of Oxide Thickness and Indium Amount on the Analog Parameters of $In_xGa_{1-x}As$ nTFETs

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***Abstract*— The basic analog parameters of three splits of $In_xGa_{1-x}As$ nTFETs are analyzed for the first time. The first two splits are $In_{0.53}Ga_{0.47}As$ devices with a 3-nm HfO_2/1-nm Al_2O_3 and a 2-nm HfO_2/1-nm Al_2O_3, while the last one is an $In_{0.7}Ga_{0.3}As$ channel with a 3-nm HfO_2/1-nm Al_2O_3 gate. The low equivalent oxide thickness improves the electrostatic coupling, enhancing I_{DS}, and, consequently, also gm and A_V, especially for higher V_{GS}. The InGaAs tunnel field-effect transistors (TFETs) show compatible performance with Si TFETs, and have better performance than Si MOSFETs, making them useful for low-power and low-voltage analog applications. The highest efficiency is found using the combination of a 2-nm HfO_2 with $In_{0.53}Ga_{0.47}As$, due to the 56-mV/dec subthreshold swing obtained. For all splits, the A_V peak can be related to the V_{GS} necessary for band-to-band tunneling to become the dominant transport mechanism.**

***Index Terms*— Analog parameters, current conduction mechanisms, intrinsic voltage gain, sub-60 mV/dec, tunnel field-effect transistors (TFET).**

I. Introduction

TUNNEL field-effect transistors (TFETs) are a relatively new type of transistors that uses the band-to-band tunneling (BTBT), where its structure is a gated p-i-n diode [1]. The TFETs were designed for logic applications because of their capability to overcome the theoretical limit of the subthreshold swing (SS) of conventional MOSFETs (60 mV/dec at room temperature) [2]–[4], leading to a reduction of the power consumption. TFETs with sub-60 mV/dec SS have already been demonstrated in [5].

However, Si TFETs present very low ON-state current (I_{ON}) due to its high bandgap (1.1 eV). Different semiconductor materials with the lower bandgap can be used to increase I_{ON}. Ge compounds [6]–[9] and III–V materials [10]–[14] are examples with the lower bandgap that can be used to obtain higher I_{ON}. The TFET design proposed in [10] is a vertical $In_{0.53}Ga_{0.47}As$ device approach using the same material layer structure as for the horizontal devices studied in this paper.

Besides excellent potential for logic applications due to their improved switching characteristics (SS $<$ 60 mV/dec), TFETs are also promising for analog applications, as reported in [15]–[23], where in [20] and [22], a comparison between TFETs and MOSFETs has shown better analog performance of TFETs. Some basic analog circuits have also been studied, not only presenting promising characteristics but also limitations [24]–[27], showing that the differential and common mode gains for the TFET differential pair were around 1–2 higher times than that for FinFETs [25], with the TFET differential pairs being also less influenced by the temperature [26].

The focus of this paper is the study of the influence of the indium amount and the HfO_2 thickness on the analog parameters of $In_xGa_{1-x}As$ nTFETs with the Zn source diffusion from the gas phase. For these analyses, three different splits are considered, the first is $In_{0.53}Ga_{0.47}As$ with a 3 nm of HfO_2, the second is $In_{0.53}Ga_{0.47}As$ with a 2 nm of HfO_2, and the last is $In_{0.7}Ga_{0.3}As$ with a 3 nm of HfO_2.

II. Device Characteristics

The studied devices are n-type $In_xGa_{1-x}As$ homojunction TFETs fabricated by using the Zn gas phase diffusion. The device follows the approach introduced by the University of Tokyo [11], [28], and further optimized in [29] using the solid-source diffusion and in [30] using the gas phase Zn diffusion. A schematic representation of the fabricated $In_xGa_{1-x}As$ nTFETs is presented in Fig. 1.

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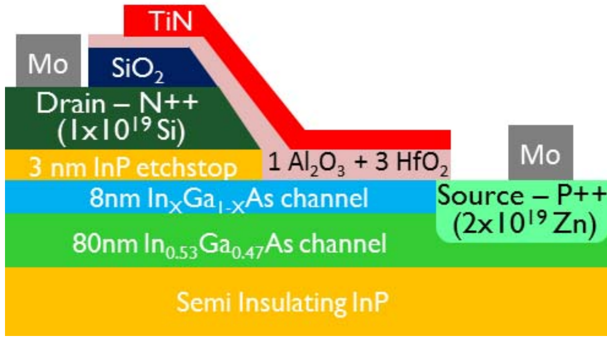

Fig. 1. Schematic representation of the $In_XGa_{1-X}As$ nTFET used.

Three different splits were analyzed, two splits with a uniform $In_{0.53}Ga_{0.47}As$ channel and the other one has an extra 8-nm $In_{0.7}Ga_{0.3}As$ layer on top of the $In_{0.53}Ga_{0.47}As$ channel, as can be observed in Fig. 1. The $In_{0.7}Ga_{0.3}As$ and one of the $In_{0.53}Ga_{0.47}As$ devices have a 3-nm HfO_2 on the top of 1-nm Al_2O_3, resulting in an equivalent oxide thickness (EOT) of about 1 nm. The last $In_{0.53}Ga_{0.47}As$ device has a 2-nm HfO_2 on the top of a 1-nm Al_2O_3, resulting in an EOT of about 0.8 nm. The gate-stack uses TiN as the metal gate. The drain is doped with Si (N++), and the P++ source is doped with Zn using the gas phase diffusion [30]. The width is about 400 μm and the gate length is about 5 μm. More processing details can be found in [30].

III. Analysis and Results

Fig. 2 presents the drain current (I_{DS}) as a function of the gate voltage (V_{GS}) for the three different splits with the drain voltage (V_{DS}) biased at 0.6 and 1 V (A), and biased at 0.05 and 0.2 V (B). One can observe that I_{ON} is higher for the $In_{0.7}Ga_{0.3}As$ nTFET because of its lower bandgap (E_g) (E_g, $In_{0.53}Ga_{0.47}As$ = 0.752 eV and E_g, $In_{0.7}Ga_{0.3}As$ = 0.588 eV [31]). Also, the reduction of the onset voltage (V_{ON}) contributes to the increase of I_{ON}. Considering the effect of the reduction of the EOT, from 3 to 2 nm of HfO_2 in the $In_{0.53}Ga_{0.47}As$ split, the I_{ON} increases slightly due to the better electrostatic control, improving also the subthreshold characteristics, reaching sub-60 mV/dec values. In Fig. 2, it is also possible to observe that I_{DS} enhances when V_{GS} increases. This enhancement is caused by the reduction of the tunneling length, which raises the BTBT generation rate, resulting in an increase of I_{DS}. Not only the I_{DS} is increased when enhancing the BTBT generation but also the hysteresis is improved (reduced), being lower for the $In_{0.7}Ga_{0.3}As$ device with high I_{DS} resulting in the hysteresis of 14 mV. The $In_{0.53}Ga_{0.47}As$ device with a 2 nm of HfO_2 is the second best (16 mV). The $In_{0.53}Ga_{0.47}As$ device with a 3 nm HfO_2 is less influenced by BTBT and presents the highest hysteresis (25 mV).

The transconductance (gm), which is given in Fig. 3, presents the same tendency as I_{DS}, showing the higher gm for the $In_{0.7}Ga_{0.3}As$, the lower gm for the $In_{0.53}Ga_{0.47}As$ channel with a 2 nm of HfO_2, and also an increase with V_{GS}.

Fig. 4 presents the output conductance (g_D) as a function of V_{GS} for all the three analyzed splits. As V_{GS} becomes higher, g_D increases (degrades) due to the higher V_{DS} dependence of the effective energy window of overlap at the source-channel junction for higher V_{GS} [32]. This energy window, where BTBT occurs, is the region limited by the valence band of the source, the conduction band of the channel and the drain, and also the Fermi levels. As V_{DS} is increased, this energy

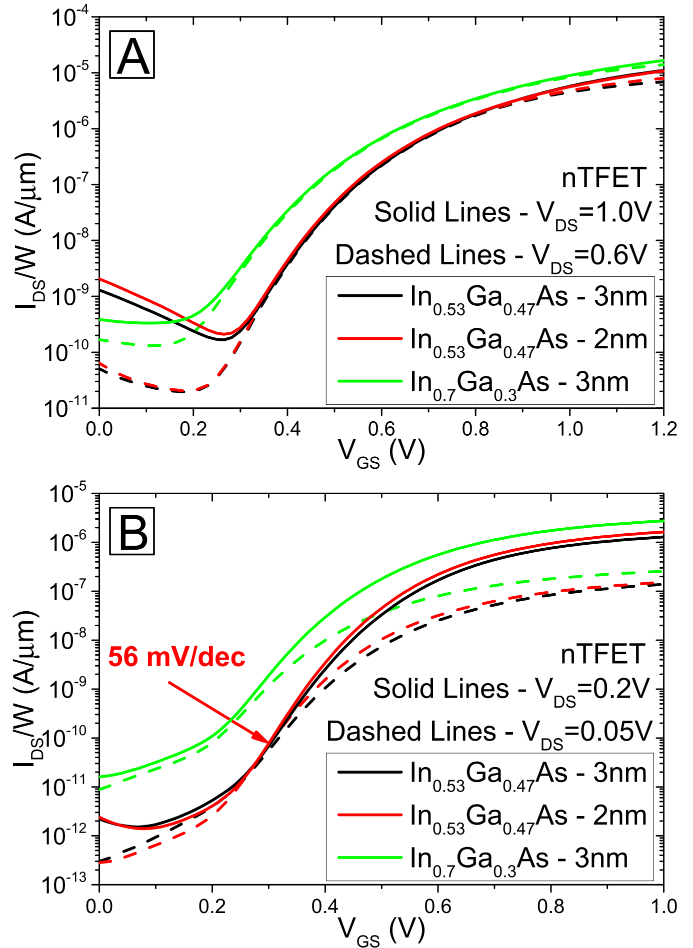

Fig. 2. Experimentally normalized I_{DS} as a function of V_{GS} for $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ (both EOTs) nTFETs. (A) With V_{DS} of 0.6 and 1 V. (B) With V_{DS} of 0.05 and 0.2 V.

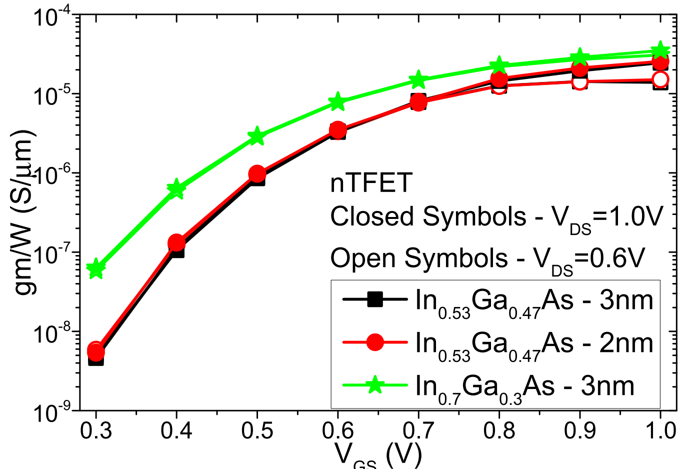

Fig. 3. Experimentally normalized gm as a function of V_{GS} for $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ (both EOTs) nTFETs, with V_{DS} of 0.6 and 1 V.

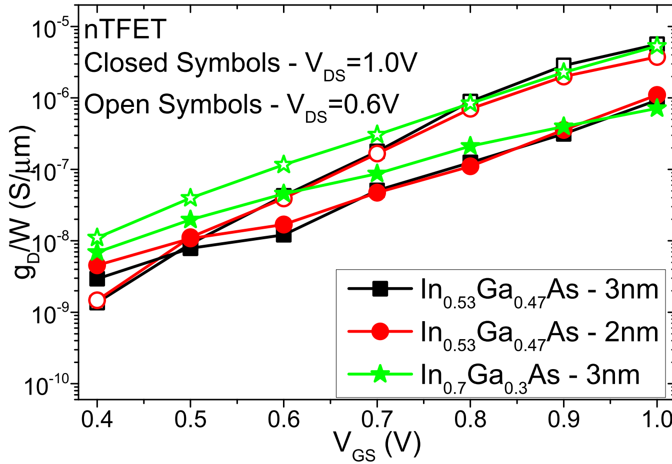

Fig. 4. Experimentally normalized g_D as a function of V_{GS} for $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ (both EOTs) nTFETs, with V_{DS} of 0.6 and 1 V.

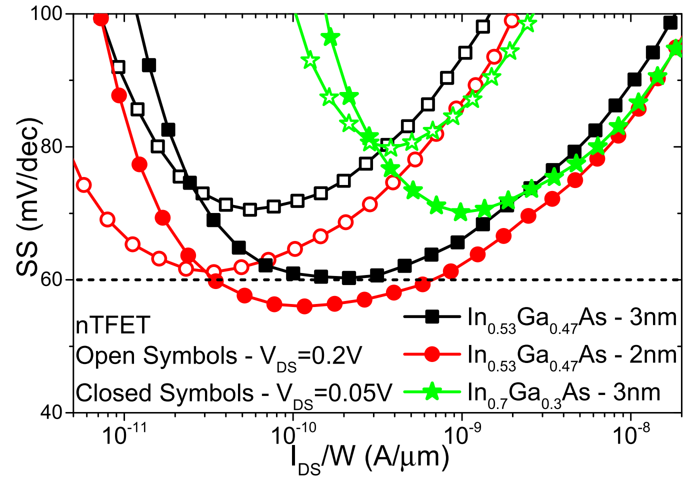

Fig. 6. Experimental SS as a function of normalized I_{DS} for $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ (both EOTs) nTFETs, with V_{DS} of 0.05 and 0.2 V.

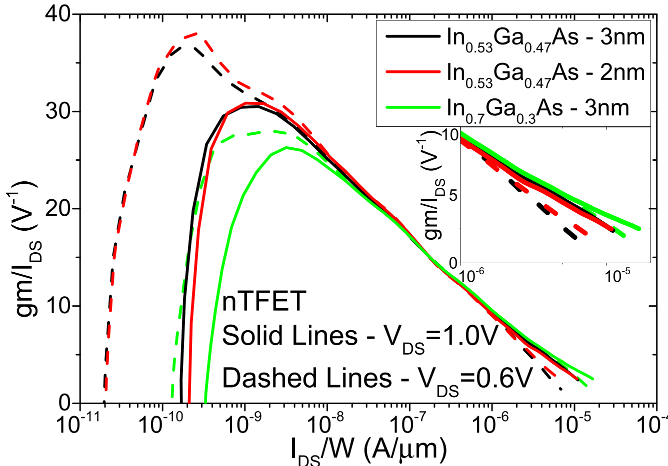

Fig. 5. Experimental gm/I_{DS} as a function of normalized I_{DS} for $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ (both EOTs) nTFETs, with V_{DS} of 0.6 and 1 V.

window becomes wider, reducing the influence of the drain and improving (decreasing) g_D. This improvement can also be observed in the I_{DS} and gm curves, where for high V_{GS}, both quantities increase with V_{DS}. Analyzing the influence of the percentage of indium, it is possible to observe different behaviors for the splits. The $In_{0.7}Ga_{0.3}As$ split presents higher g_D values than the $In_{0.53}Ga_{0.47}As$ splits at low V_{GS} ($V_{GS} \approx$ 0.5 V); however, for high V_{GS} values, they present similar values.

Another important figure of merit for the analog performance is the transistor efficiency (gm/I_{DS}), where it is possible to study the transistor performance from weak to strong conduction regime (Fig. 5). In the strong conduction regime, the dominant parameter is the gm. In this regime, all the samples present similar behavior at $V_{DS} = 1$ V, due to their similar gm at the same I_{DS}. However, at $V_{DS} = 0.6$ V, the $In_{0.7}Ga_{0.3}As$ presented a slightly better efficiency compared with $In_{0.53}Ga_{0.47}As$ samples.

In the weak conduction regime (peak region), the efficiency is inversely related to the SS of the devices. The SS as a function of the normalized I_{DS} is presented in Fig. 6. In the efficiency curve, at weak conduction regime, it is noticeable that the $In_{0.53}Ga_{0.47}As$ with a 2 nm of HfO_2 yields the best efficiency. This high efficiency is related to its sub-60 mV/dec behavior, as shown in Fig. 6, where the $In_{0.53}Ga_{0.47}As$ presents the best efficiency characteristics at weak conduction regime. Although the $In_{0.7}Ga_{0.3}As$ sample demonstrates satisfactory results at the strong conduction regime, at the weak conduction regime, it exhibits a degraded efficiency, worse than both $In_{0.53}Ga_{0.47}As$ samples. This degradation is related to its high OFF-state current (I_{OFF}), as can be observed in Fig. 2(B), showing I_{DS} for the low V_{DS} polarization.

Fig. 7 presents the I_{DS} as a function of V_{DS}, presenting the output characteristics of the studied devices. The early voltage (V_{EA}) is another important analog parameter that relates the output characteristics with the drain current (Fig. 8). The V_{EA} can be extracted by the intercept value with the V_{DS} axis ($I_{DS} = 0$) obtained by a linear extrapolation of the I_{DS} as a function of V_{DS}.

One can observe that for $V_{DS} = 1$ V, V_{EA} presents higher values than for $V_{DS} = 0.6$ V, a behavior that is due to the higher I_{DS} current. Moreover, for higher V_{DS}, the device operates more in a saturation-like region; that is, it has less drain dependence, resulting in a higher V_{EA}.

For low V_{GS}, V_{EA} is also low because it is dominated by the low I_{DS}. As the V_{GS} is increased, the current is enhanced, causing an improvement in V_{EA}. However, increasing even more V_{GS}, besides increasing I_{DS}, the drain dependence also increases (g_D degradation), resulting in a reduction of V_{EA} for high V_{GS} values.

The $In_{0.7}Ga_{0.3}As$ device presents higher V_{EA} due to its higher I_{DS} and g_D, especially for low V_{GS} and V_{DS} above 0.8 V. At low V_{GS} bias, the output characteristic presents an anomalous behavior in the saturation-like region, as can be observed in Fig. 7. In this case, for high drain bias, the TFET works like a diode, tunneling at the channel or drain junction, increasing the drain influence in I_{DS}, and resulting in a degradation of V_{EA}. The $In_{0.53}Ga_{0.47}As$ device is more

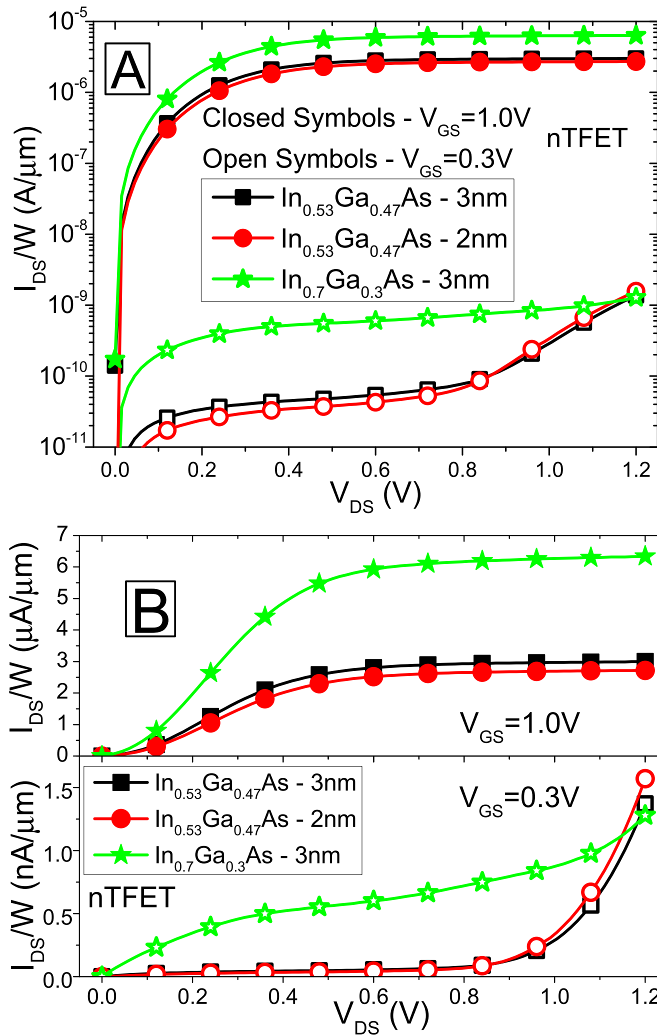

Fig. 7. Experimentally normalized I_{DS} as a function of V_{DS} for $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ (both EOTs) nTFETs, with V_{GS} of 0.3 and 1 V in (A) logarithmic and (B) linear scales.

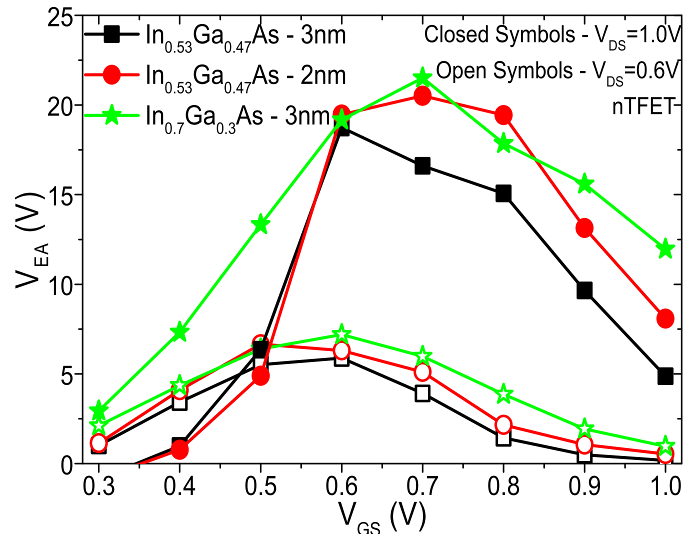

Fig. 8. Experimental V_{EA} as a function of V_{GS} for $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ (both EOTs) nTFETs, with V_{DS} of 0.6 and 1 V.

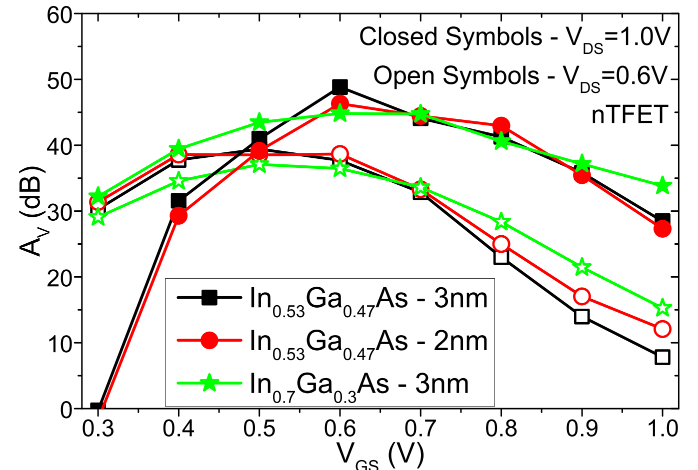

Fig. 9. Experimental A_V as a function of V_{GS} for $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ (both EOTs) nTFETs, with V_{DS} of 0.6 and 1 V.

susceptible to this diode behavior than the $In_{0.7}Ga_{0.3}As$ device due to the lower V_{ON} of the last one.

One of the most important figures of merit for analog performance is the intrinsic voltage gain (A_V), shown in Fig. 9. This parameter can be calculated by the gm and g_D ratio, or using V_{EA} and the transistor efficiency, as can be seen in the following:

$$A_V = 20 \cdot \log\left(\left|\frac{\text{gm}}{g_D}\right|\right) = 20 \cdot \log\left(V_{EA} \cdot \frac{\text{gm}}{I_{DS}}\right). \quad (1)$$

One can observe that there are two different behaviors of the samples, depending on the V_{GS} applied. For low V_{GS}, the $In_{0.7}Ga_{0.3}As$ is the poorest performing device at $V_{DS} = 0.6$ V, due to its high I_{OFF}, which degrades the efficiency and g_D. However, at $V_{DS} = 1$ V, it presents A_V values better than the $In_{0.53}Ga_{0.47}As$ samples due to the more pronounced diode behavior of the $In_{0.53}Ga_{0.47}As$ device at this bias.

For high V_{GS}, it is noticeable that the $In_{0.7}Ga_{0.3}As$ device has better A_V than the $In_{0.53}Ga_{0.47}As$ case, due to its better gm and V_{EA}, independent of the V_{DS} applied. Comparing the EOT scaling in the $In_{0.53}Ga_{0.47}As$ nTFET at high V_{GS} bias, it can be observed that the 2 nm HfO_2 device presents better A_V values for $V_{DS} = 0.6$ V, due to its better electrostatic coupling.

For V_{GS} higher than 0.4 V, where the diode behavior is suppressed, one important characteristic that can be observed is the peak presented in the A_V curve of all the samples. This A_V peak can be related with the conduction mechanism of the drain current, and it can be investigated by using the activation energy (E_a), presented in Fig. 10. The E_a is obtained using temperature-dependent measurements, using the Arrhenius plot [23]. When the BTBT starts to dominate the transport, where A_V starts to become more constant, gm has its maximum increase rate. Beyond that onset point the gm increase rate becomes lower (Fig. 3). While gm presents this behavior, g_D continues to increase in a more linear progression with the increasing V_{GS}, and when g_D starts to increase more than gm, A_V starts to degrade, which in turns results in this peak in the A_V curve.

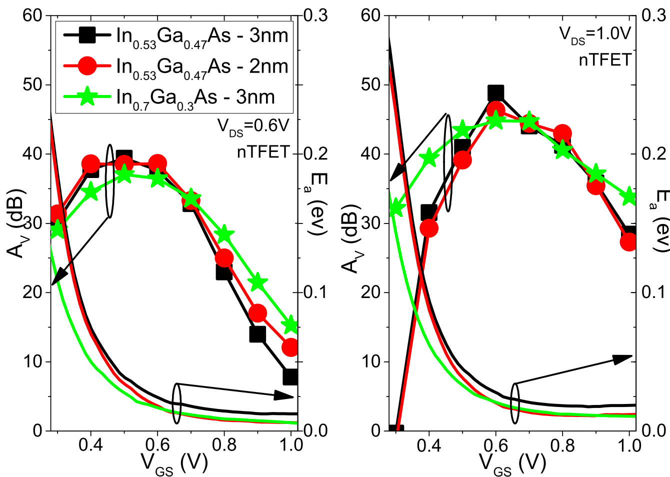

Fig. 10. Experimental A_V and E_a as a function of V_{GS} for $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ (both EOTs) nTFETs, with V_{DS} of 0.6 and 1 V.

The A_Vs presented in Fig. 9 are compatible to Si NW-TFETs and better than the Si NW-MOSFETs reported in [22], showing good analog characteristics.

IV. Conclusion

In this paper, the analysis of the basic analog parameters is done for three different splits, i.e., $In_{0.53}Ga_{0.47}As$ with a 3 nm of HfO_2, $In_{0.53}Ga_{0.47}As$ with a 2 nm of HfO_2, and $In_{0.7}Ga_{0.3}As$ with a 3 nm of HfO_2. In the $In_{0.7}Ga_{0.3}As$ device, the bandgap is lower causing an improvement of the BTBT current and consequently enhancing I_{ON}. In this device, the V_{ON} is also lower, which improves I_{ON} even more. Although this lower bandgap promotes an increase of gm, it also degrades g_D, especially for low V_{GS} bias. A competition between these factors, gm improvement and g_D degradation, results in better A_V for $In_{0.53}Ga_{0.47}As$ at low V_{GS} and in better A_V for $In_{0.7}Ga_{0.3}As$ at high V_{GS}.

The use of a thinner EOT with the $In_{0.53}Ga_{0.47}As$ channel causes an improvement of the electrostatic coupling, enhancing I_{DS}, and consequently improving gm and A_V, especially for higher V_{GS}. The A_V of the samples is compatible to Si NW-TFETs and better than Si NW-MOSFETs presented in [22], but for lower V_{DS} and V_{GS} biases, proving itself to be useful for analog applications at low power and low voltage.

Although the $In_{0.7}Ga_{0.3}As$ device presents a slightly higher efficiency for the strong current conduction regime, the $In_{0.53}Ga_{0.47}As$ exhibits much better efficiency for the weak conduction regime. The $In_{0.53}Ga_{0.47}As$ nTFET with a 2 nm of HfO_2reveals the highest efficiency at weak conduction due to its SS, which reaches a minimum value of 56 mV/dec.

The A_V peak found in all the samples can be related to the V_{GS} corresponding with the onset of BTBT as the dominant transport mechanism. Near this V_{GS} bias, the gm enhancement is the highest and this enhancement starts to decay beyond the onset point. When the gm increase rate starts to become smaller than the g_D increase rate, which is more constant with V_{GS} increase, it results in a degradation of A_V, reducing its value for higher V_{GS}.

References

[1] W. M. Reddick and G. A. J. Amaratunga, "Silicon surface tunnel transistor," *Appl. Phys. Lett.*, vol. 67, no. 4, pp. 494–496, Jul. 1995.

[2] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, Aug. 2007.

[3] T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, "Double-gate strained-ge heterostructure tunneling FET (TFET) with record high drive currents and ≪60 mV/dec subthreshold slope," in *IEDM Tech. Dig.*, Dec. 2008, pp. 947–949.

[4] M. Kim, Y. Wakabayashi, R. Nakane, M. Yokoyama, M. Takenaka, and S. Takagi, "High I_{on}/I_{off} Ge-source ultrathin body strained-SOI tunnel FETs," in *IEDM Tech. Dig.*, Dec. 2014, pp. 331–334.

[5] H. Lu and A. Seabaugh, "Tunnel field-effect transistors: State-of-the-art," *IEEE J. Electron Device Soc.*, vol. 2, no. 4, pp. 44–49, Jul. 2014.

[6] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, "Boosting the on-current of a *n*-channel nanowire tunnel field-effect transistor by source material optimization," *J. Appl. Phys.*, vol. 104, no. 6, p. 064514, Sep. 2008.

[7] D. Leonelli, A. Vandooren, R. Rooyackers, S. De Gendt, M. M. Heyns, and G. Groeseneken, "Drive current enhancement in p-tunnel FETs by optimization of the process conditions," *Solid-State Electron.*, vols. 65–66, pp. 28–32, Nov./Dec. 2011.

[8] A. Vandooren *et al.*, "Analysis of trap-assisted tunneling in vertical Si homo-junction and SiGe hetero-junction tunnel-FETs," *Solid-State Electron.*, vol. 83, pp. 50–55, May 2013.

[9] M. Schmidt *et al.*, "Line and point tunneling in scaled Si/SiGe heterostructure TFETs," *IEEE Electron Device Lett.*, vol. 35, no. 7, pp. 699–701, Jul. 2014.

[10] S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, and S. Datta, "Temperature-dependent *I–V* characteristics of a vertical $In_{0.53}Ga_{0.47}As$ tunnel FET," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 564–566, Jun. 2010.

[11] S. Takagi, M.-S. Kim, M. Noguchi, K. Nishi, and M. Takenaka, "Tunneling FET device technologies using III–V and Ge materials," in *Proc. Symp. Energy Efficient Electron. Syst. (E3S)*, Oct. 2015, pp. 1–2.

[12] D. Verreck *et al.*, "Uniform strain in heterostructure tunnel field-effect transistors," *IEEE Electron Device Lett.*, vol. 37, no. 3, pp. 337–340, Mar. 2016.

[13] E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind, and L.-E. Wernersson, "Vertical InAs/GaAsSb/GaSb tunneling field-effect transistor on Si with S = 48 mV/decade and I_{on} = 10 μA/μm for I_{off} = 1 nA/μm at V_{DS} = 0.3 V," in *IEDM Tech. Dig.*, Dec. 2016, pp. 500–503.

[14] R. Pandey *et al.*, "Performance benchmarking of p-type $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ and $Ge/Ge_{0.93}Sn_{0.07}$ hetero-junction tunnel FETs," in *IEDM Tech. Dig.*, Dec. 2016, pp. 521–523.

[15] A. Mallik and A. Chattopadhyay, "Tunnel field-effect transistors for analog/mixed-signal system-on-chip applications," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 888–894, Apr. 2012.

[16] P. G. D. Agopian, J. A. Martino, R. Rooyackers, A. Vandooren, E. Simoen, and C. Claeys, "Experimental comparison between trigate p-TFET and p-FinFET analog performance as a function of temperature," *IEEE Trans. Electron Devices*, vol. 60, no. 8, pp. 2493–2497, Aug. 2013.

[17] P. G. D. Agopian *et al.*, "NW-TFET analog performance for different Ge source compositions," in *Proc. IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, Oct. 2013, pp. 1–2.

[18] P. G. D. Agopian *et al.*, "Influence of the source composition on the analog performance parameters of vertical nanowire-TFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 1, pp. 16–22, Jan. 2015.

[19] Q.-T. Zhao *et al.*, "Strained Si and SiGe nanowire tunnel FETs for logic and analog applications," *IEEE J. Electron Device Soc.*, vol. 3, no. 3, pp. 103–114, May 2015.

[20] P. G. D. Agopian *et al.*, "Intrinsic voltage gain of line-TFETs and comparison with other TFET and MOSFET architectures," in *Proc. EuroSOI-ULIS*, Jan. 2016, pp. 13–15.

[21] M. D. V. Martino *et al.*, "Analog performance of vertical nanowire TFETs as a function of temperature and transport mechanism," *Solid-State Electron.*, vol. 112, pp. 51–55, Oct. 2015.

[22] P. G. D. Agopian *et al.*, "Comparison between vertical silicon NW-TFET and NW-MOSFETfrom analog point of view," in *Proc. EuroSOI-ULIS*, Jan. 2015, pp. 233–236.

[23] C. C. M. Bordallo *et al.*, "Impact of the NW-TFET diameter on the efficiency and the intrinsic voltage gain from a conduction regime perspective," *IEEE Trans. Electron Devices*, vol. 63, no. 7, pp. 2930–2935, Jul. 2016.

[24] B. Sedighi, X. S. Hu, H. Liu, J. J. Nahas, and M. Niemier, "Analog circuit design using tunnel-FETs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 1, pp. 39–48, Jan. 2015.

[25] M. D. V. Martino, J. A. Martino, and P. G. D. Agopian, "Performance comparison between TFET and FinFET differential pair," in *Proc. Symp. Microelectron. Technol. Devices (SBMicro)*, Aug./Sep. 2015, pp. 1–4.

[26] M. D. V. Martino, J. A. Martino, and P. G. D. Agopian, "Analysis of TFET and FinFET differential pairs with active load from 300 K to 450 K," in *Proc. EuroSOI-ULIS*, Jan. 2016, pp. 246–249.

[27] T. Mori *et al.*, "Demonstrating performance improvement of complementary TFET circuits by ION enhancement based on isoelectronic trap technology," in *IEDM Tech. Dig.*, Dec. 2016, pp. 512–515.

[28] M. Noguchi *et al.*, "High I_{on}/I_{off} and low subthreshold slope planar-type InGaAs tunnel field effect transistors with Zn-diffused source junctions," *J. Appl. Phys.*, vol. 118, no. 4, p. 045712, 2015.

[29] A. Alian *et al.*, "Record performance InGaAs homo-junction TFET with superior SS reliability over MOSFET," in *IEDM Tech. Dig.*, Dec. 2015, pp. 823–826.

[30] A. Alian *et al.*, "InGaAs tunnel FET with sub-nanometer *EOT* and sub-60 mV/dec sub-threshold swing at room temperature," *Appl. Phys. Lett.*, vol. 109, p. 243502, Dec. 2016.

[31] R. E. Nahory, M. A. Pollack, W. D. Johnson, and R. L. Barns, "Band gap versus composition and demonstration of Vegard's law for $In_{1-X}Ga_XAs_YP_{1-Y}$ lattice matched to InP," *Appl. Phys. Lett.*, vol. 33, no. 7, pp. 659–661, Oct. 1978.

[32] A. S. Verhulst, D. Leonelli, R. Rooyackers, and G. Groeseneken, "Drain voltage dependent analytical model of tunnel field-effect transistors," *J. Appl. Phys.*, vol. 110, p. 024510, Jul. 2011.

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