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Parasitic Conduction on Ω-Gate Nanowires SOI nMOSFETs

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In this work is analyzed the influence of fixed charges and interface traps on the subthreshold region of Ω-Gate Nanowires SOI nMOSFETs devices with different channel width (W_{fin}) and length (L). The implementation of the fixed charges on the back interface (channel/buried oxide) results in a parasitic conduction in this region, reducing the effective threshold voltage of the transistor. It was verified that the presence of these fixed charges and of the interface traps hardly affect the subthreshold swing due to the strong coupling among the interfaces.

Introduction

The use of low-power low-voltage (LPLV) devices becomes even more important nowadays where microelectronics products are present on everyone's life, as medical equipment (hearing aids and pacemaker), smart watches, self-powered devices and microsensors, as habitat monitoring, health, structural monitoring, and automotive sensing (1)(2) . The circuits operating on the subthreshold region are used on applications where the reduction of power consumptions is more important than the performance. Since the subthreshold current is exponentially related to the gate voltage, this relationship is expected to give an exponential reduction in power consumption, making operating in this region advantageous for the applications mentioned before (2).

The Ω-Gate nanowire (NW) SOI nMOSFETs is an excellent candidate for future technology nodes. The goal of this work is to study the Ω-Gate NW SOI nMOSFET working in subthreshold region for low-power low-voltage (LPLV) application, with special attention on a possible parasitic drain current conduction.

Devices Characteristics

The studied devices are Ω-Gate nanowires SOI nMOSFETs that were fabricated at CEA-LETI/France with the following characteristics: the effective oxide thickness (EOT) of 1.3nm, the buried oxide thickness (t_{oxb}) of 145nm and the channel height (h_{fin}) of 11nm with three channel width (W_{NW}) 220, 40 and 10nm and four channel lengths (L) 40, 100, 200nm and 1μm. In this work, the channel width (W_{NW}) refers to the horizontal diameter of the transistor channel.

Figure 1 shows scanning electron microscopy (SEM) (left) and cross-sectional transmission electron microscopy (TEM) (right) images of t Ω-Gate NW SOI MOSFETs.

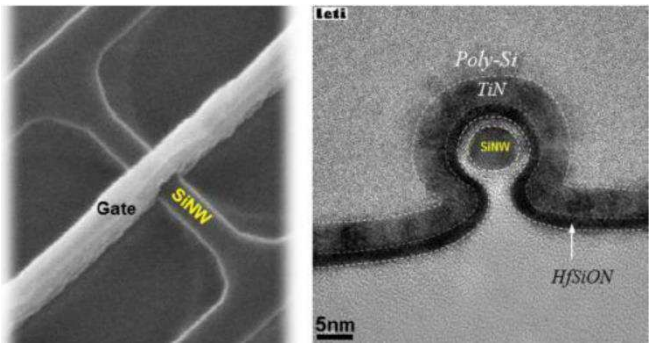

Figure 1 – SEM (left) and TEM (right) images of Ω-Gate NW SOI MOSFETs (3).

The measurements of the devices were done varying the voltage from gate to source (V_{GS}) from -2 to 1.2V and with a drain to source voltage (V_{DS}) of 50mV.

Results

Figure 2 presents the curve of the drain current (I_{DS}) as a function of gate voltage (V_{GS}) from which the electrical parameters such as threshold voltage (V_T) and subthreshold swing (SS) (Fig.3) were extracted. The curve for W_{NW}=220nm presents a displacement when compared with the other two curves. To understand the reason of this displacement, some simulations were done and they are presented in figure 4.

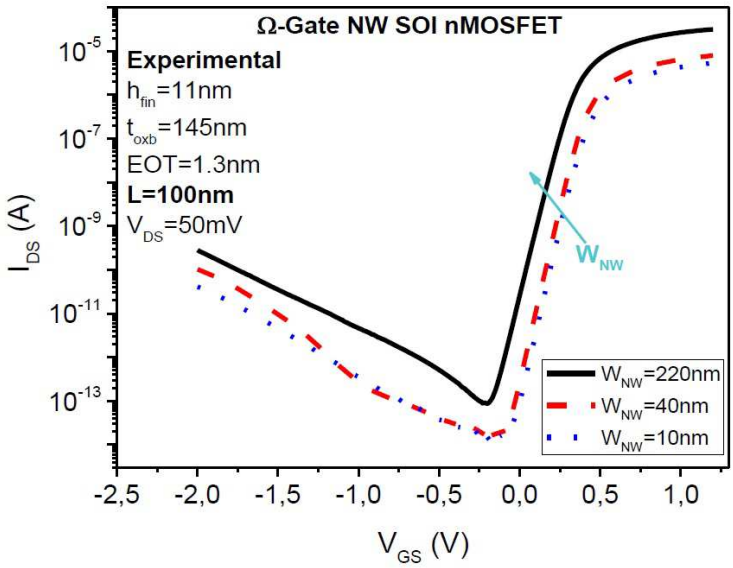

Figure 2 – Experimental drain current as a function of gate voltage, for channel length of 100 nm and V_{DS}=50mV.

Figure 3 presents the experimental extract threshold voltage (V_T) and subthreshold swing (SS) of the three analyzed W_{NW}. It is possible to see that short channel devices present a SS degradation as well as present a V_T variation for all channel widths, improving for narrow width as expected. However, focusing on V_T behavior, an unexpected reduction on the V_T values is observed for wider channel width even for long devices.

Aiming to better understand this unexpected behavior, some simulations were performed using TCAD Sentaurus, Synopsis® (4). It was simulated the device with channel

width (W_{NW}) of 220nm and channel length (L) of 100nm, the others characteristics as the channel height (h_{fin}) were the same of the experimental devices.

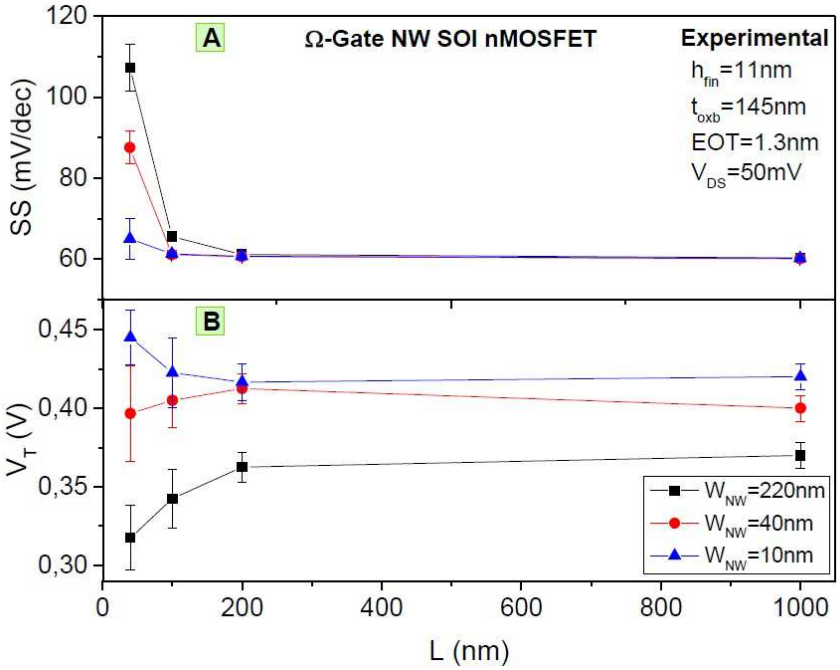

Figure 3 – Experimental subthreshold swing (A) and threshold voltage (B) as a function of channel length, for V_{DS}=50mV.

Figure 4, shows the simulated transfer characteristic for device with the same characteristics of the experimental one. It was observed that in order to have a good agreement of the simulated with the experimental data, it was necessary to include the interface fixed charges of $5x10^{11}cm^{-3}$.

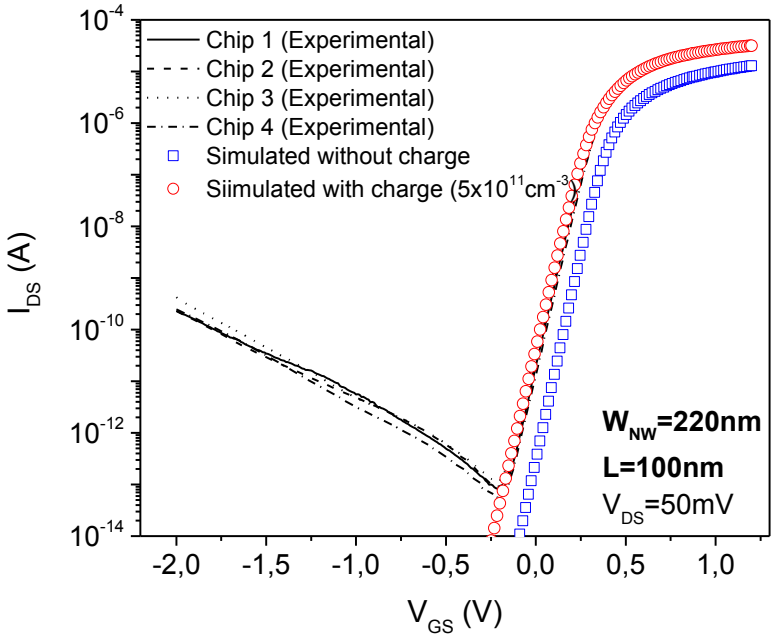

Figure 4 – Simulated drain current as a function of gate voltage for W_{NW}=220nm and L=100nm.

The presence of positive fixed charges changes the back interface conduction condition, that means, the device can be conducting by the back interface (channel/buried oxide). To analyze this conduction, were done some simulations varying the fixed charge concentration from $5x10^{11}cm^{-3}$ up to $1x10^{13}cm^{-3}$ at back interface.

Figure 5 shows the curves with different fixed charges concentrations, where it is possible to notice that the increase of fixed charges causes a parasitic conduction from drain to source at the back interface.

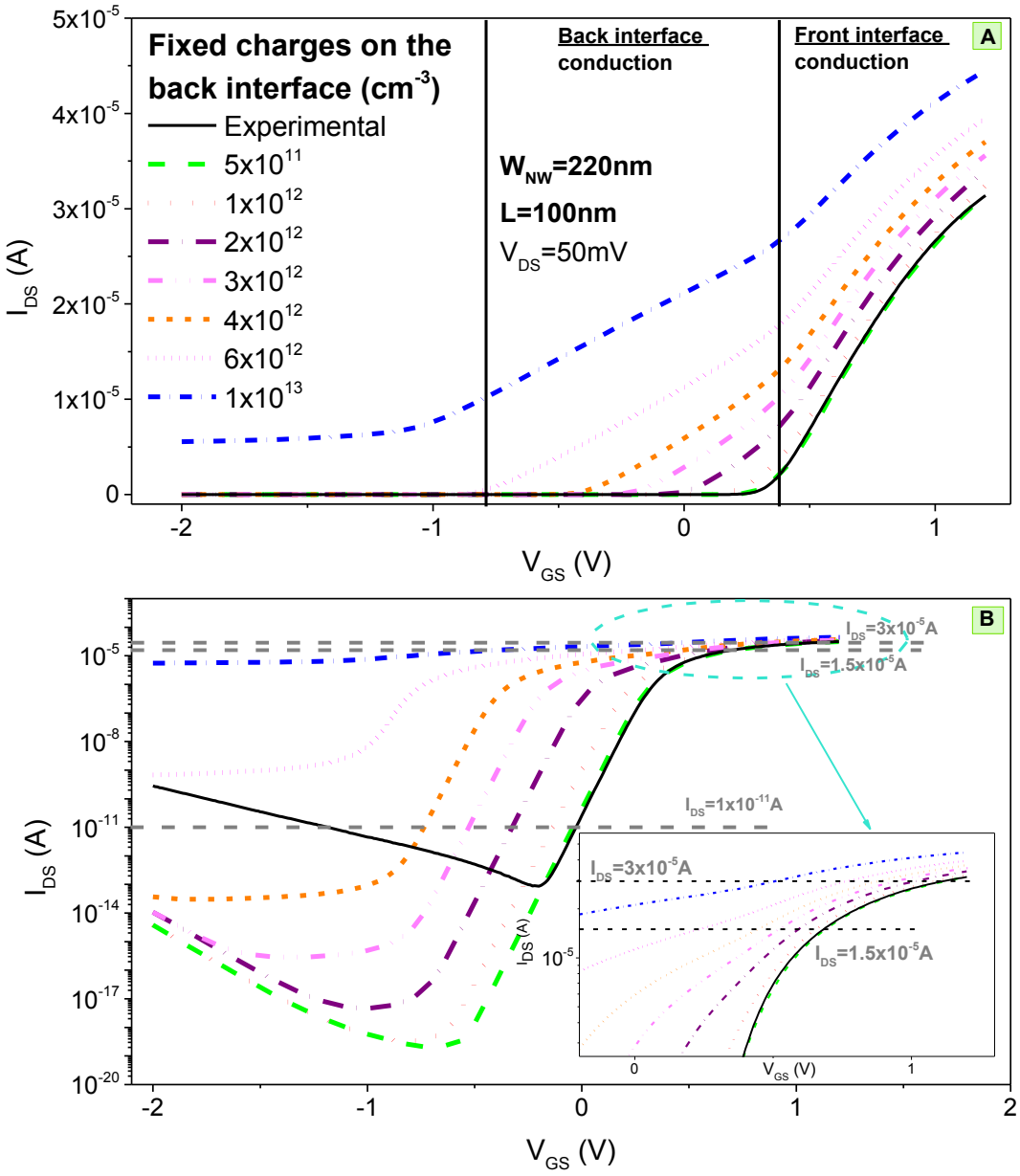

Figure 5 – Simulated drain current as a function of gate voltage in linear (A) and logarithmic (B) scale.

Aiming to analyze the back conduction, three different values of I_{DS} were adopted, as can be seen in figure 5B. Analyzing the current density on the front and back interface in figure 6, it can be noted that on the first point, that is located on the subthreshold slope (Fig.6A), the conduction is mainly composed by the back interface for all fixed charges level. When getting closer to V_T (Fig.6B) the conduction by the front interface starts to increase but the device characteristics is still affect by the back conduction and then after

V_T (Fig.6C) the front interface predominates. The transition of predominant conduction from the back to the front interface usually causes an abnormal I_{DS} behavior that can be seen in the inset presented in figure 5B, where a kind of kink is clearly observed in the curves which the fixed charges is higher than $3x10^{12}cm^{-3}$.

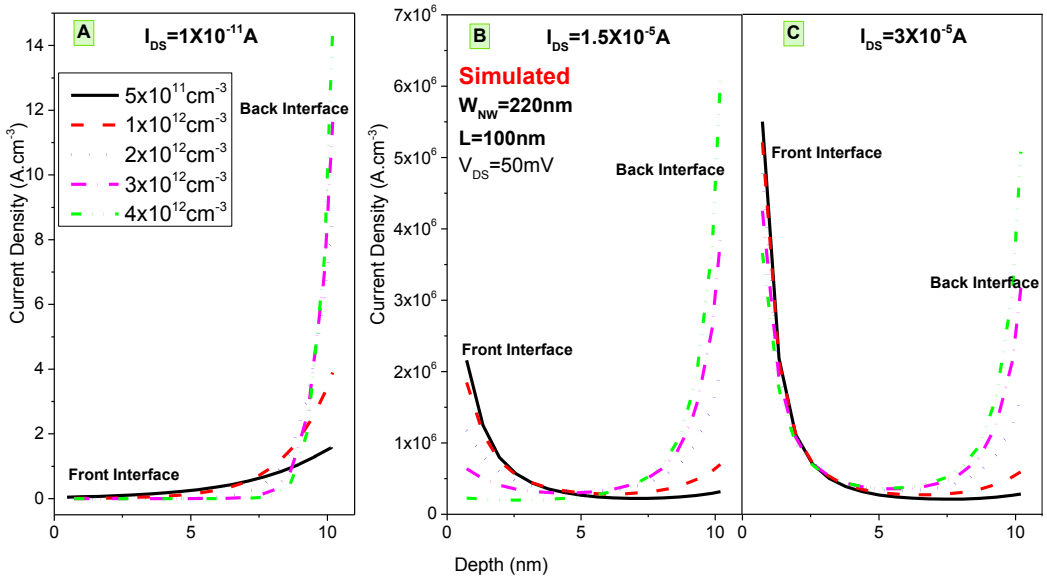

Figure 6 – Current density as a function of depth for three values of drain current.

Since the EOT is very thin, and the h_{fin} is 11nm, for fixed charges smaller than $3x10^{12}cm^{-3}$ the usual behavior degradation caused by back conduction (the SS increase or a hump in the subthreshold region) is not observed in the simulated results. This unexpected result can be explained by calculating the theoretical values of SS for the two different situations: 1) front and 2) back interface conduction, presenting and insignificant variation between the front and back SS values. This behavior can also be observed from the extracted SS values from the simulations varying the fixed charges, presented in table I. This SS immunity to back conduction happens because these devices have a very good coupling between the interfaces due to the thinner EOT and h_{fin}.

TABLE I – Subthreshold swing values for different fixed charges concentrations.

Fixed Charges (cm^{-3})	SS (mV/dec)
$5x10^{11}$	65.1
$1x10^{12}$	65.7
$2x10^{12}$	66.1
$3x10^{12}$	68.1
$4x10^{12}$	68.2

Although this device presents a higher SS immunity, the back interface conduction occurs early as the channel width becomes wider, resulting in smaller V_T for all channel lengths. This behavior is more pronounced as the fixed charge increases on the back interface. This behavior can also explain the reduction on V_T values for wider devices presented on the experimental results (Fig.3).

As the interface fixed charges did not present a significant variation on the SS, was performed some simulations adding the interface traps in the front interface (gate oxide/channel). The interface fixed charges were kept in $5x10^{11}cm^{-3}$ and the interface traps

concentrations were $1x10^{12}$ and $5x10^{12}cm^{-3}$. Figure 7 presents the simulated curves with the respective simulations.

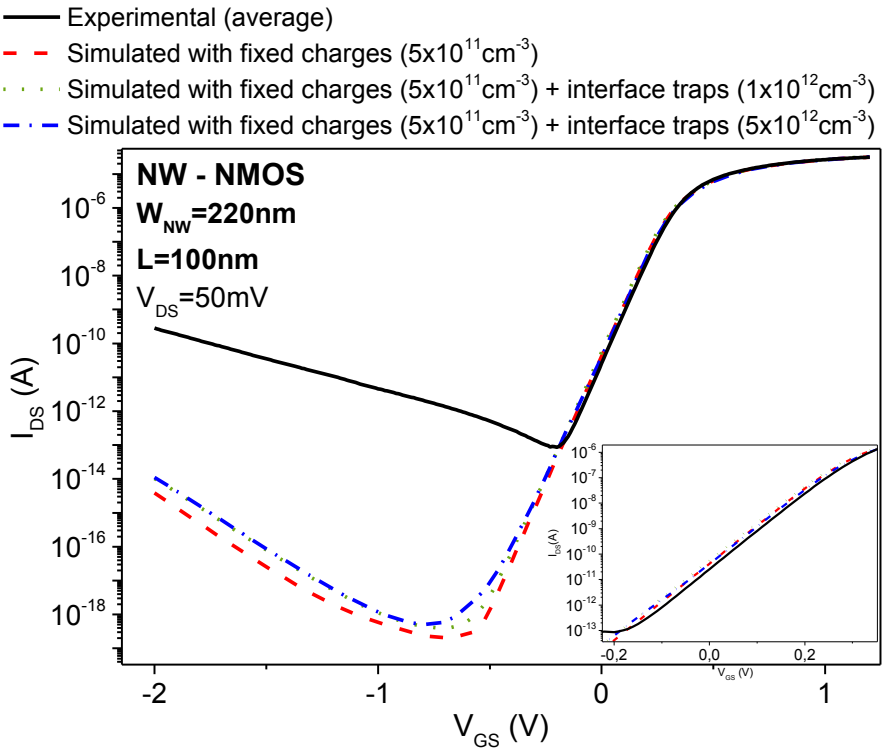

Figure 7 – Simulated drain current as a function of gate voltage with interface fixed charges and interface traps.

It is expected that the interface traps degrades the device performance, as a threshold voltage shift, subthreshold swing increase, and drain current degradation (5). However, when analyzing the simulations curves (Fig.7) and the SS extracted values from table II, it is presented an insignificant variation. Even when expanding the subthreshold region on the inset of figure 7, it is impossible to note a SS variation.

This SS immunity to fixed charges and interface traps is related to the EOT and the silicon height (h_{fin}) of these devices that is very thin and provides a very good coupling between the interfaces and when adding interface traps it did not affect the device behavior.

TABLE II – Subthreshold swing values for different fixed charges and interface traps concentration.

	SS (mV/dec)
Experimental (mean)	65.6
Fixed charges ($5x10^{11}$ cm^{-3})	65.1
Fixed charges ($5x10^{11}$ cm^{-3}) + interface traps ($1.10^{12}cm^{-3}$)	67.2
Fixed charges ($5x10^{11}$ cm^{-3}) + interface traps ($5.10^{12}cm^{-3}$)	67.2

Conclusions

The fixed charges on the back interfaces affects significantly the threshold voltage, reducing its values, due to the parasitic conduction on the back interface, reducing the control of V_T by the voltage applied at the gate. This behavior was observed experimentally for W_{NW}=220nm, and then confirmed by the numerical simulations.

The simulated fixed charges on the back interface and the interface traps did not presented a significant influence on the SS behavior for these devices. This immunity is

provided due to the thinner gate oxide of 1.3nm and the thinner silicon layer (h_{fin}) of 11nm that provides a very strong coupling between the interfaces. Then, for W_{NW}=220nm even with a back interface conduction and that provides a reduction of the channel charges control by the gate voltage, there is no important degradation in SS.

Acknowledgment

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